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1.0 GENERAL

This specification covers .039 inches vertical DDR II Low Profile & Very Low Profile sockets with blanked / formed contact designed for printed wiring board to dual in-line memory module interconnection. In all applications the mated system plating should be tin to tin or gold to gold. The specification is composed of the following section.

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2.0 APPLICABLE DOCUMENTS

The following document of the issue in effect on the date of the latest revision of this specification, shall form a part of this specification to the extent specified herein.

2.1 SPECIFICATIONS

Please refer to FCI released drawing. In the event of conflict between this document and product prints, the product prints shall take precedence.

2.2 OTHER STANDARD AND SPECIFICATION

- * UL-94 tests for flammability of plastic materials.
- * EIA 364 electrical connector/socket test procedures include environmental classification.
- * EIA-364-1000.01 environmental test methodology for assessing the performance of electrical connectors and sockets used in business office applications.

2.3 FCI SPECIFICATION

BUS-19-002

solderability test.

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DDR product specification.

3.0 REQUIREMENTTS

3.1 <u>DESIGN AND CONSTRUCTION</u>

Connectors shall be of the design construction and physical dimensions specified on the applicable product drawing.

3.2 MATERIAL

The material for each part shall be as specified herein or equivalent. The substitute material shall meet the performance requirement of this specification.

- 3.2.1 **CONTACTS** The contact shall be copper alloy, post plated.
- 3.2.2 <u>HOUSINGS</u> All housing material shall be rated flame retardant 94V-0 in accordance with UL-94. The housing shall be glass filled, nylon, or other high performance resin.
- 3.2.3 **EJECTORS** The material of ejector shall be high performance resin.

3.3 <u>FINISH</u>

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The finish for applicable components shall be specified herein or equivalent reference BUS-02-057.

- 3.3.1 CONTACT COATING: Gold plating over 50 microinches min. Nickel underplated.
- 3.3.2 SOLDER TAIL COATING: 100~120 microinches Tin/Lead or Tin/Copper plating over 50 microinches min. Nickel underplate.
- 3.3.3 Connector P/N with "LF" suffix means lead free plating and Rohs compatible.

3.4 <u>MECHANICAL CHARACTERISTICS</u>

3.4.1 <u>WORKMANSHIP</u>

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DDR 2 connectors shall be uniform in quality and shall be free from burrs, scratch, cracks, voids, chips, blisters pinholes, and other defects that will adversely affect the performance.

3.4.2 CONTACT RETENTION

The individual contact retention shall not be less than 0.67 lbs (300 gf) while applying a downward axial load to the support member of the contact. (per EIA 364-29; no movement > 0.38 mm)

3.4.3 FORKLOCK RETENTION FORCE:

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The forklock retention force shall be 3 lbs min per forklock. (per EIA 364-29; no movement > 0.38 mm)

3.4.4 <u>DURABILITY</u>

After 25 mating cycles with maximum thickness-gage at a rate of 5 inches / minute. There shall be no damage to the housing or contacts. The connector shall meet all electrical and mechanical characteristics.

3.4.5 INSERTION FORCE (CONNECTOR WITH 3 FORKLOCKS TO PCB)

Insert connector to PCB with max forklock hole (dim 2.45 +0/-0.05 mm) and nominal forklock hole (dim 2.45 +0.05/-0). Per EIA 364-05 at a rate of 0.2 inches / minute, the insertion force no more than 22.4 lbs.

3.4.6 <u>SOLDERABILITY</u>

Per EIA 364-52, class 1, category 3. There shall have a solder coverage of 95% minimum.

3.4.7 MATING/UNMATING FORCE

The total force to mate a connector and DDR 2 module should not exceed 24 lbs. The unmating force no less than 14 gf per pin pair. Test per EIA 364-05 and EIA 364-13 accordingly, with speed of 0.2 inch / minute.

3.4.8 <u>LATCH OPEN FORCE</u>

Pull test on latch parallel to PCB seating plan with 1.37 mm FBD module card. The force should not exceed 7.3 lbs.

3.4.9 RESEATING

Manual plug/ unplug the connector with module board. Perform 3 such cycles.

3.5 <u>ECECTRICAL CHARACTERISTICS</u>

3.5.1 **CURRENT RATING**

The maximum temperature rise per conductor should no more than 30 degree c with current of 0.5 ampere / pin. (per EIA 364-70).

3.5.2 <u>LOW LEVEL CONTACT RESISTANCE</u>

The low level contact resistance shall not exceed the value specified as below.

Maximum resistance (milli-ohms)

 $\begin{array}{ccc} \underline{\text{Initial}} & \underline{\text{After test}} \\ 30 & \text{Delta R} <= 10 \end{array}$

Test per EIA 364-23 (termination of connector to base board and add-in card shall be included in measurements).

3.5.3 DIELECTRIC WITHSTANDING VOLTAGE

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Per EIA 364-20, there shall no short circuit or insulation break down with 500 V.

3.5.4 <u>INSULATION RESISTANCE</u>

Per EIA 364-21, the insulation resistance shall be 1K Meg-ohm min with voltage of 500V.

3.5.5 INDUCTANCE

Per Intel "Vertical FB DIMM 240 position connector specification". Measure at 250 to 8.0 GHz. The signal loop inductance L11 shall be 3.7 to 5.0 nh. Mutual inductance between adjacent signals L12 shall be 2.0 nh max.

3.5.6 <u>CAPACITANCE</u>

Per Intel "Vertical FB DIMM 240 position connector specification". Measure at 250 to 8.0 GHz. The C11 (signal to ground) capacitance should be 1.3 to 2.0 pf, the C12 (coupling capacitance between adjacent signals) should be 0.3 pf max.

3.6 ENVIRONMENTAL CONDITIONS

3.6.1 PHYSICAL SHOCK

There shall be no evidence of physical damage per EIA 364-27. with test condition:

- (A) 20G, duration 11 ms of trapezoidal wave.
- (B) Module weight 40g +/- 10 g (no heat spreader) with center of gravity 17~22 mm from the module mating edge.
- (C) number of shocks: 3 shocks in each of 6 directions applied to three sample boards.

3.6.2 RANDOM VIBRATION

There shall be no evidence of physical damage. Per EIA 364-28 with test condition:

- (A) frequency range: $5 \text{ hz} \sim 500 \text{ hz}$.
- (B) Duration: 1 hour per axis for all 3 axis on all samples.
- (C) Module weight 40g +/- 10 g with center of gravity 17~22 mm from the module mating edge.

3.6.3 <u>HIGH TEMPERATURE LIFE</u>

Test per EIA 364 1000.01. 300 hours at temperature 105 degree c.

3.6.4 THERMAL SHOCK:

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Per EIA 364-32, test condition 1. cycle the connector -55 to +85 degree c. Dwell time of 30 minutes at extreme temperature. Transfer time 5 minutes max. No damage after 10 cycles.

3.6.5 CYCLIC TEMPERATURE AND HUMIDITY:

Per EIA 364-1000-01, test group 2. cycle the connector between 25 °C \pm 3°C at 90% rh and 65 °C \pm 3°C at 95% rh. Ramp times should be 2 hours and dwell times should be 2 hours. Dwell times start when the temperature and humidity have stabilized within the specified levels. Perform 60 such cycles. (Procedure per EIA 364-31)

3.6.6 MIXED FLOWING GAS:

Per EIA 364 1000.01, class IIA. Perform 5 days to simulate a 3-year field life for gold flash contact plating. 7 days (or above) to simulate a 5-year field life for 15u" or above contact gold plating.

3.6.7 THERMAL DISTURBANCE:

Cycle the connector between 15 $^{\circ}$ C \pm 3 $^{\circ}$ C and 85 $^{\circ}$ C \pm 3 $^{\circ}$ C , as measured on the part. Ramps should be a minimum of 2 $^{\circ}$ C per minute, and dwell times should insure that the contacts reach the temperature extremes(a minimum of 5 minutes) . Humidity is not controlled. Per EIA 364-1000.01 test group 4 . Perform 10 such cycles.

3.6.8 DUST:

Per EIA 364-91, the test specimens shall be unmated during the test.

4.0 PRODUCT QUALIFICATION PROVISIONS

4.1 EQUIPMENT CALIBRATION

All test equipment and inspection facilities used in the performance of any test shall be maintained a calibration system in accordance with MIL-C-45662.

4.2 INSPECTION CONDITIONS

Unless otherwise specified herein, all inspections shall be performed under the following ambient condition.

(a) Temperature : 25 + / - 5 degree c.

(b) Relative humidity: 30 to 80%

(c) Barometric pressure: local ambient

4.3 SAMPLE QUANITY AND DESCRIPTION:

Samples shall be selected at random from current production. The sample size shall be according to test sequence needed.

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4.4 QUALIFICATION TEST SEQUENCE: (Please see next 2 pages)

	Refer			TES	T SEQUE	ENCE		
Test Items	to	GROUP 1	GROUP 2	GROUP 3	GROUP 4	GROUP 5	GROUP 6	GROUP 7
Insertion force (connector to PCB)	3.4.5				-	1	0	,
Mating/ unmating force	3.4.7					2		
Contact retention	3.4.2					3		
Forklock retention force	3.4.3					4		
Physical shock	3.6.1			6				
Random vibration	3.6.2			4				
Inductance	3.5.5							1
Capacitance	3.5.6							2
Solderability	3.4.6					5		
Durability	3.4.4	2	2	2	2		3	
LLCR	3.5.2	1,4,6	1,4,7	1,3,5,	1,4,6, 8,10		2,5	
Insulation resistance	3.5.4		6					
Dielectric withstanding voltage	3.5.3						1,4	
Current rating	3.5.1							3
High temperature life	3.6.3	3			3			
Cycling temperature & humidity	3.6.5		5					
Thermal disturbance	3.6.7				7			
Thermal shock	3.6.4		3					
Mixed flowing gas	3.6.6				5			
Reseating	3.4.10	5	8		9			

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Sample quantity		5	5	5	5	5	5	5
	Refer			TES	T SEQUE	NCE		
Test Items	to	GROUP 8	GROUP 9	GROUP 10	GROUP 11			
Latch open force	3.4.8							
Contact retention	3.4.2							
Forklock retention force	3.4.3							
Physical shock	3.6.1							
Random vibration	3.6.2	5						
Solderability	3.4.6							
Durability	3.4.4	2	2	2	2			
LLCR	3.5.2	1,4,6	1,4,6	1,4,6,	1,4,6,			
Insulation resistance	3.5.4		6					
Dielectric withstanding voltage	3.5.3							
Current rating	3.5.1							
High temperature life	3.6.3	3	3	3				
Cycling temperature & humidity	3.6.5							
Thermal disturbance	3.6.7		7	5	5			
Thermal shock	3.6.4							
Mixed flowing gas	3.6.6		5					
Reseating	3.4. 10		9	7	7			
Dust	3.6.8				3			
Sample quantity		5	5	5	5			

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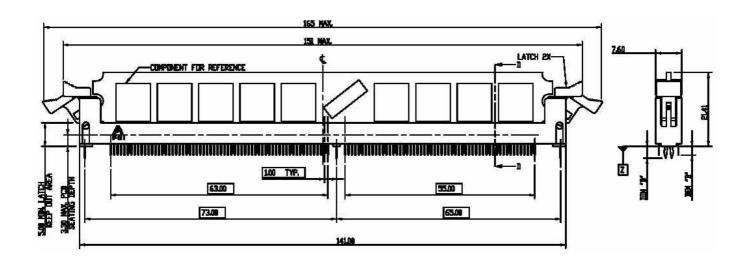
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5 PACKAGING AND SHIPPING

- 5.3 Packing the packing and packaging shall be in accordance with industry standard practice in a manner to insure carrier acceptance and safe delivery to destination per FCI packaging specification.
- 5.4 Packaging marking each shipping container shall be clearly marked with the name of the contents, the amount of contained, the FCI part number, and the name of the receiving part, as listed in the procurement.

6 THE PROFILE OF DDR 2 LOW PROFILE CONNECTOR:

- A. Please see FCI customer drawing for details)
- B. Please see FCI drawing for DDR2 240P Very Low Profile connector profile.

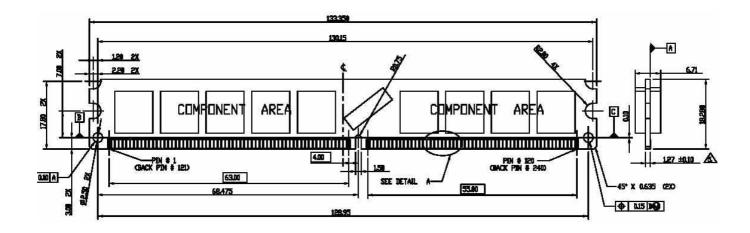


Low Profile Product outline

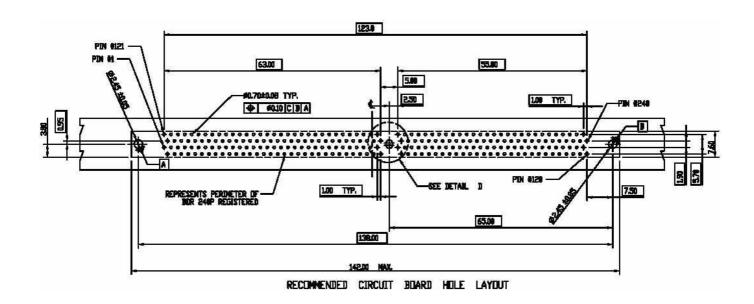
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Recommend module card outline



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REVISION RECORD

REV	PAGE	DESCRIPTION	EC#	DATE
Α	All	NEW RELEASE	T05-0298	2/17/06

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