HMC605LP3 / 605LP3E

v04.1013

GAAS PHEMT MMIC LOW NOISE AMPLIFIER w/ BYPASS MODE, 2.3 - 2.7 GHz

Typical Applications

The HMC605LP3 / HMC605LP3E is ideal for:

- Wireless Infrastructure
- Customer Premise Equipment
- Fixed Wireless
- WiMAX & WiBro
- Tower Mounted Amplifiers

Features

Noise Figure: 1.1 dB

Output IP3: +31 dBm

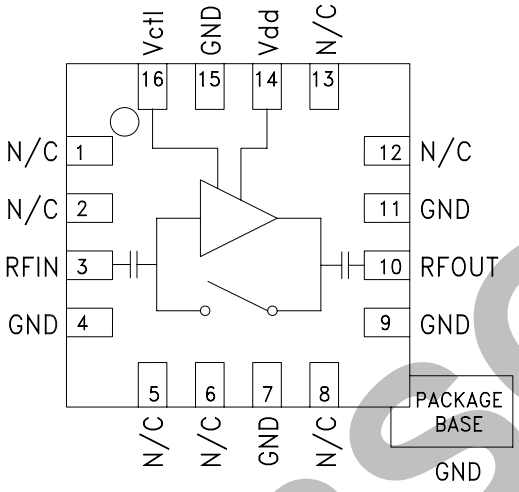
Gain: 20 dB

Low Loss & Failsafe Bypass Path

Single Supply: +3V or +5V

50 Ohm Matched Output/Input

Functional Diagram



General Description

The HMC605LP3 / HMC605LP3E are versatile, high dynamic range GaAs MMIC Low Noise Amplifi ers that integrate a low loss LNA bypass path on the IC. The amplifi er is ideal for WiBro & WiMAX receivers operating between 2.3 and 2.7 GHz and provides 1.1 dB noise figure, 20 dB of gain and +31 dBm output IP3 from a single supply of +5V @ 74 mA. Input and output return losses are 14 and 15 dB respectively with no external matching components required. A single control line (Vctl) is used to switch between LNA mode and a low 2 dB loss bypass mode and reduces the current consumption to 10 µA. The HMC605LP3 is failsafe and will default to the bypass mode with no DC power applied.

Electrical Specifications, T_A = +25° C, Vdd = 5V

Parameter		LNA Mode			Bypass Mode			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range			2.3 - 2.7			2.3 - 2.7		GHz
Gain		17.5	20.5		-3.0	-2.0		dB
Gain Variation Over Temperature			0.012			0.002		dB / °C
Noise Figure			1.1	1.3				dB
Input Return Loss			14			13		dB
Output Return Loss			15			13		dB
Reverse Isolation			33					dB
Power for 1dB Compression (P1dB)[1]			17			14		dBm
Third Order Intercept (IP3) [2]			31			23		dBm
Supply Current (Idd)			74	90		0.01		mA
Switching Speed	LNA Mode to Bypass Mode		-			6.0		ns
	Bypass Mode to LNA Mode		60			-		ns

[1] P1dB and IIP3 is referenced to RFOUT for LNA mode and to RFIN for Bypass Mode.

[2] For LNA Mode: Input tone power is -20 dBm/tone at 1 MHz tone spacing.
For Bypass Mode: Input tone power is 0dBm/tone at 1MHz tone spacing

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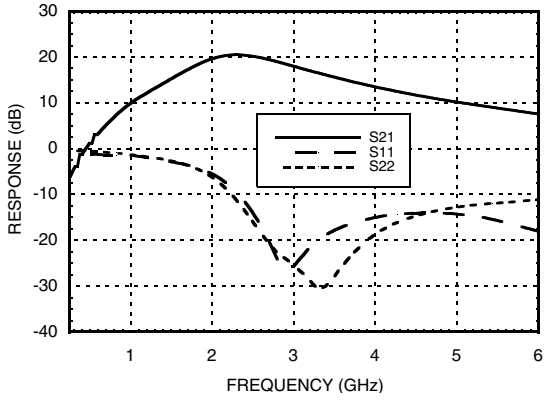
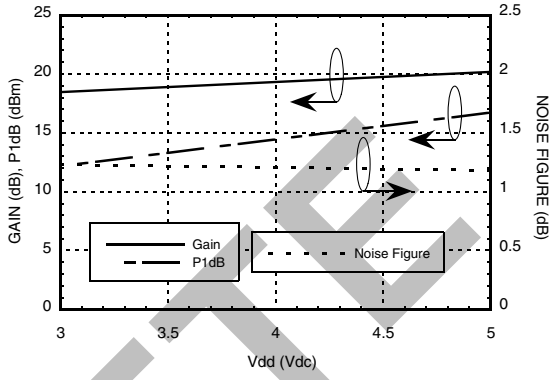
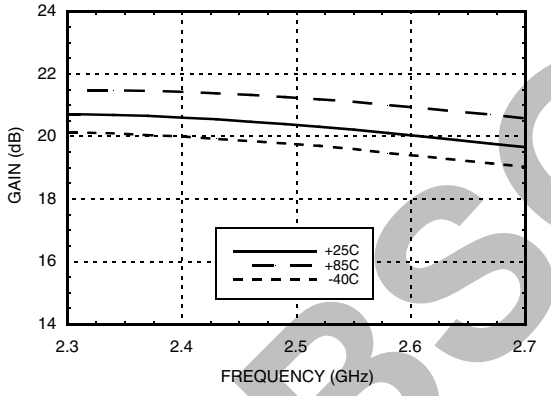
LNA Broadband Gain & Return Loss



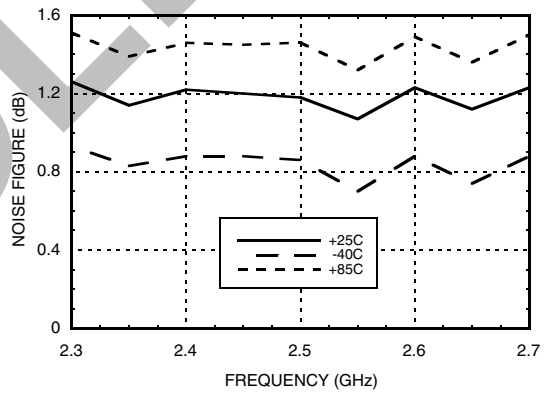
LNA Gain, Noise Figure & Power vs. Supply Voltage @ 2.5 GHz



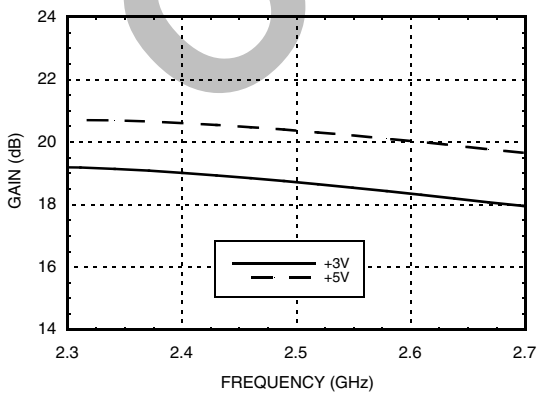
LNA Gain vs. Temperature



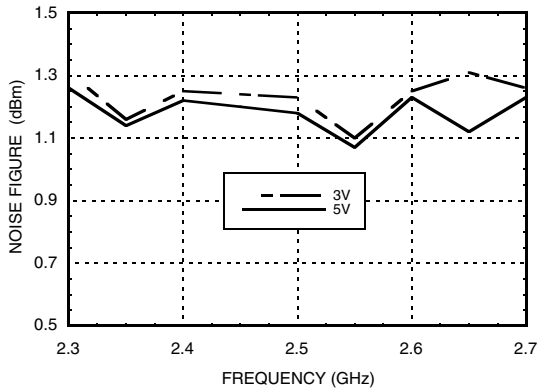
LNA Noise Figure vs. Temperature



LNA Gain vs. Vdd



LNA Noise Figure vs. Vdd



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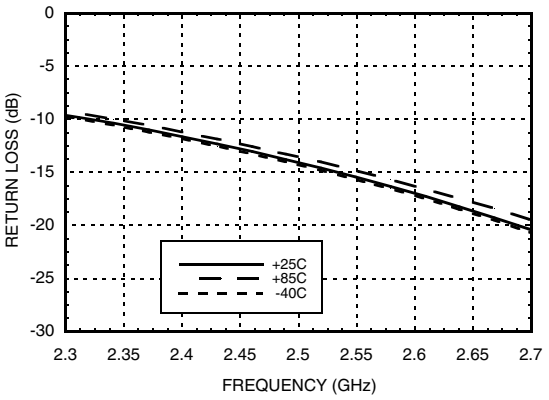
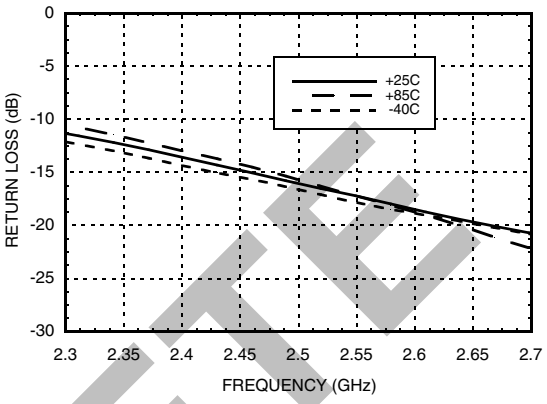
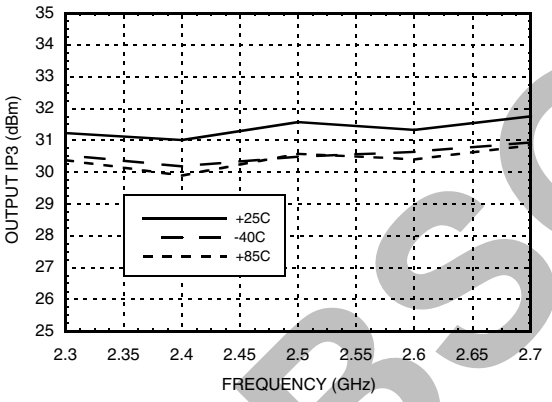
LNA Input Return Loss vs. Temperature



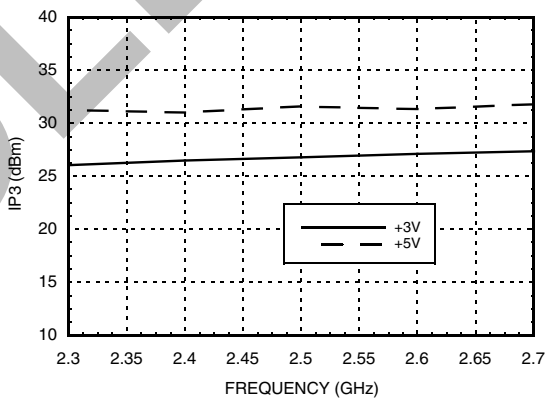
LNA Output Return Loss vs. Temperature



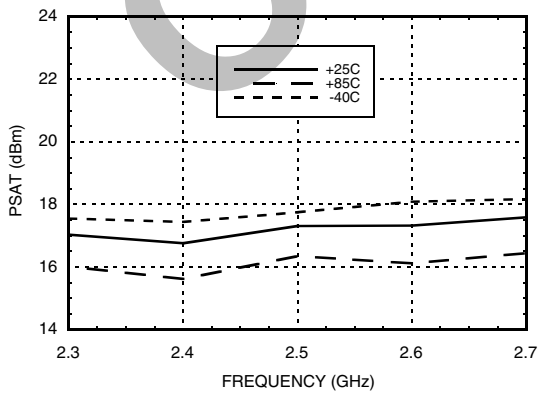
LNA Output IP3 vs. Temperature



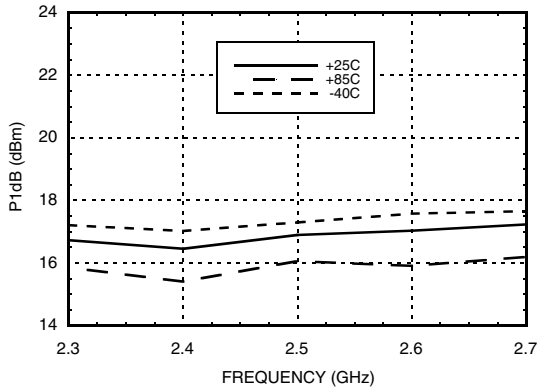
LNA Output IP3 vs. Vdd



LNA Psat vs. Temperature



LNA Output P1dB vs. Temperature



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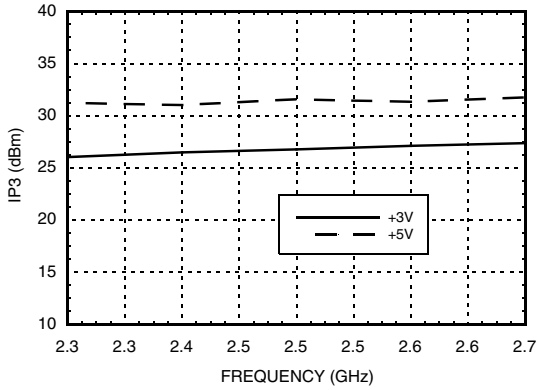
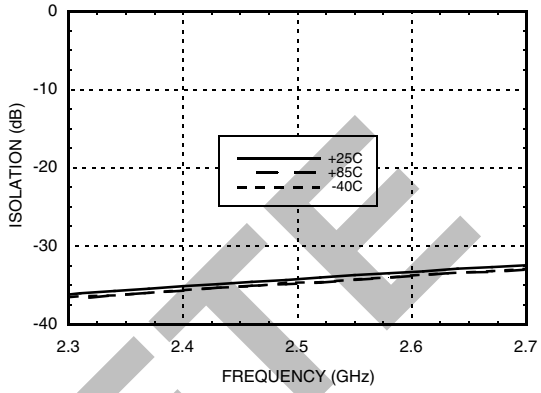
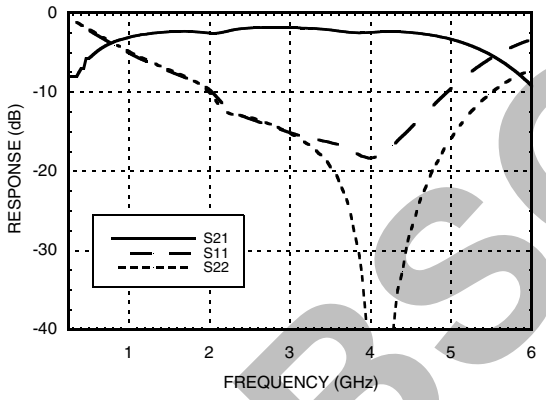
LNA Output P1dB vs. Vdd



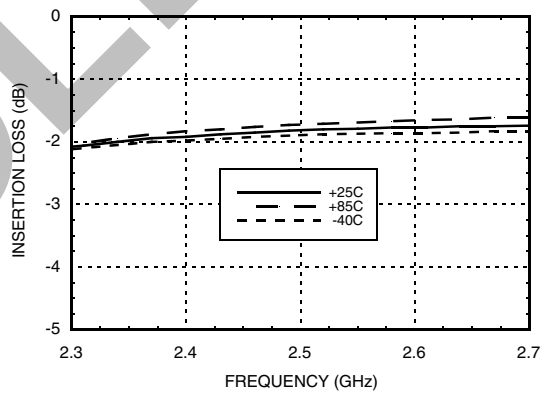
LNA Reverse Isolation vs. Temperature



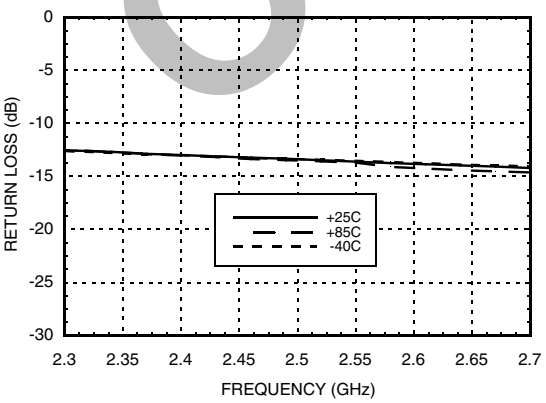
Bypass Mode Broadband Gain & Return Loss



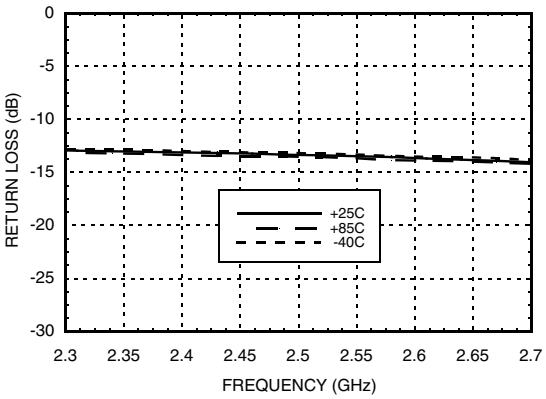
Bypass Mode Insertion Loss vs. Temperature



Bypass Mode Input Return Loss vs. Temperature [1]



Bypass Mode Output Return Loss vs. Temperature [1]



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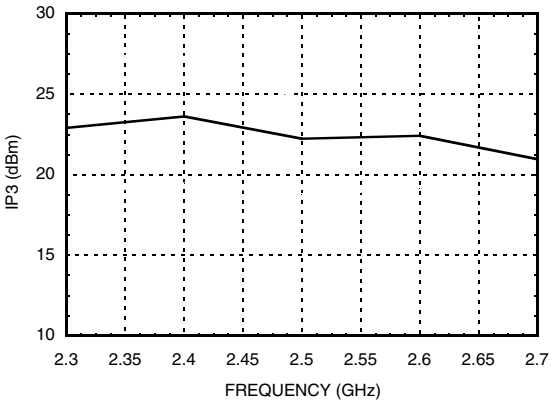
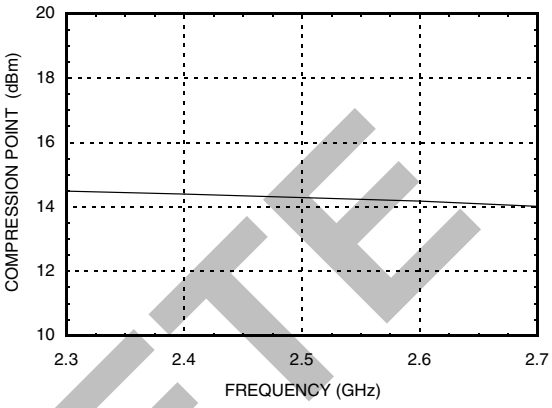
Bypass Mode Input IP3 vs. Frequency



Bypass Mode Input P1dB vs. Frequency



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Absolute Maximum Ratings

Drain Bias Voltage (Vdd)		+8 Vdc
RF Input Power (RFIN) (Vdd = +5.0 Vdc)	LNA Mode Bypass Mode	+22 dBm +30 dBm
Channel Temperature		150 °C
Continuous Pdiss (T = 85 °C) (derate 15.85 mW/°C above 85 °C)		1.03 mW
Thermal Resistance (channel to ground paddle)		63.08 °C/W
Storage Temperature		-65 to +150° C
Operating Temperature		-40 to +100° C

Typical Supply Current vs. Vdd

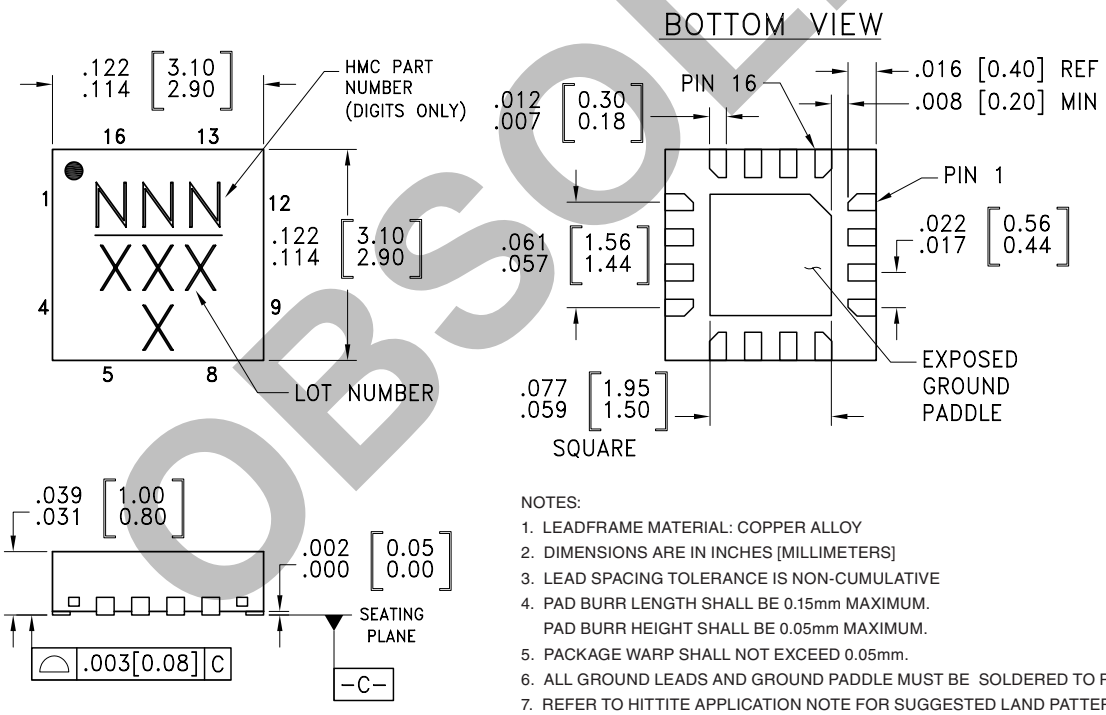
Vdd (Vdc)	Idd (mA)
+3.0	28
+5.0	74

Truth Table

LNA Mode	Vctl= Vdd ± 0.3V
Bypass Mode	Vctl= 0 ± 0.3V

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC605LP3	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	605 XXXX
HMC605LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	605 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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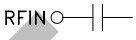
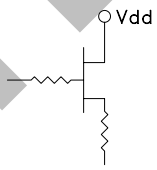
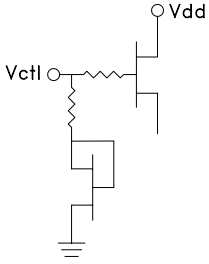
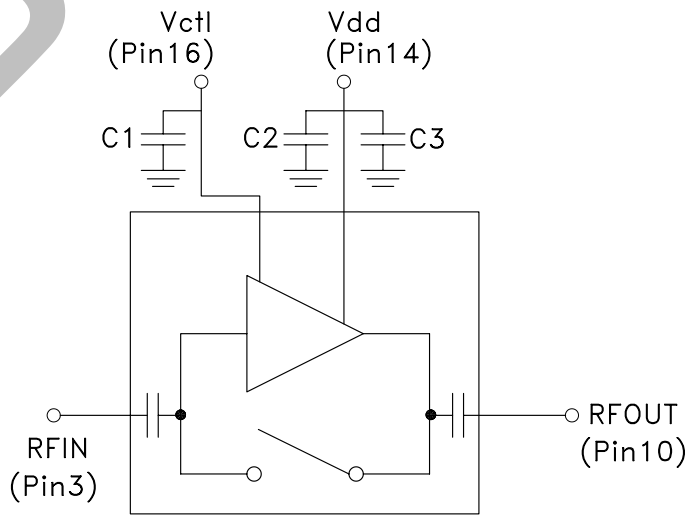
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 2, 5, 6, 8, 12	N/C	No connection necessary. These pins may be connected to RF/DC ground.	
3	RFIN	This pin is AC coupled and matched to 50 Ohms.	
4, 7, 9, 11, 15	GND	These pins must be connected to RF/DC ground.	
10	RFOUT	This pin is AC coupled and matched to 50 Ohms.	
14	Vdd	Power supply voltage. Bypass capacitors are required. See application circuit.	
16	Vctl	LNA/Bypass Mode Control Voltage. See truth table.	

Application Circuit

Components	Value
C1, C2	100pF
C3	10KpF



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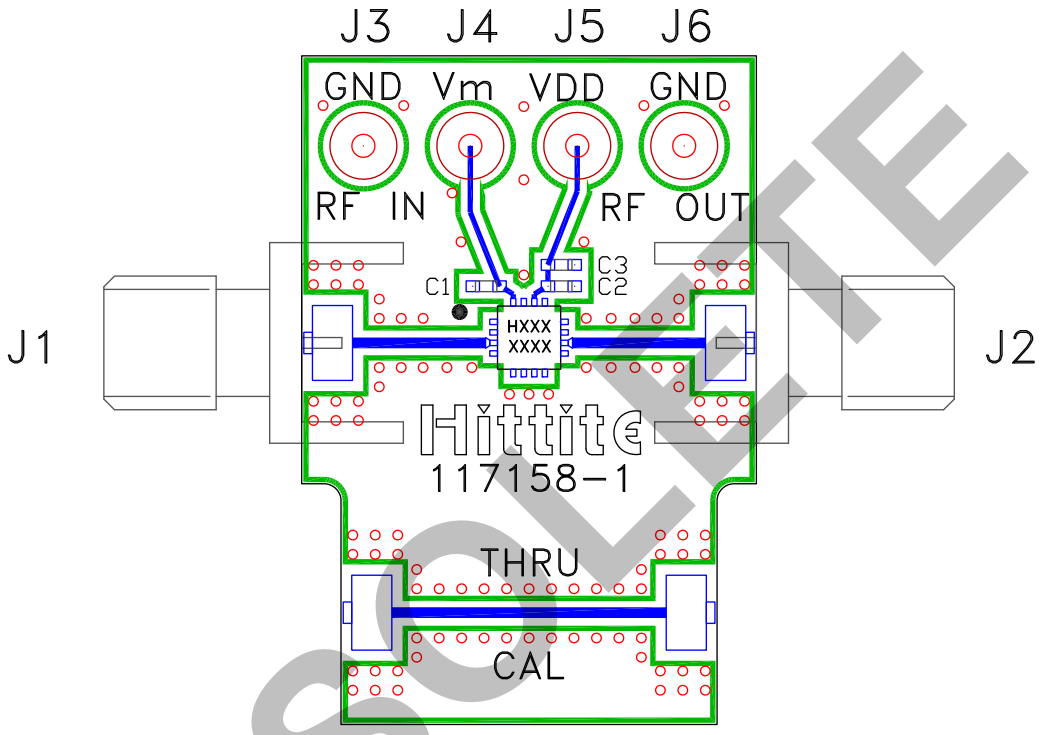
Evaluation PCB



List of Materials for Evaluation PCB 117160 [1]

Item	Description
J1 - J2	PCB Mount SMA RF Connector
J3 - J6	DC Pin
C1, C2	100 pF Capacitor, 0402 Pkg.
C3	10 KpF Capacitor, 0402 Pkg.
U1	HMC605LP3 / 605LP3E Amplifier
PCB [2]	117158 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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