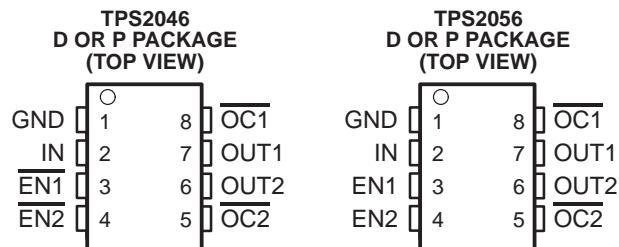


features

- 135-mΩ -Maximum (5-V Input) High-Side MOSFET Switch
- 250 mA Continuous Current per Channel
- Independent Short-Circuit and Thermal Protection With Overcurrent Logic Output
- Operating Range . . . 2.7-V to 5.5-V
- Logic-Level Enable Input
- 2.5-ms Typical Rise Time
- Undervoltage Lockout
- 10 µA Maximum Standby Supply Current
- Bidirectional Switch
- Available in 8-pin SOIC and PDIP Packages
- Ambient Temperature Range, –40°C to 85°C
- 2-kV Human-Body-Model, 200-V Machine-Model ESD Protection

typical applications

- Notebook, Desktop and Palmtop PCs
- Monitors, Keyboards, Scanners, and Printers
- Digital Cameras, Phones, and PBXs
- Hot-Insertion Applications



description

The TPS2046 and TPS2056 dual power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely. These devices incorporate in single packages two 135-mΩ N-channel MOSFET high-side power switches for power-distribution systems that require multiple power switches. Each switch is controlled by a logic enable compatible with 5-V and 3-V logic. Gate drive is provided by an internal charge pump that controls the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS2046 and TPS2056 limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent (\overline{OCx}) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch causing the junction temperature to rise, a thermal protection circuit shuts off the switch in overcurrent to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

The TPS2046 and TPS2056 are designed to limit at 0.44-A load. These power distribution switches, available in 8-pin small-outline integrated circuit (SOIC) and 8-pin plastic dual-in-line packages (PDIP), operate over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

TA	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES	
				SOIC (D) [†]	PDIP (P)
–40°C to 85°C	Active low	0.25	0.44	TPS2046D	TPS2046P
–40°C to 85°C	Active high	0.25	0.44	TPS2056D	TPS2056P

[†] The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2046DR)

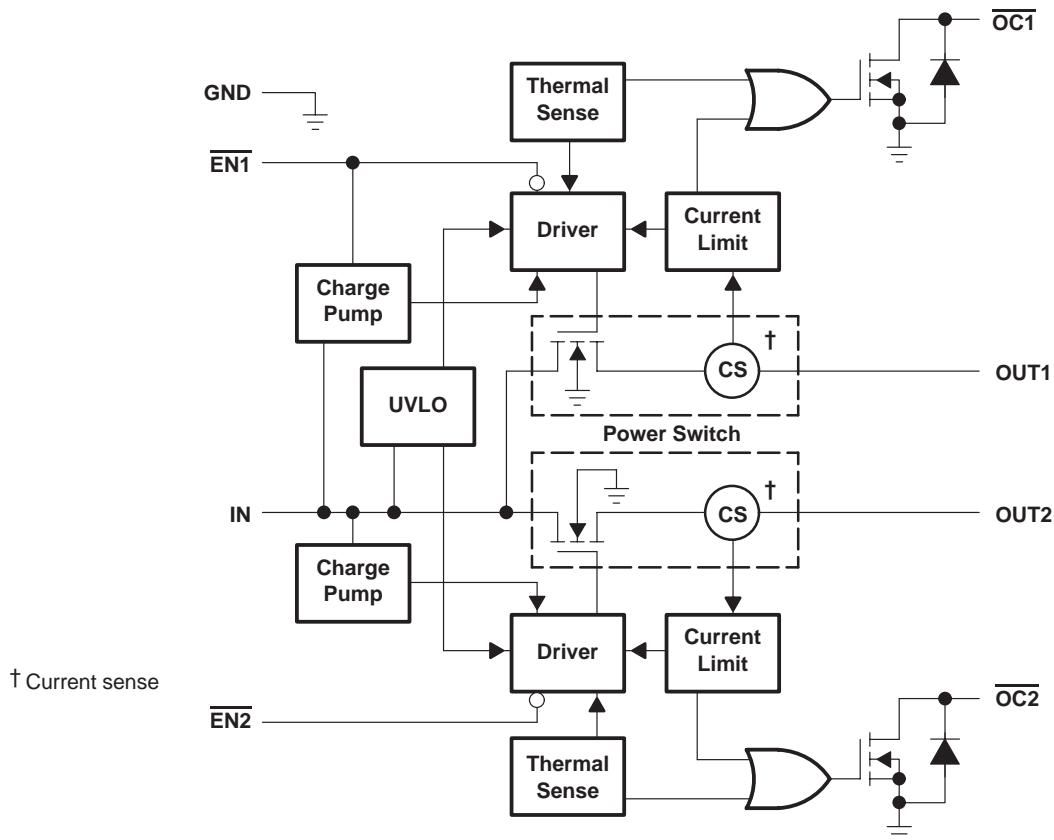


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TPS2046, TPS2056 DUAL CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES

SLVS183 – APRIL 1999

TPS2046 functional block diagram



Terminal Functions

NAME	TERMINAL		I/O	DESCRIPTION		
	NO.					
	D OR P					
	TPS2046	TPS2056				
EN1	3	–	I	Enable input. Logic low turns on power switch, IN-OUT1.		
EN2	4	–	I	Enable input. Logic low turns on power switch, IN-OUT2.		
EN1	–	3	I	Enable input. Logic high turns on power switch, IN-OUT1.		
EN2	–	4	I	Enable input. Logic high turns on power switch, IN-OUT2.		
GND	1	1	I	Ground		
IN	2	2	I	Input voltage		
OC1	8	8	O	Overcurrent. Logic output active low, for power switch, IN-OUT1		
OC2	5	5	O	Overcurrent. Logic output active low, for power switch, IN-OUT2		
OUT1	7	7	O	Power-switch output		
OUT2	6	6	O	Power-switch output		

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of $135\text{ m}\Omega$ ($V_{I(IN)} = 5\text{ V}$). Configured as a high-side switch, the power switch prevents current flow from OUTx to IN and IN to OUTx when disabled. The power switch can supply a minimum of 250 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable (\bar{EN}_x or EN_x)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than $10\text{ }\mu\text{A}$ when a logic high is present on \bar{EN}_x (TPS2046) or a logic low is present on EN_x (TPS2056). A logic zero input on \bar{EN}_x or logic high on EN_x restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent (\bar{OC}_x)

The \bar{OC}_x open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

The TPS2046 and TPS2056 implement a dual-threshold thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C , the internal thermal sense circuitry checks to determine which power switch is in an overcurrent condition and turns off that switch, thus isolating the fault without interrupting operation of the adjacent power switches. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The (\bar{OC}_x) open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

TPS2046, TPS2056 DUAL CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES

SLVS183 – APRIL 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Input voltage range, $V_{I(IN)}$ (see Note1)	–0.3 V to 6 V
Output voltage range, $V_{O(OUTx)}$ (see Note1)	–0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, $V_{I(ENx)}$ or $V_{I(ENx)}$	–0.3 V to 6 V
Continuous output current, $I_{O(OUTx)}$	internally limited
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 125°C
Storage temperature range, T_{STG}	–65°C to 150°C
Lead temperature soldering 1.6 mm (1/16 inch) from case for 10 seconds	260°C
Electrostatic discharge (ESD) protection: Human body model MIL-STD-883C	2 kV
Machine model	0.2 kV

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ C$	$T_A = 70^\circ C$	$T_A = 85^\circ C$
			POWER RATING	POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1175 mW	9.4 mW/°C	752 mW	611 mW

recommended operating conditions

	TPS2046		TPS2056		UNIT
	MIN	MAX	MIN	MAX	
Input voltage, $V_{I(IN)}$	2.7	5.5	2.7	5.5	V
Input voltage, $V_{I(ENx)}$ or $V_{I(ENx)}$	0	5.5	0	5.5	V
Continuous output current, $I_{O(OUTx)}$	0	250	0	250	mA
Operating virtual junction temperature, T_J	–40	125	–40	125	°C

TPS2046, TPS2056
DUAL CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES

SLVS183 – APRIL 1999

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)} = 5.5$ V, $I_O = \text{rated current}$, $V_{I(ENx)} = 0$ V, $V_{I(ENx)} = \text{Hi}$ (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS [†]	TPS2046			TPS2056			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation	$V_{I(IN)} = 5$ V, $T_J = 25^\circ\text{C}$, $I_O = 0.1$ A	80	95		80	95		mΩ
		$V_{I(IN)} = 5$ V, $T_J = 85^\circ\text{C}$, $I_O = 0.1$ A	90	120		90	120		
		$V_{I(IN)} = 5$ V, $T_J = 125^\circ\text{C}$, $I_O = 0.1$ A	100	135		100	135		
	Static drain-source on-state resistance, 3.3-V operation	$V_{I(IN)} = 3.3$ V, $T_J = 25^\circ\text{C}$, $I_O = 0.1$ A	85	105		85	105		
		$V_{I(IN)} = 3.3$ V, $T_J = 85^\circ\text{C}$, $I_O = 0.1$ A	100	135		100	135		
		$V_{I(IN)} = 3.3$ V, $T_J = 125^\circ\text{C}$, $I_O = 0.1$ A	115	150		115	150		
t_r	Rise time, output	$V_{I(IN)} = 5.5$ V, $T_J = 25^\circ\text{C}$, $C_L = 1 \mu\text{F}$, $R_L = 20 \Omega$	2.5		2.5				ms
		$V_{I(IN)} = 2.7$ V, $T_J = 25^\circ\text{C}$, $C_L = 1 \mu\text{F}$, $R_L = 20 \Omega$	3		3				
t_f	Fall time, output	$V_{I(IN)} = 5.5$ V, $T_J = 25^\circ\text{C}$, $C_L = 1 \mu\text{F}$, $R_L = 20 \Omega$	4.4		4.4				ms
		$V_{I(IN)} = 2.7$ V, $T_J = 25^\circ\text{C}$, $C_L = 1 \mu\text{F}$, $R_L = 20 \Omega$	2.5		2.5				

[†] Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input \overline{ENx} or ENx

PARAMETER		TEST CONDITIONS	TPS2046			TPS2056			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage	$2.7 \text{ V} \leq V_{I(IN)} \leq 5.5 \text{ V}$	2		2				V
		$4.5 \text{ V} \leq V_{I(IN)} \leq 5.5 \text{ V}$		0.8		0.8			
		$2.7 \text{ V} \leq V_{I(IN)} \leq 4.5 \text{ V}$		0.4		0.4			
I_I	Input current	TPS2046 $V_{I(ENx)} = 0$ V or $V_{I(ENx)} = V_{I(IN)}$	-0.5	0.5					μA
		TPS2056 $V_{I(ENx)} = V_{I(IN)}$ or $V_{I(ENx)} = 0$ V			-0.5	0.5			
t_{on}	Turn-on time	$C_L = 100 \mu\text{F}$, $R_L = 20 \Omega$		20		20			ms
t_{off}	Turn-off time	$C_L = 100 \mu\text{F}$, $R_L = 20 \Omega$		40		40			

current limit

PARAMETER		TEST CONDITIONS [†]	TPS2046			TPS2056			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short-circuit output current	$V_{I(IN)} = 5$ V, OUT connected to GND, Device enable into short circuit.	0.345	0.44	0.525	0.345	0.44	0.525	A

[†] Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

TPS2046, TPS2056

DUAL CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES

SLVS183 – APRIL 1999

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)} = 5.5$ V, $I_O = \text{rated current}$, $V_{I(ENx)} = 0$ V, $V_{I(ENx)} = \text{Hi}$ (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS				TPS2046			TPS2056			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUTx	$V_{I(ENx)} = V_{I(IN)}$	$T_J = 25^\circ\text{C}$	TPS2046	0.015	1		0.015	1		μA
			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$				10				
	No Load on OUTx	$V_{I(ENx)} = 0$ V	$T_J = 25^\circ\text{C}$	TPS2056				0.015	1		
			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$							10	
Supply current, high-level output	No Load on OUTx	$V_{I(ENx)} = 0$ V	$T_J = 25^\circ\text{C}$	TPS2046	80	100		80	100		μA
			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		100						
	No Load on OUTx	$V_{I(ENx)} = V_{I(IN)}$	$T_J = 25^\circ\text{C}$	TPS2056				100	100		
			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$							100	
Leakage current	OUTx connected to ground	$V_{I(ENx)} = V_{I(IN)}$	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	TPS2046	100			100	100		μA
		$V_{I(ENx)} = 0$ V	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	TPS2056							
Reverse leakage current	IN = high impedance	$V_{I(ENx)} = 0$ V	$T_J = 25^\circ\text{C}$	TPS2046	0.3			0.3	0.3		μA
		$V_{I(ENx)} = \text{Hi}$		TPS2056							

undervoltage lockout

PARAMETER	TEST CONDITIONS	TPS2046			TPS2056			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Low-level input voltage		2	2.5		2	2.5		V
Hysteresis	$T_J = 25^\circ\text{C}$	100			100			mV

overcurrent OCx

PARAMETER	TEST CONDITIONS	TPS2046			TPS2056			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Sink current [†]	$V_O = 5$ V		10			10		mA
Output low voltage	$I_O = 5$ mA, $V_{OL(OCx)}$		0.5			0.5		V
Off-state current [†]	$V_O = 5$ V, $V_O = 3.3$ V		1			1		μA

[†] Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

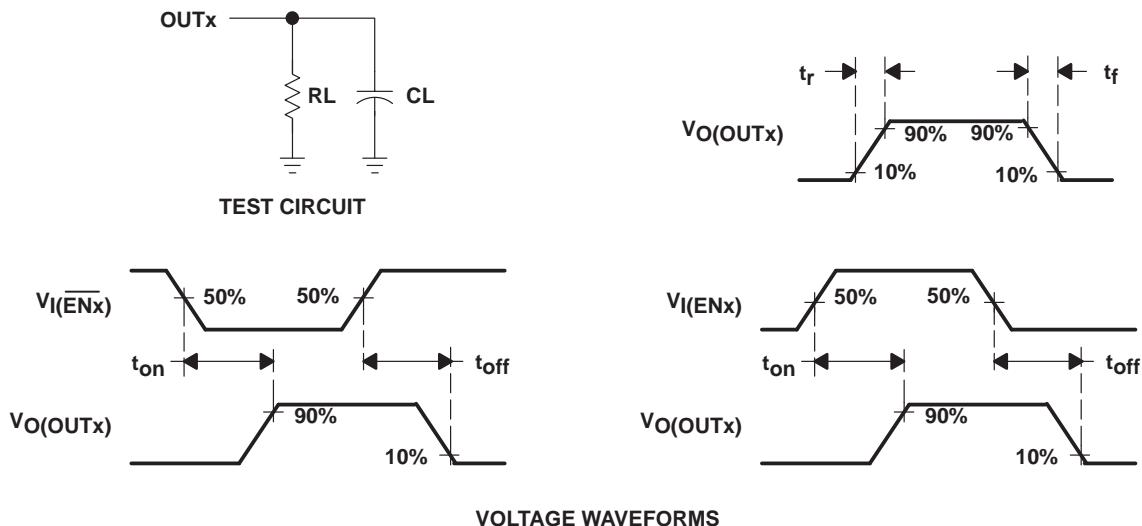


Figure 1. Test Circuit and Voltage Waveforms

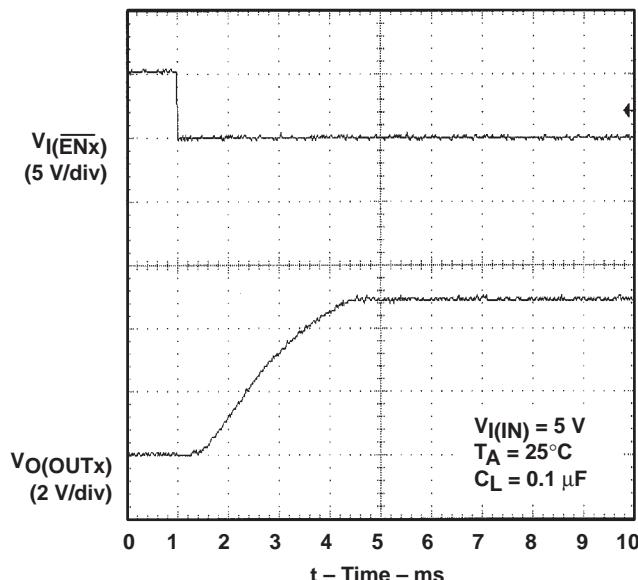


Figure 2. Turnon Delay and Rise Time with $0.1\text{-}\mu\text{F}$ Load

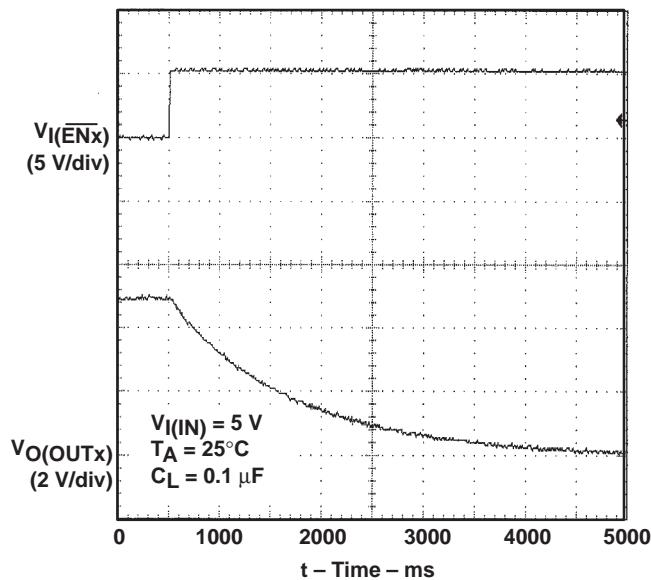


Figure 3. Turnoff Delay and Fall Time with $0.1\text{-}\mu\text{F}$ Load

TPS2046, TPS2056 DUAL CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES

SLVS183 – APRIL 1999

PARAMETER MEASUREMENT INFORMATION

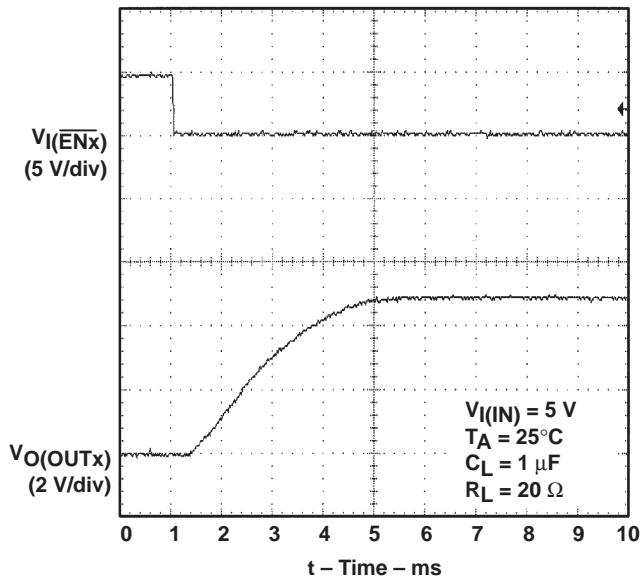


Figure 4. Turnon Delay and Rise Time with 1- μF Load

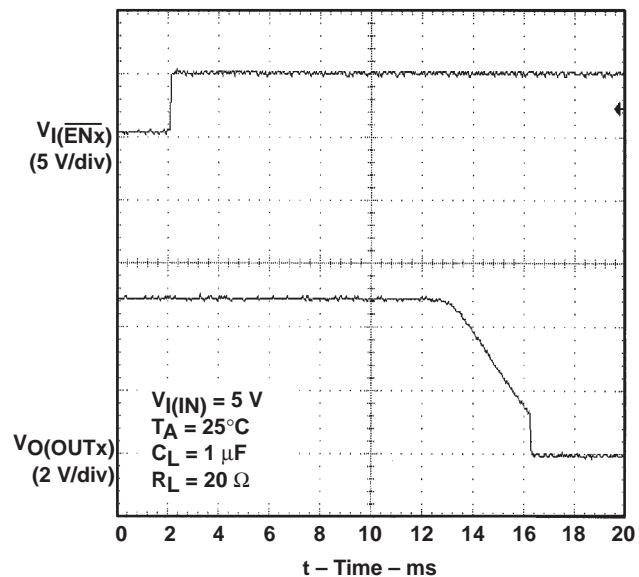


Figure 5. Turnoff Delay and Fall Time with 1- μF Load

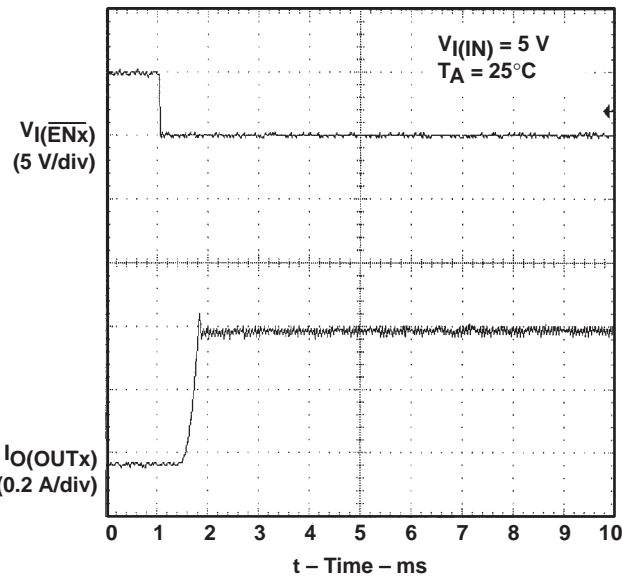


Figure 6. TPS2046, Short-Circuit Current, Device Enabled into Short

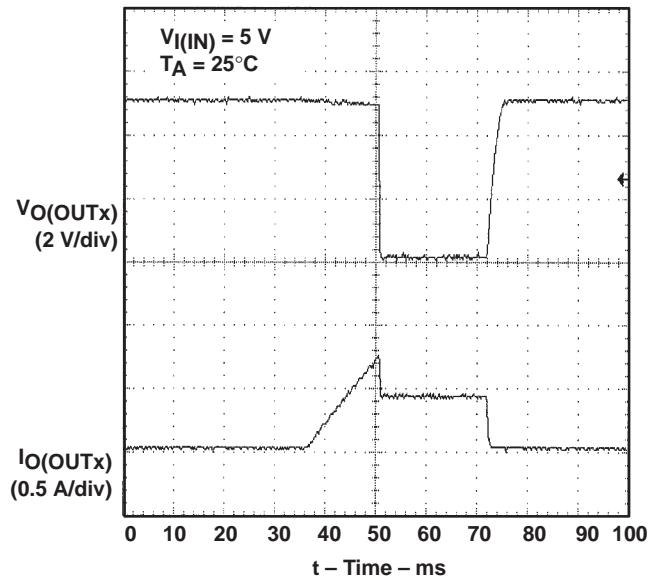


Figure 7. TPS2046, Threshold Trip Current with Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

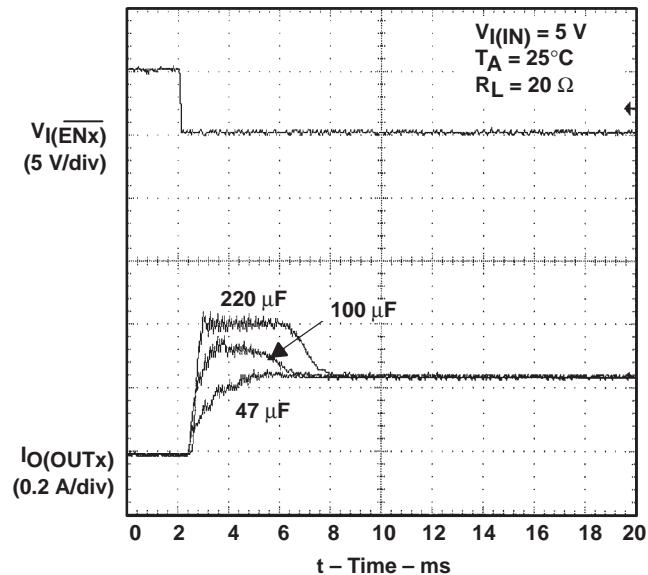


Figure 8. Inrush Current with 220- μF , 100- μF and 47- μF Load Capacitance

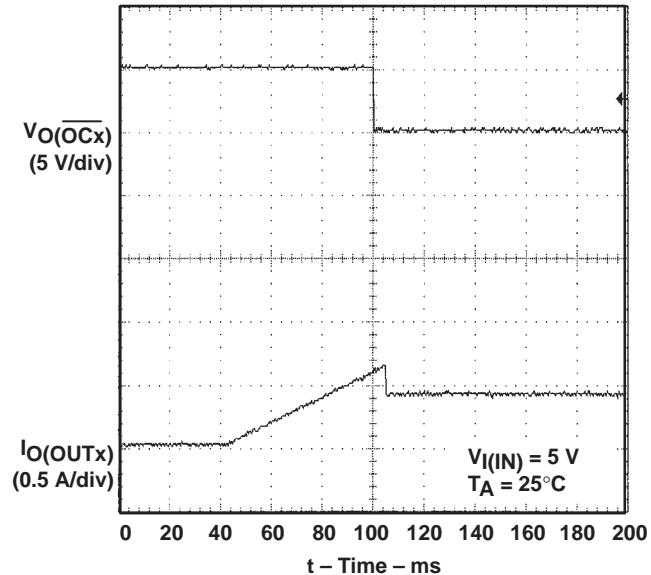


Figure 9. Ramped Load on Enabled Device

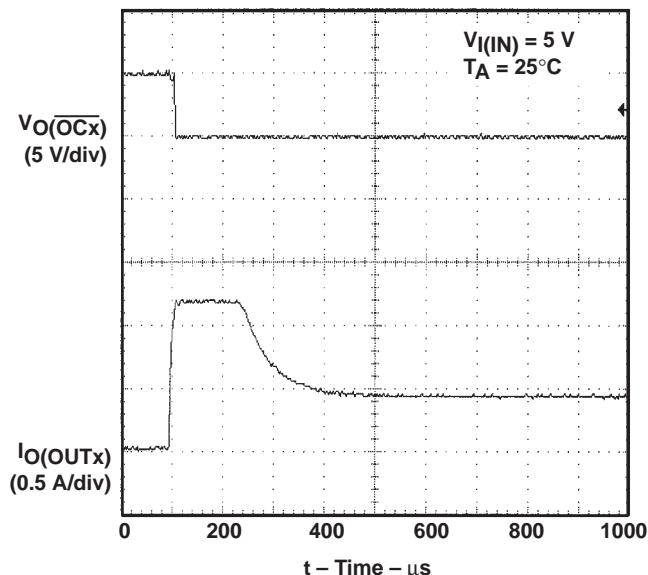


Figure 10. 4- Ω Load Connected to Enabled Device

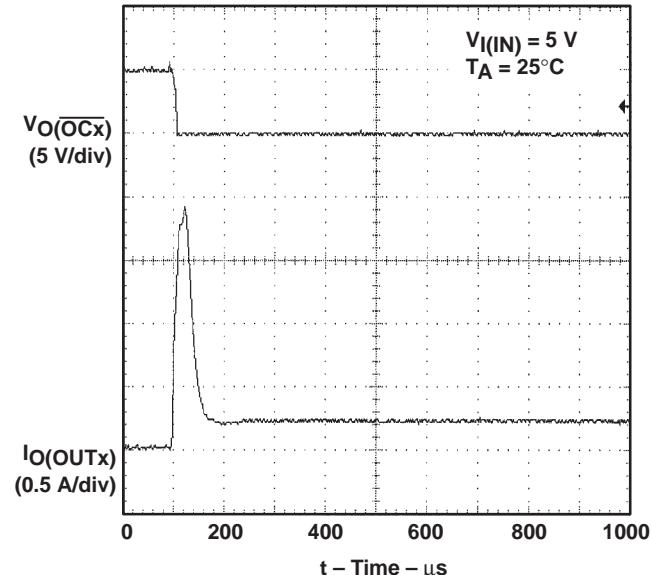


Figure 11. 1- Ω Load Connected to Enabled Device

TPS2046, TPS2056 DUAL CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES

SLVS183 – APRIL 1999

TYPICAL CHARACTERISTICS

TURNON DELAY
vs
INPUT VOLTAGE

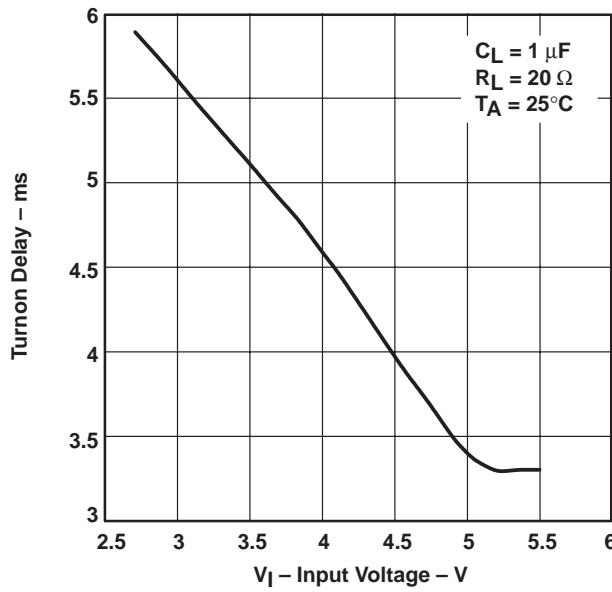


Figure 12

TOURNOFF DELAY
vs
INPUT VOLTAGE

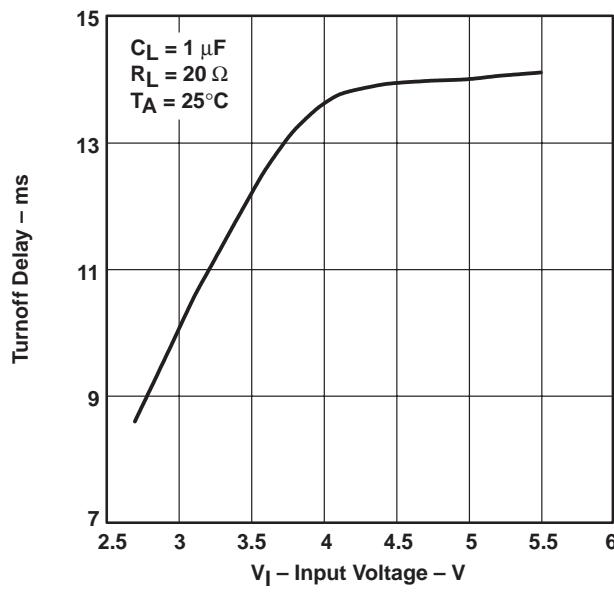


Figure 13

RISE TIME
vs
LOAD CURRENT

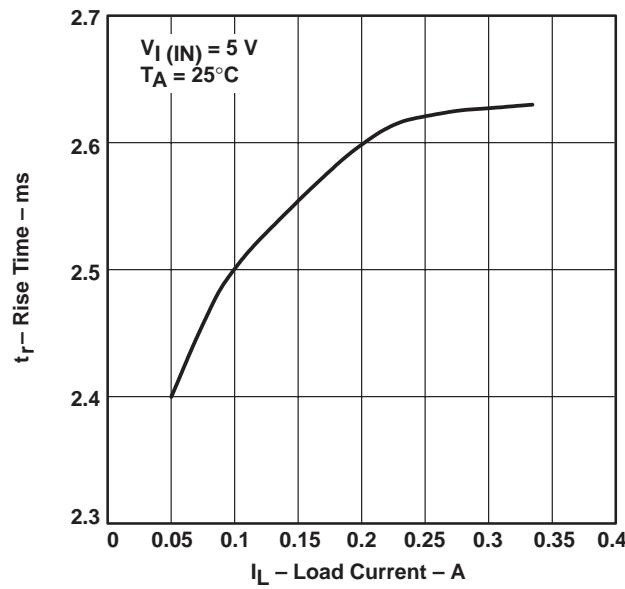


Figure 14

FALL TIME
vs
LOAD CURRENT

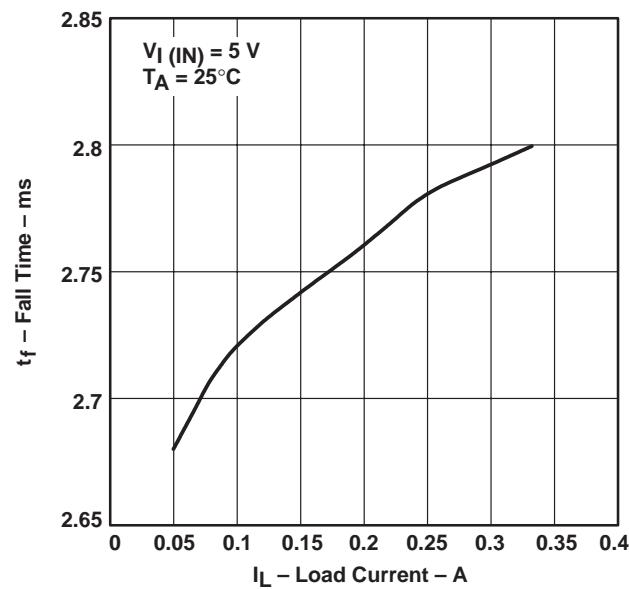


Figure 15

TYPICAL CHARACTERISTICS

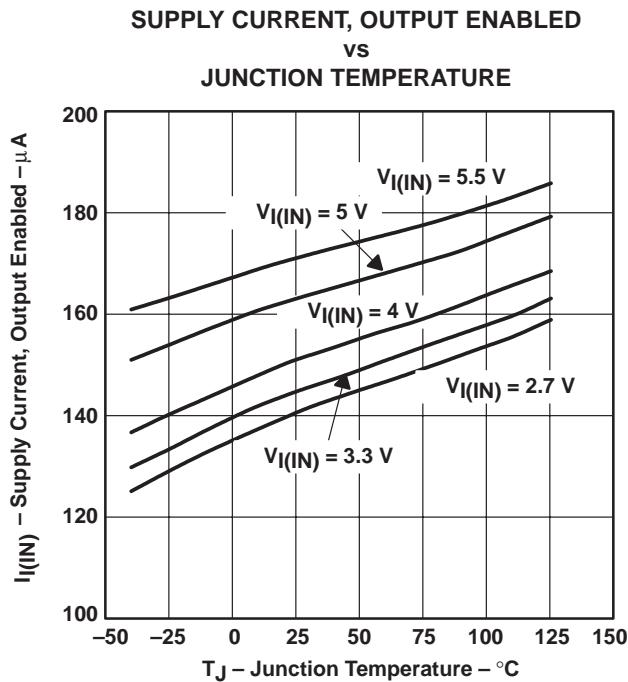


Figure 16

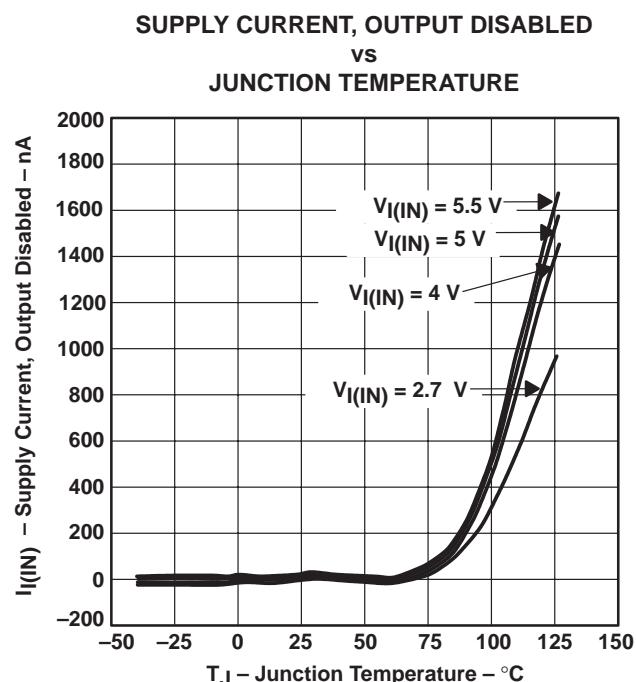


Figure 17

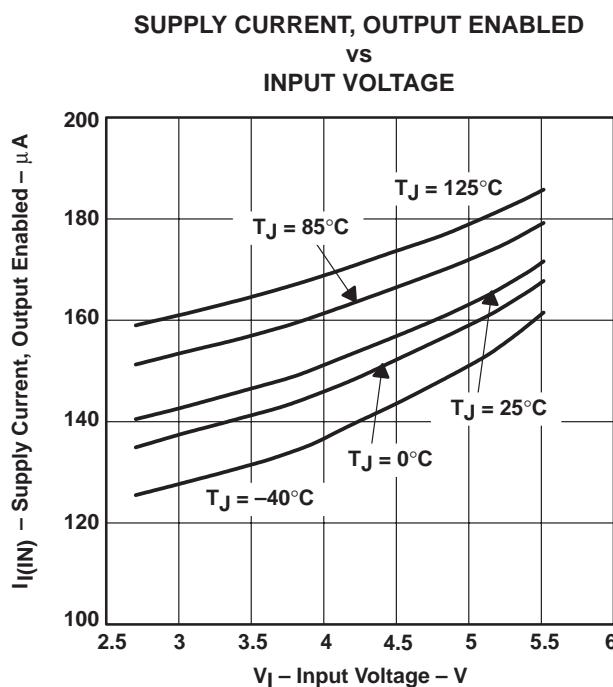


Figure 18

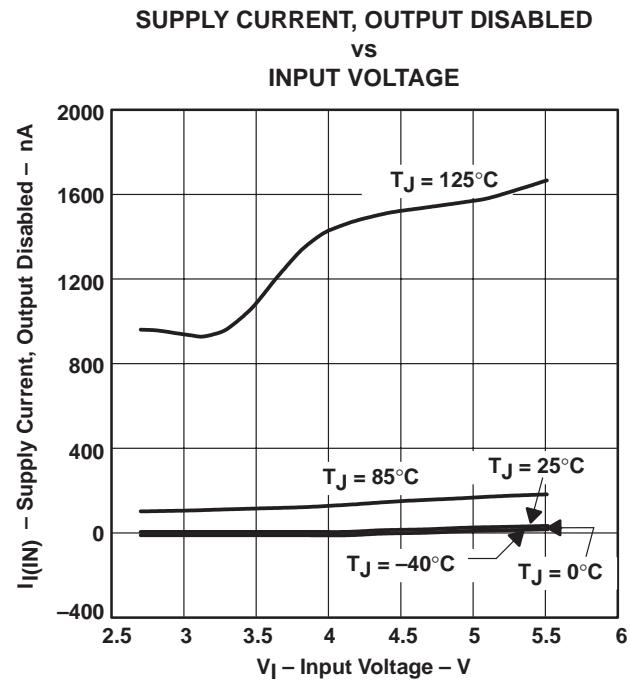


Figure 19

TPS2046, TPS2056 DUAL CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES

SLVS183 – APRIL 1999

TYPICAL CHARACTERISTICS

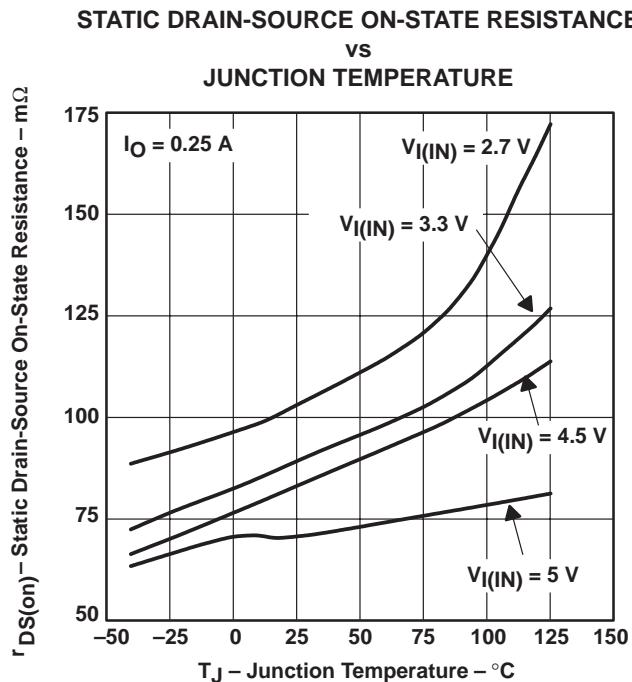


Figure 20

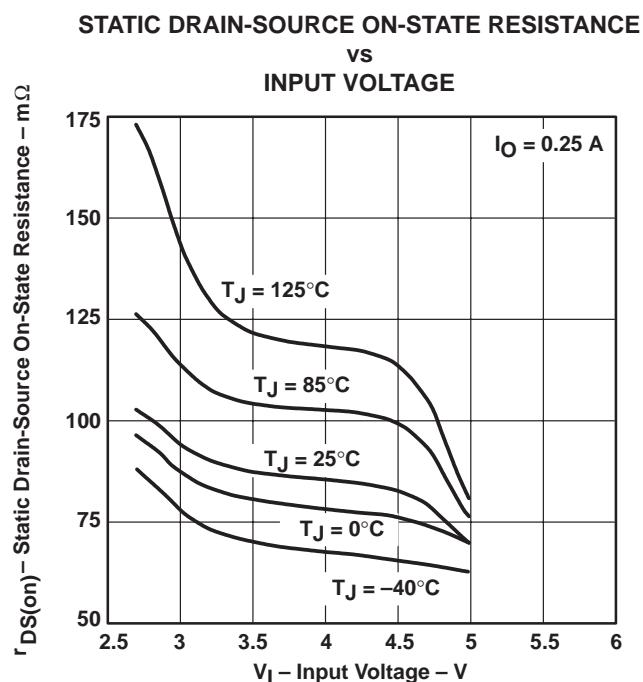


Figure 21

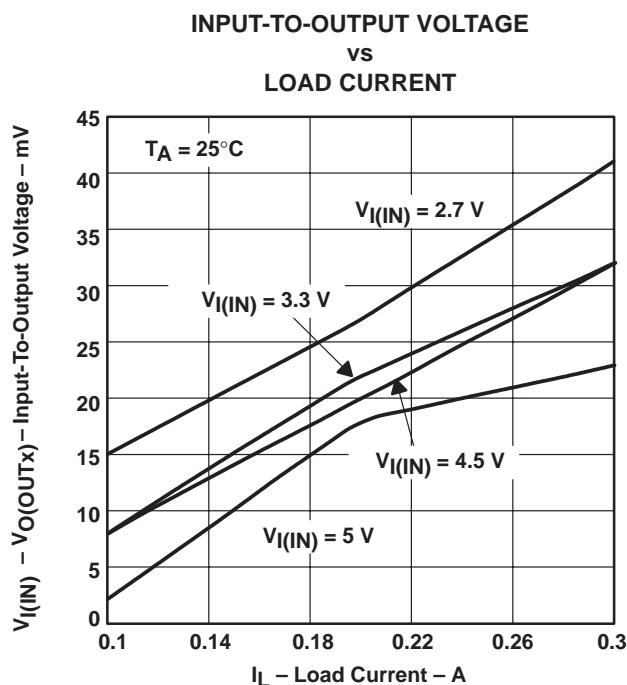


Figure 22

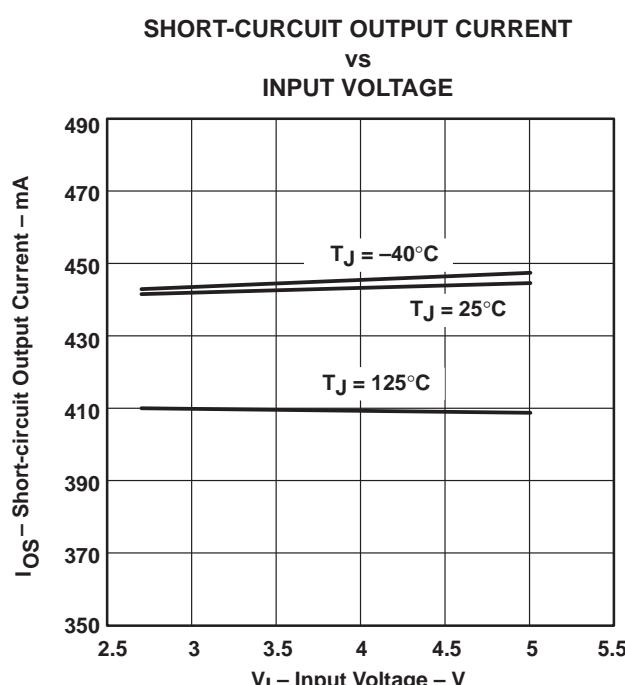
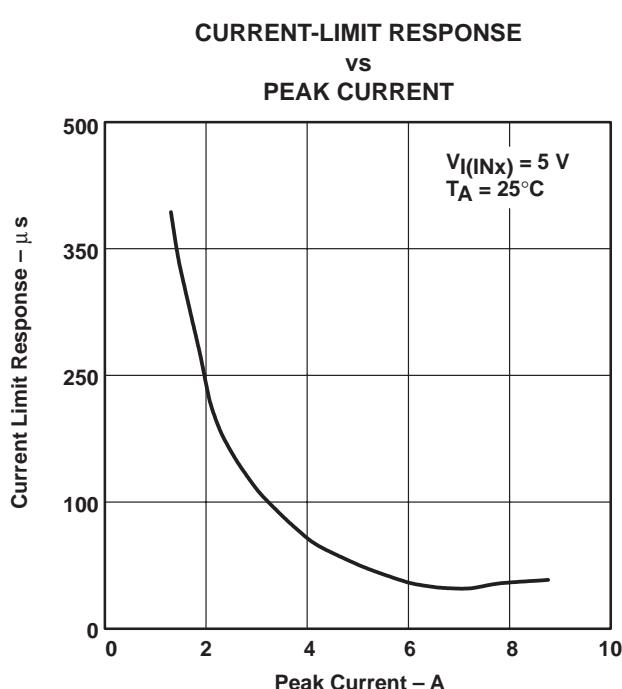
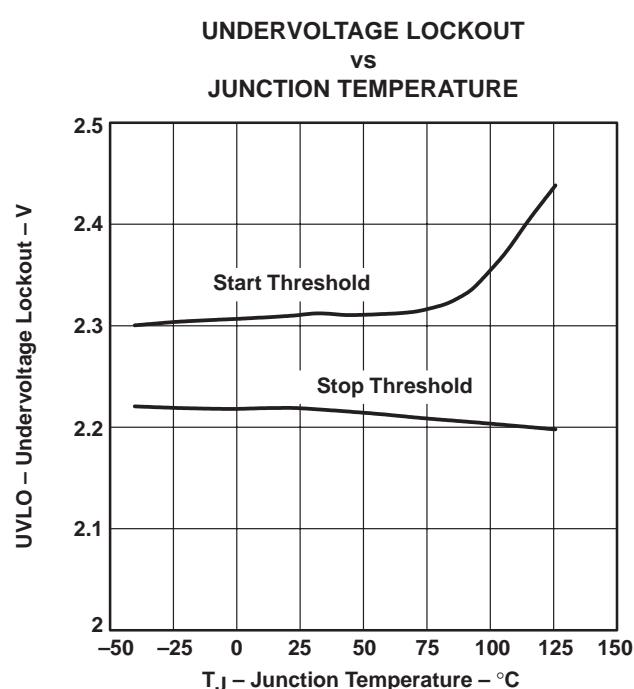
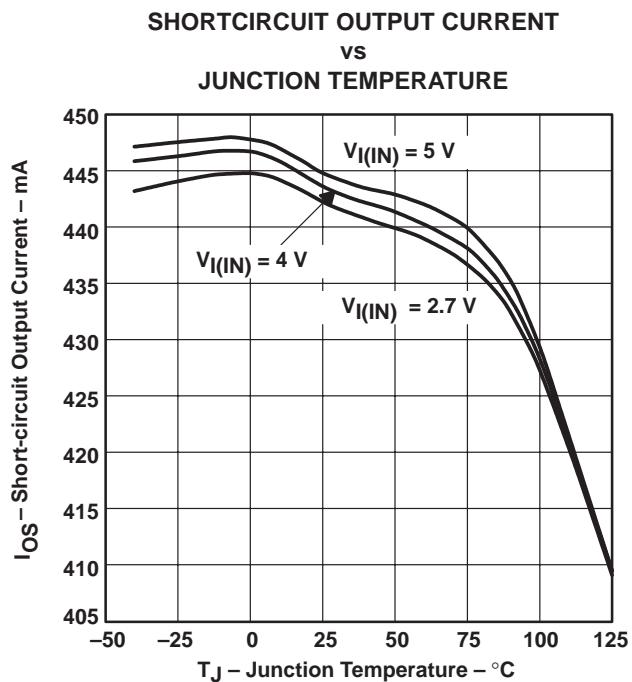
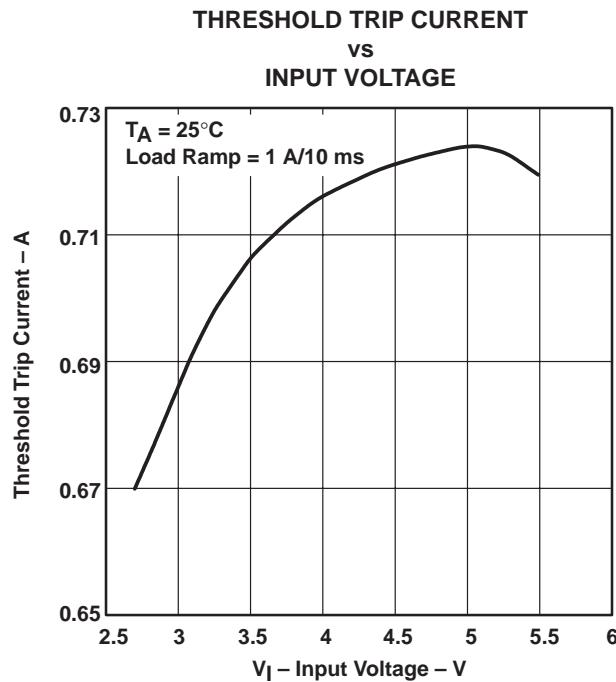


Figure 23

TYPICAL CHARACTERISTICS



TPS2046, TPS2056 DUAL CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES

SLVS183 – APRIL 1999

TYPICAL CHARACTERISTICS

OVERCURRENT (OCx) RESPONSE TIME VS PEAK CURRENT

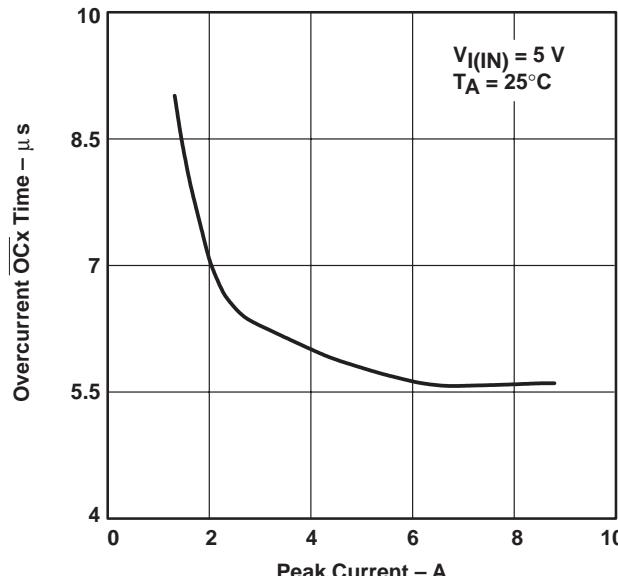


Figure 28

APPLICATION INFORMATION

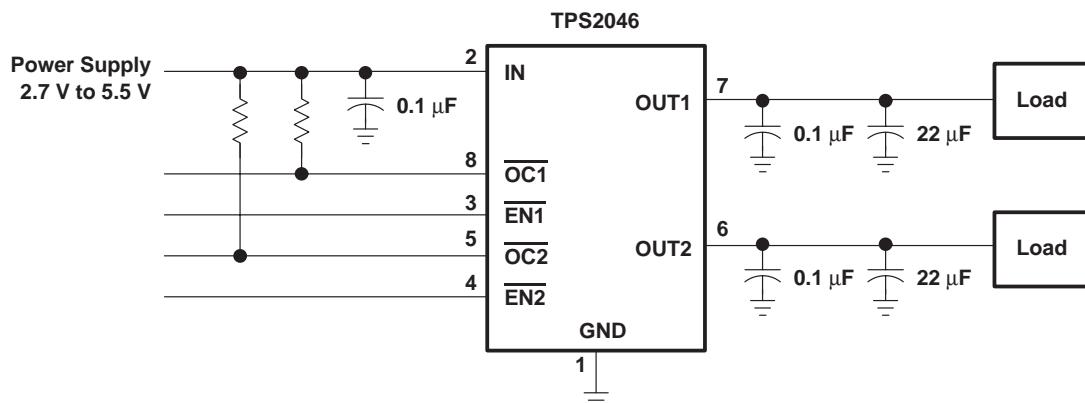


Figure 29. Typical Application

power-supply considerations

A 0.01- μ F to 0.1- μ F ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01- μ F to 0.1- μ F ceramic capacitor improves the immunity of the device to short-circuit transients.

APPLICATION INFORMATION

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS2046 and TPS2056 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS2046 and TPS2056 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

OCx response

The \overline{OCx} open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter (see Figure 30) can be connected to the \overline{OCx} pin to reduce false overcurrent reporting caused by hot-plug switching events or extremely high capacitive loads. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

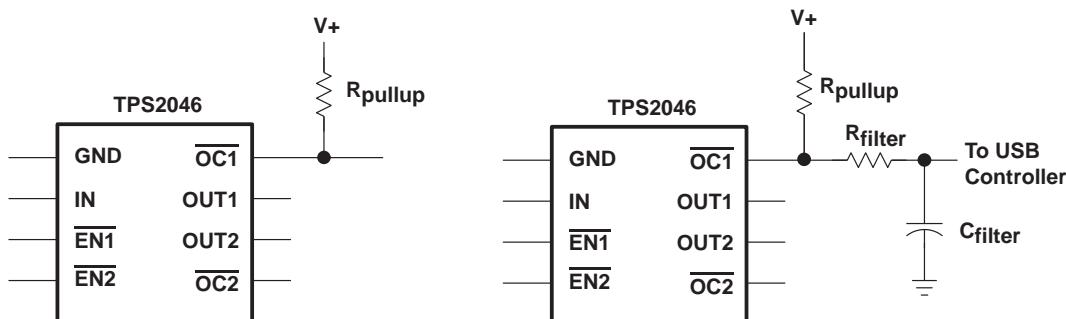


Figure 30. Typical Circuits for \overline{OC} Pin and RC Filter for Damping Inrush \overline{OC} Responses

TPS2046, TPS2056 DUAL CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES

SLVS183 – APRIL 1999

APPLICATION INFORMATION

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 21. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C

$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2046 and TPS2056 into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2046 and TPS2056 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature will rise. Once the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of 140°C and reach 160°C, both switches turn off. The \overline{OC} open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on with a controlled rise time to reduce EMI and voltage overshoots.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION

Universal Serial Bus (USB) applications

The Universal Serial Bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS2046 and TPS2056 can provide power-distribution solutions for many of these classes of devices.

bus-powered hubs

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

low-power bus-powered functions and high-power bus-powered functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA, and high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of $44\ \Omega$ and $10\ \mu\text{F}$ at power up, the device must implement inrush current limiting (see Figure 31).

TPS2046, TPS2056 DUAL CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES

SLVS183 – APRIL 1999

APPLICATION INFORMATION

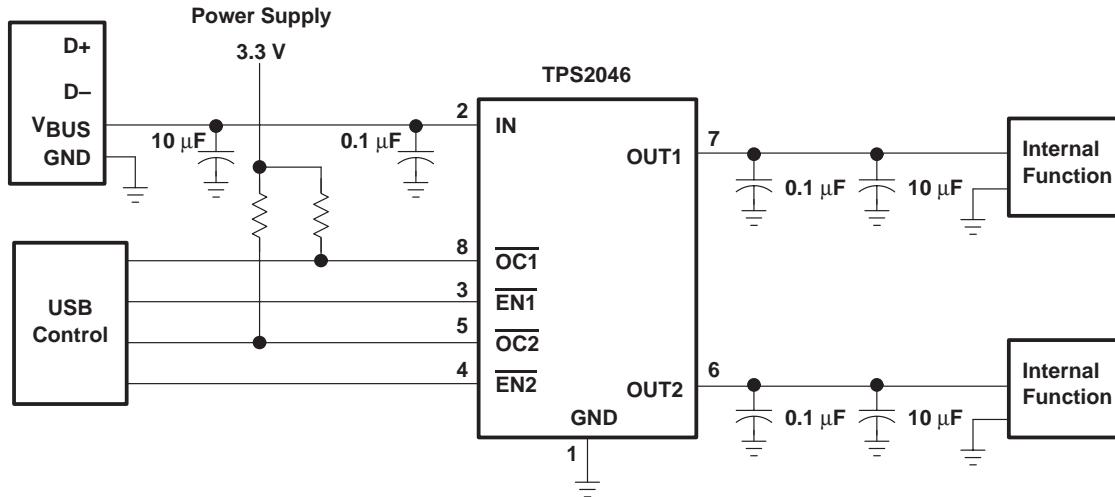


Figure 31. High-Power Bus-Powered Function

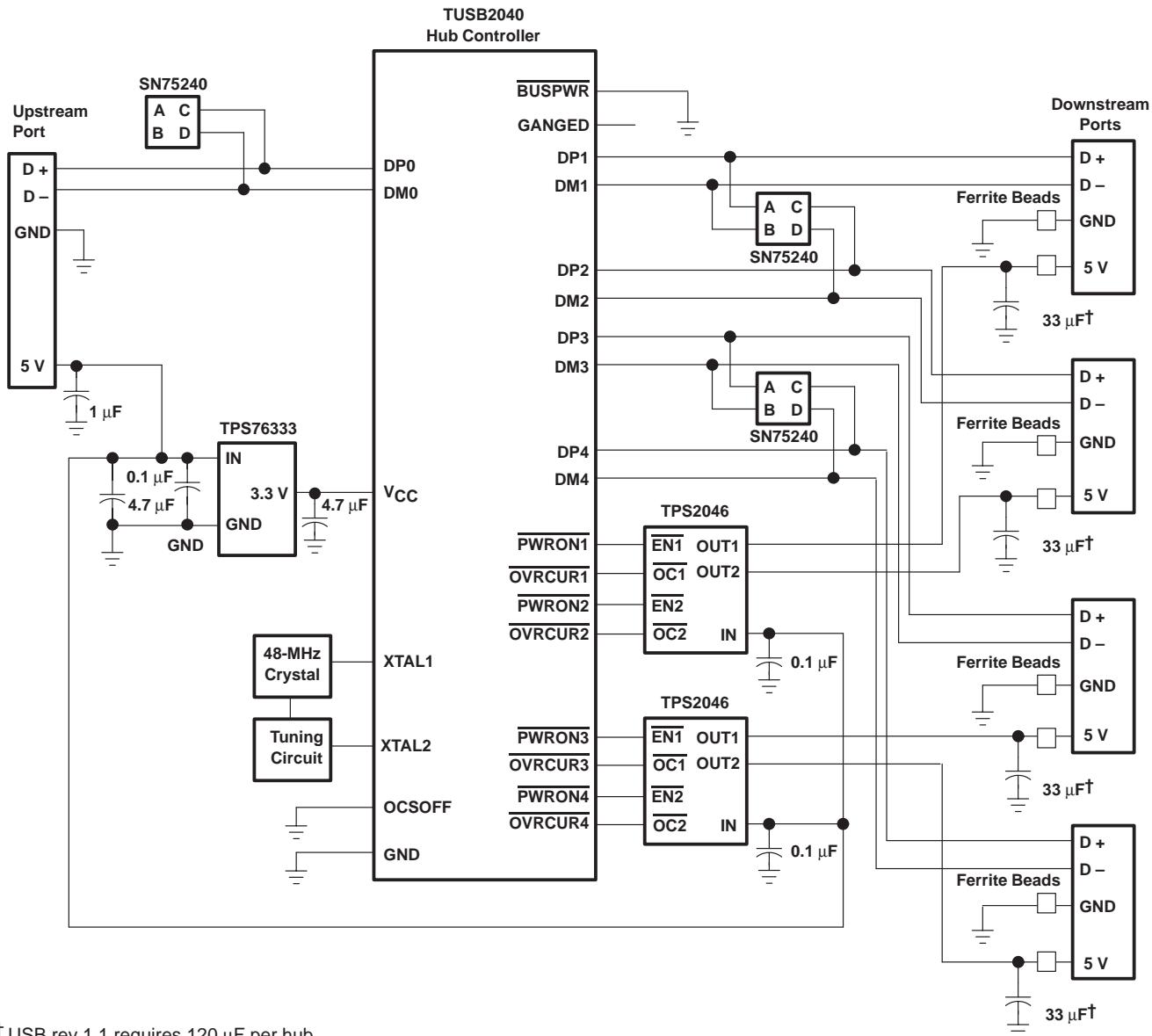
USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power distribution features must be implemented.

- Bus-Powered Hubs must:
 - Enable/disable power to downstream ports
 - Power up at <100 mA
 - Limit inrush current (<44 Ω and 10 μ F)
- Functions must:
 - Limit inrush currents
 - Power up at <100 mA

The feature set of the TPS2046 and TPS2056 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-power hubs, as well as the input ports for bus-power functions (see Figure 32).

APPLICATION INFORMATION



[†] USB rev 1.1 requires 120 μ F per hub.

Figure 32. Bus-Powered Hub Implementation

APPLICATION INFORMATION

generic hot-plug applications (see Figure 33)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2046 and TPS2056, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2046 and TPS2056 also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

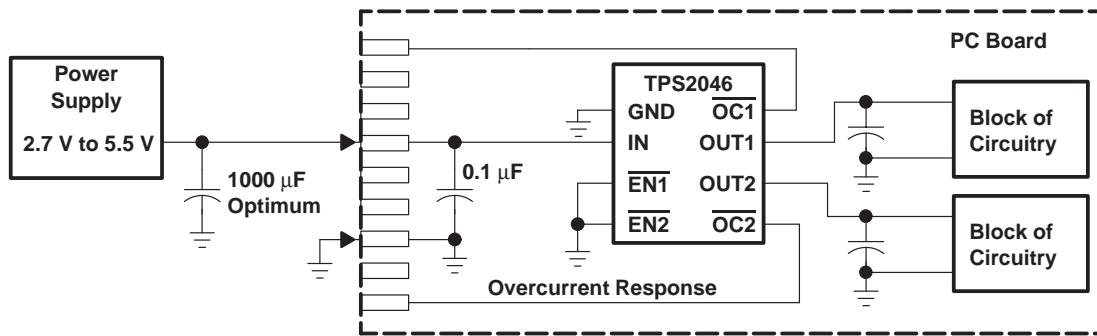


Figure 33. Typical Hot-Plug Implementation

By placing the TPS2046 and TPS2056 between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2046D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2046	
TPS2046DR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2046	
TPS2046P	NRND	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TPS2046P	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and



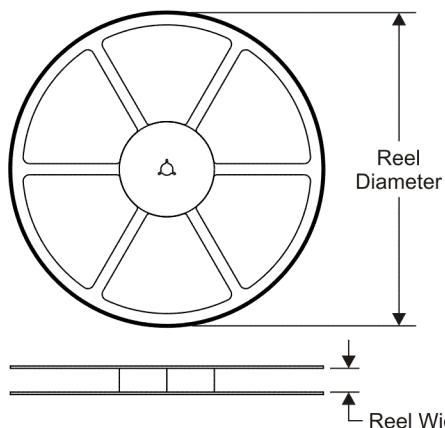
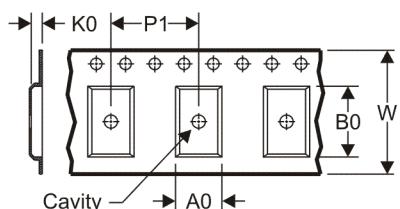
www.ti.com

PACKAGE OPTION ADDENDUM

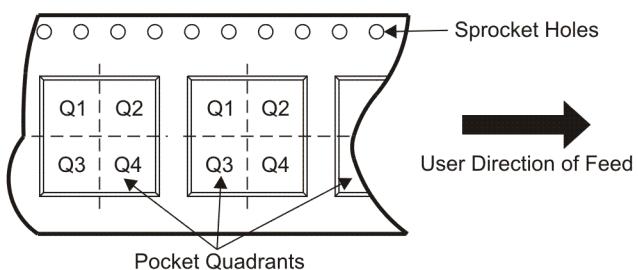
2-Oct-2014

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

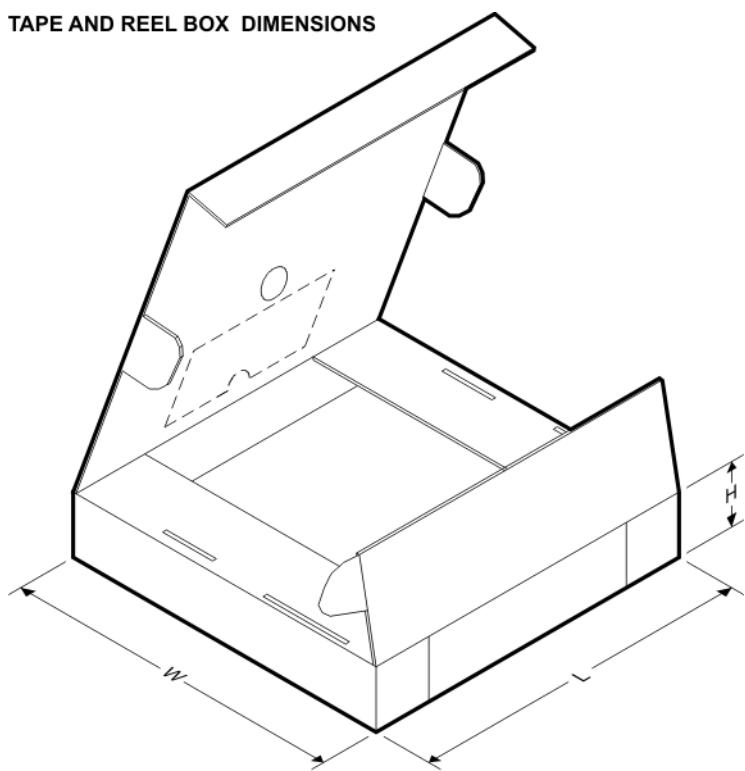
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2046DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2046DR	SOIC	D	8	2500	340.5	338.1	20.6

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications
Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity
	TI E2E Community
	e2e.ti.com