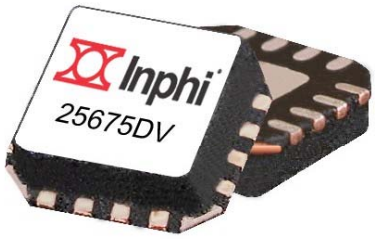
25675DV-QFN
DC to 25 GHz Divide-by-4 Prescaler in QFN Plastic Package
Data Sheet



Applications

- Phase-locked loop (PLL) applications from DC to 25 GHz
- Point-to-point and point-to-multipoint digital radios
- Broadband test and measurement equipment

Features

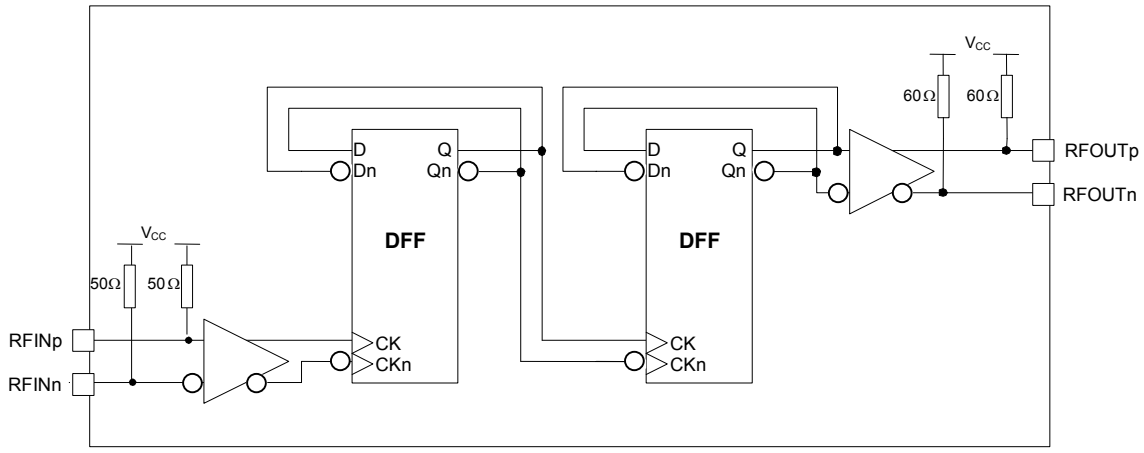
- Ultra Low SSB Phase Noise
- Wide frequency range: DC to 25 GHz
- High input power sensitivity: –20 dBm typical
- Supports single-ended and differential operation
- Low supply current: 84 mA typical
- Single +3.0 to +3.5 V power supply
- Available in QFN plastic package
- Evaluation board available

Description

The 25675DV divide-by-4 prescaler is designed for a wide range of communications and broadband test and measurement applications from DC to 25 GHz. It is typically used in high-frequency phase-locked loop (PLL) oscillator and signal-path down conversion circuits.

The 25675DV operates from a single +3.0 to +3.5 V power supply and is available in a 3 x 3 mm quad flat no lead (QFN) plastic package. The packaged parts are also available on an evaluation board.

Block Diagram



Absolute Maximum Ratings

- Stresses beyond those listed here may cause permanent damage to the device.
- These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the "Operating Conditions" and "Electrical Specifications" of this datasheet is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Conditions	Min	Max	Unit
Power Supply Voltage	V_{CC}		–0.5	+3.6	V
CW RF Input Power	P_{IN} (CW)		---	+5	dBm
DC Input Voltage	V_{RFIN}		V_{CC}-2	V_{CC}+0.6	V
DC Output Voltage	V_{RFOUT}		V_{CC}-1.5	V_{CC}+1.0	V
Junction Temperature – Die	T_J		–40	+175	°C
Case Temperature – Packaged	T_C		–55	+125	°C
Shipping/Storage Temperature	T_{STORE}		–65	+125	°C
Humidity	RH		0	100	%

Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}		+3.0	+3.3	+3.5	V
Supply Current	I_{CC}		---	84	105	mA
Operating Temperature (Junction)	T_J		–20	---	+125	°C
Operating Temperature (Case)	T_C		–40	---	+85	°C
Thermal Resistance	R_{JC}		---	---	54	°C/W

Electrical Specifications

WARNING – To prevent damage to the part:
- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions.						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Max Input Frequency	F_{IN} (max)		25	26	---	GHz
Min Input Frequency[1]	F_{IN} (min)		---	0.5	1.0	GHz
Input Return Loss	RL_{IN}	< 25 GHz, $V_{CMIN} \leq V_{CC}$	10	---	---	dB
		< 25 GHz, $V_{CMIN} > V_{CC}$	6	---	---	dB
Input Power Range[2]	P_{IN}	1 – 4 GHz (sine wave) Single ended, AC coupled	–4	> –10	4	dBm
		4 – 8 GHz (sine wave) Single ended, AC coupled	–10	> –20	4	dBm
		8 – 20 GHz (sine wave) Single ended, AC coupled	–16	> –25	4	dBm
		20 – 24 GHz (sine wave) Single ended, AC coupled	–8	> –15	4	dBm
Output Return Loss	RL_{OUT}	< 13 GHz	10	---	---	dB
Output Power	P_{OUT}	Single ended, AC coupled, F_{IN} = 24 GHz	–3	0	3	dBm
Reverse Leakage (output power appearing at input ports)	$P_{LEAKAGE}$	Both RF outputs terminated (For F_{IN} = 12.5 to 25 GHz)	---	–60	---	dBm
		One RF output terminated	---	–42	---	
Harmonics	$2F_{OUT}$	P_{IN} = 0 dBm, F_{IN} = 24 GHz	---	–32	---	dBc
	$3F_{OUT}$	P_{IN} = 0 dBm, F_{IN} = 24 GHz	---	–16	---	dBc
Jitter rms		F_{IN} = 24 GHz	---	0.9	---	ps
Output Rise/Fall Time	t_r/t_f	20% – 80%, F_{IN} = 25 GHz	---	18	---	ps
SSB Phase Noise @ 100 kHz offset	Φ	F_{IN} = 25 GHz	---	-149	---	dBc/Hz
Spurious Output Power[3]		All input frequencies	---	---	none	dBc

Notes:
[1] For sine wave input signal. Prescaler will operate down to DC with a square wave signal.
[2] For digital square wave inputs, the minimum input amplitude should be 300 mVpp (differential or single-ended) over the frequency range of DC to 25 GHz. Note: The minimum slew rate needs to be 1V/ns.
[3] The Spurious Output Power measured was too low to be statistically significant.

Typical Operating Characteristics

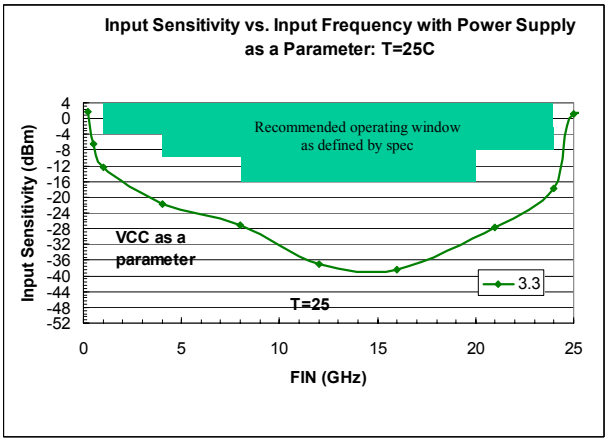


Figure 1. Input sensitivity over input frequency for Vcc = 3.3V at an ambient temperature of 25 C

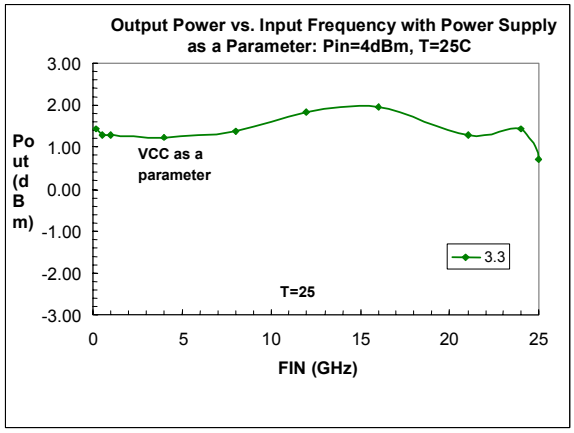


Figure 2. Output power (single-ended) versus input frequency for Vcc = 3.3V and Pin = 4 dBm at 25 C

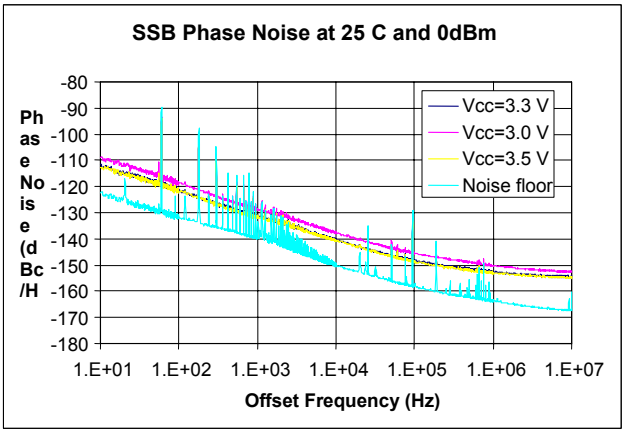


Figure 3. SSB phase noise for Fin = 25 GHz and Pin = 0 dBm at 25 C over supply voltage

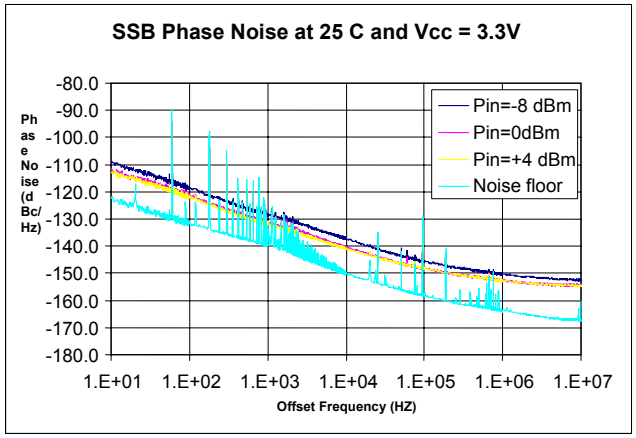


Figure 4. SSB phase noise for Fin = 25 GHz and Vcc = 3.3V at 25 C over input power

Typical Operating Characteristics (cont'd.)

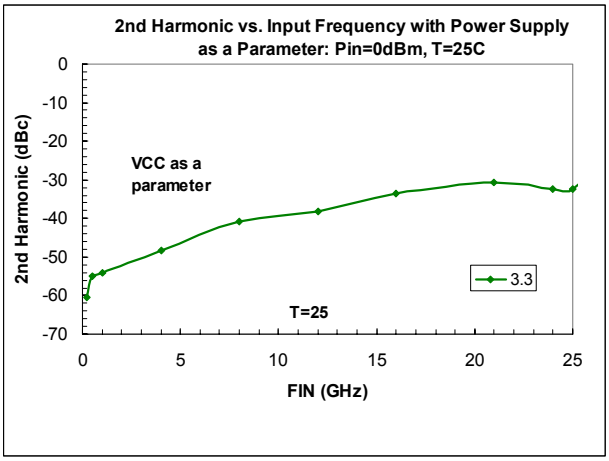


Figure 5. Second harmonic power versus input frequency at Vcc = 3.3V, Pin = 0 dBm at 25 C

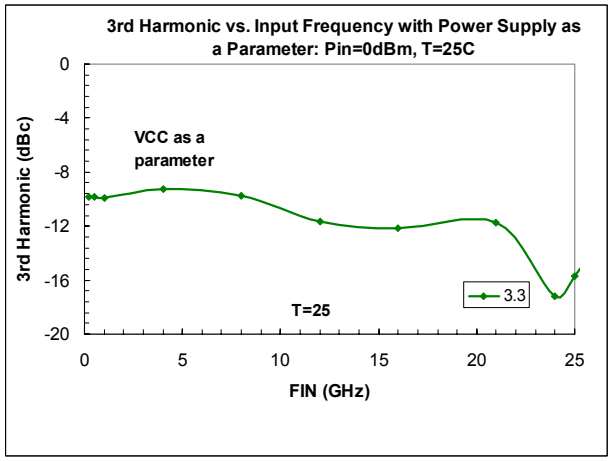


Figure 6. Third harmonic power versus input frequency at Vcc = 3.3V, Pin = 0 dBm at 25 C

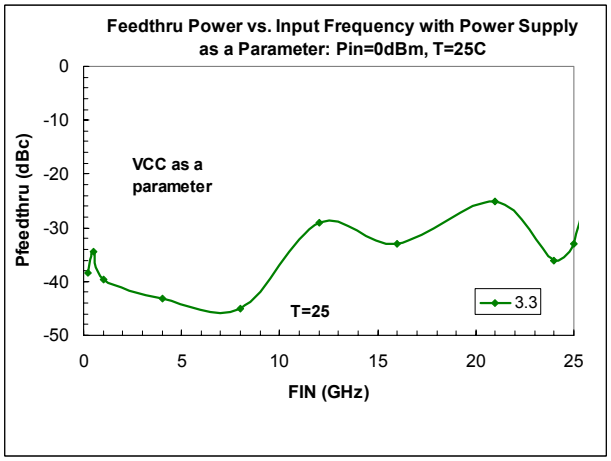


Figure 7. Feedthru power vs. Input Frequency at Vcc = 3.3 V, Pin = 0 dBm at 25 °C

Typical Time Domain Operating Characteristics

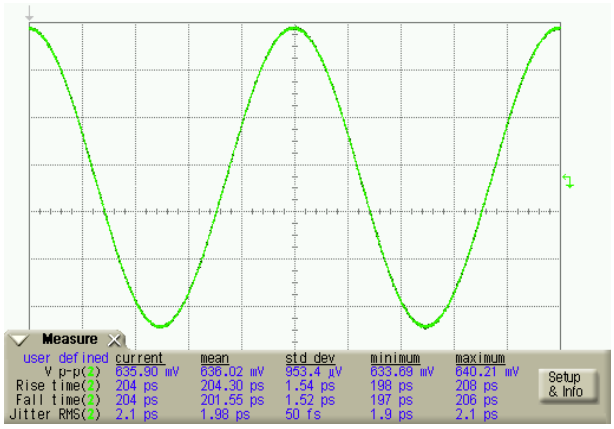


Figure 8. Input waveform, AC-coupled, for F_{IN} = 1 GHz and P_{IN} = 0 dBm; 200 ps/div, 100mV/div, T=25° C

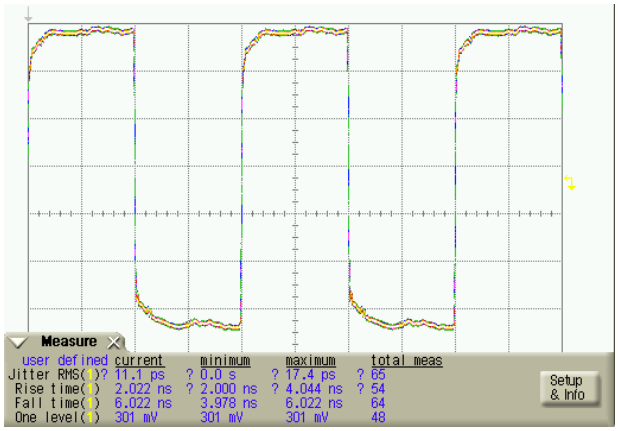


Figure 9. Output waveform, AC-coupled, for F_{IN} = 1 GHz and P_{IN} = 0 dBm; 1 ns/div, 100 mV/div, T=25° C; and Vcc=3.3 V

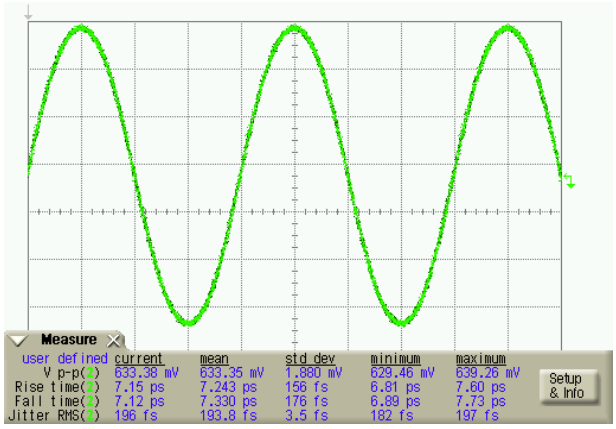


Figure 10. Input waveform, AC-coupled, for F_{IN} = 25 GHz and P_{IN} = 0 dBm; 10 ps/div, 100mV/div, T=25° C

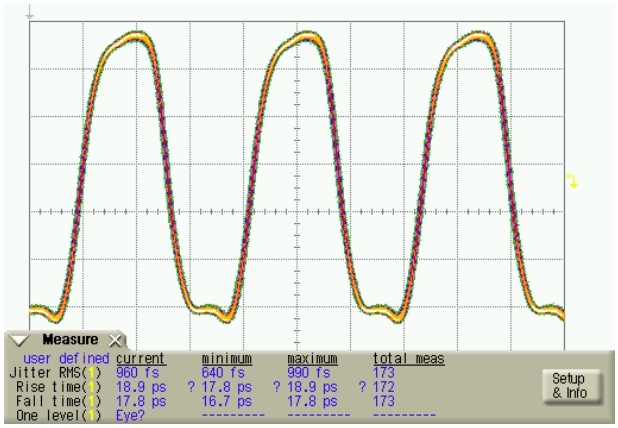


Figure 11. Output waveform, AC-coupled, for F_{IN} = 25 GHz and P_{IN} = 0 dBm; 50 ps/div, 100mV/div, T = 25° C; Vcc = 3.3 V

Application Notes

AC/DC Coupling and Termination

In a typical application, the RF inputs and outputs should be AC coupled via DC blocking capacitors mounted on a substrate or circuit board at each RF port. All unused RF outputs should be terminated with DC blocking capacitors and 50 Ω resistors to V_{CC} or ground for optimum performance. Unused RF output ports may be left open, but this configuration will result in additional power leakage from one RF port to the other.

All unused RF inputs should be terminated with DC blocking capacitors and 50 Ω resistors to Vcc or ground for optimum performance. Unused RF input ports may be left open, but this configuration will result in additional power leakage from one RF port to the other. The improvement from adding the 50 Ω terminations is small, and may not be noticeable in all cases. It may be possible to omit the termination if the part meets all the customer requirements without it.

In applications where the use of DC blocking capacitors is not desirable, the part may be directly DC coupled at the RF inputs and outputs. However, care must be taken to ascertain that the DC voltages at all RF input and output ports stay within the specified limits (see Absolute Maximum Ratings on p. 2). All unused RF inputs and outputs should be terminated with 50 Ω resistors to V_{CC} (not ground) for optimum performance. Damage to the part may occur if the unused RF inputs and outputs are terminated directly to ground without the use of the DC blocking capacitors.

Single-Ended Operation

The 25675DV is designed for either single-ended or differential operation. For single-ended operation, the unused RF input and output should be terminated in the manner described above.

Input DC Offset

Under certain conditions, the 25675DV may self oscillate under no RF input power. This self-oscillation will produce an undesired output signal commonly referred to as "false trigger." To prevent false trigger, a small DC offset voltage between 20 mV and 100 mV may be applied between the RF input ports. Since the input has an internal 50 Ω resistor to V_{CC} (nominally +3.3 V), adding a 10 kΩ resistor between the unused RF input and ground will result in an offset voltage of around 16.5 mV between the RF inputs and prevent the false trigger.

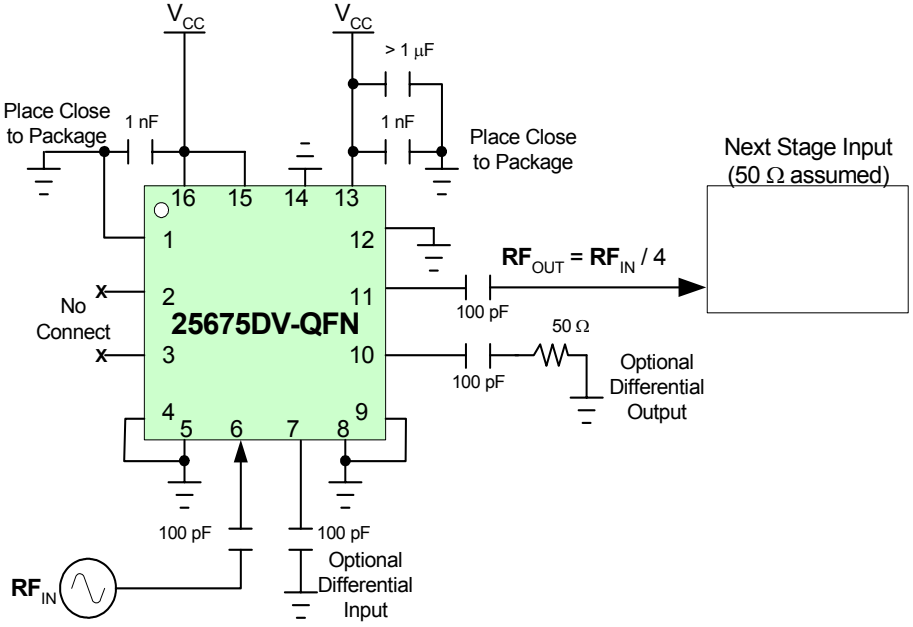
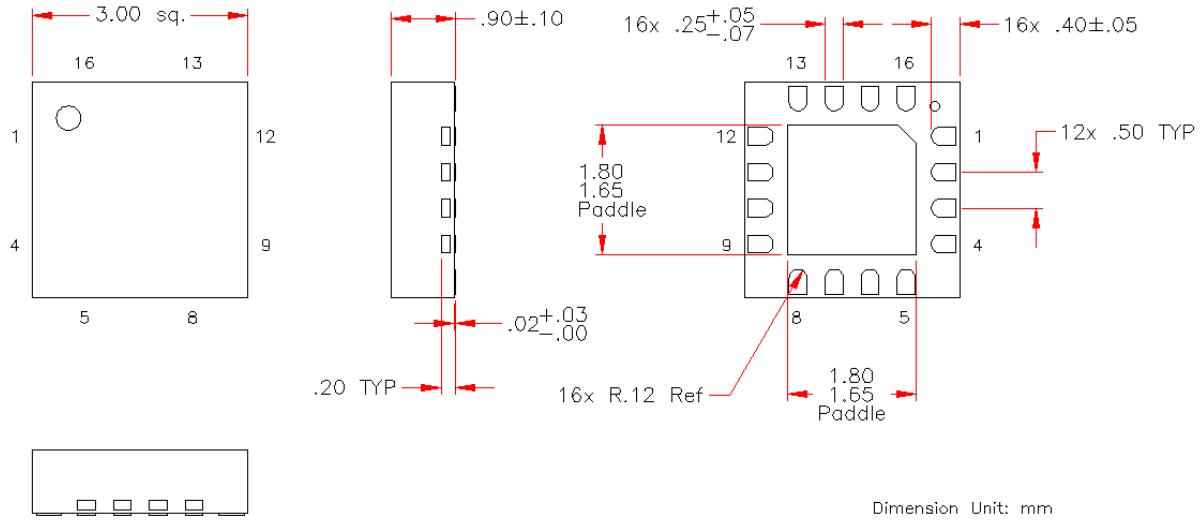


Figure 12. 25675DV-QFN suggested circuit configuration

QFN Package Outline Drawing



Name	Pin	Description	Function
RFINp	6	RF Non-inverting Input	Input
RFINn	7	RF Inverting Input	Input
RFOUTp	11	RF Non-inverting Output	Output
RFOUTn	10	RF Inverting Output	Output
GND	1, 4, 5, 8, 9, 12, 14, Paddle	Ground	Supply
V_{CC}	13, 15, 16	Power Supply: Connect to +3.0 to 3.4V Supply	Supply
NC	2, 3	Not Connected	NC

NOTE: DC blocking capacitors are required at RF input and RF output ports for AC coupling.

Order Information

Part No.	Description
25675DV-S03QFN	DC to 25 GHz Divide-by-4 Prescaler Quad Flat No Lead Plastic Package
25675DV-S03QFNEVB	DC to 25 GHz Divide-by-4 Prescaler in Quad Flat No Lead Plastic Package on an Evaluation Board with SMA Connectors

Related Products

Part No.	Description
25675DV-S03D	DC to 25 GHz Divide-by-4 Prescaler – Die
25675DV-S03L	DC to 25 GHz Divide-by-4 Prescaler in LGA Ceramic Package
25675DV-S03LEVB	DC to 25 GHz Divide-by-4 Prescaler in LGA Ceramic Package on an Evaluation Board with SMA Connectors

Contact Information

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Qualification Notification

The 25675DV is fully qualified. Please contact Inphi for the qualification report.

Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi's Standard Customer Purchase Order Terms and Conditions.

Version Updates

From Version 1.4 to 1.3 (dated 02/08/06)

1. Changed Part number from 25675DV-S02 to 25675DV-S03 throughout datasheet.
2. Changes in "Features" section (page 1):
    a. Added "Ultra Low SSB Phase Noise".
    b. Power supply current changed from 68 mA to 84 mA typical.
3. Changes to Block Diagram: removed the approximate symbols (~) from the output termination resistors.
4. Added the three comments on Absolute Maximum Ratings (at top of table on page 2.)
5. Changes to Operating Conditions (page 2):
    a. Power Supply Voltage maximum spec. = +3.5V from +3.4V.
    b. Power Supply Current spec.: typical from 68 mA to 84 mA.
6. Changes to Electrical Specification (page 3):
    a. Added Input Return Loss specifications.
    b. Added Output Return Loss specifications.
    c. Added maximum Output Power spec. = +3 dBm.
    d. Changed Feedthru Power from –30 dBc to –36 dBc.
    e. Changed 2Fout Harmonic typical spec from –26 dBc to –32 dBc.
    f. Changed 3Fout Harmonic typical spec from –15 dBc to –16 dBc.
    g. Added Spurious Output Power spec. maximum = none.
7. Replaced figures 1 through 10 in the Typical Operating Characteristics section (pages 4 & 5).
8. Changed Qualification Notification section to Limited Qualification Notification and changed statement from fully qualified (25675DV-S02) to not yet fully qualified (page 8).

From Version 2.0 to 2.1 (dated 2007-05-24):

1. Updated Electrical Specifications Table (page 3):
    a. Added 2nd condition for Input Return Loss
        i. Condition = "< 25 GHz, $V_{CMIN} > V_{CC}$"
        ii. Min = 6 dB
    b. For Reverse Leakage condition, added note: "(for F_{IN} = 12.5 to 25 GHz)" when both RF outputs are terminated.
    c. Removed Feedthru Power parameter.
    d. Updated footnotes
        i. Added footnote #2, for Input Power Range (P_{IN}), the minimum input amplitude and slew rate needed for digital square wave inputs.
        ii. Added footnote #3 for Spurious Output parameter.
2. Updated Typical Operating Characteristics (pages 4 – 5):
    a. Added Figure 7, Feedthru Power plot.
3. Updated Application Notes section to add information about optional 50 Ω resistors on unused RF inputs (page 7).
4. Added caption for Figure 12, suggested circuit configuration (page 7).
5. Updated Qualification Notification status to indicate that this product is fully qualified (page 9).