1165898

Switchmode™ series NPN silicon power transistors.
The 2N6547 transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volts line operated switch-mode applications.

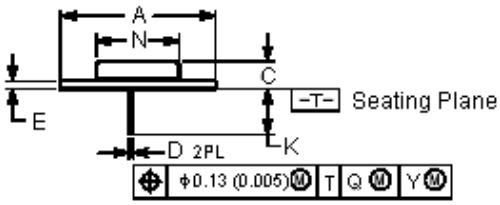
Features:

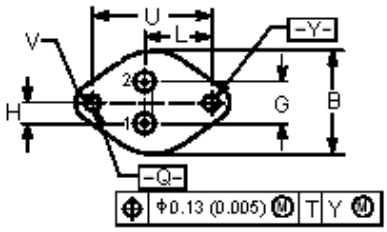
- High temperature performance specified for:
  - Reversed biased SOA with inductive loads.
  - Switching time with inductive loads.
  - Saturation voltages.
  - Leakage currents.

Applications:

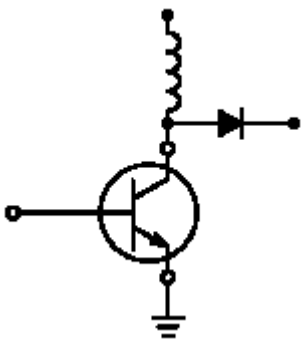
Switching regulators.
PWM inverters and motor controls.
Solenoid and relay drivers.
Deflection circuits.

TO-204 (TO-3)





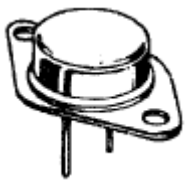
Style 1:
Pin 1. Base
2. Emitter
Collector (Case)



Dimensions	Minimum	Maximum
A	1.550 (39.37) Reference	
B	-	1.050 (26.67)
C	0.250 (6.35)	0.335 (8.51)
D	0.038 (0.97)	0.043 (1.09)
E	0.055 (1.40)	0.070 (1.77)
G	0.430 (10.92) BSC	
H	0.215 (5.46) BSC	
K	0.440 (11.18)	0.480 (12.19)
L	0.665 (16.89) BSC	
N	-	0.830 (21.08)
Q	0.151 (3.84)	0.165 (4.19)
U	1.187 (30.15) BSC	
V	0.131 (3.33)	0.188 (4.77)

Dimensions : Inches (Millimetres)

15 Ampere
NPN Silicon
Power Transistors
300 and 400 Volts
175 Watts



TO-3
Case 1-07

Maximum Ratings (1)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO\ (SUS)}$	400	V dc
Collector-Emitter Voltage	$V_{CEX\ (SUS)}$	450	
Collector-Emitter Voltage	V_{CEV}	850	
Emitter-Base Voltage	V_{EB}	9.0	
Collector Current - Continuous - Peak (2)	I_C I_{CM}	15 30	A dc
Base Current - Continuous - Peak (2)	I_B I_{BM}	10 20	
Emitter Current - Continuous - Peak (2)	I_E I_{EM}	25 35	
Total Power Dissipation at T_C = 25°C at T_C = 100°C Derate above 25°C	P_D	 175 100 1.0	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

Thermal Characteristics

Characteristics	Symbol	Maximum	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8 Inches from Case for 5 Seconds	T_L	275	°C

*Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Minimum	Maximum	Unit
Off Characteristics (1)				
Collector-Emitter Sustaining Voltage (I_C = 100mA, I_B = 0) **2N6547**	$V_{EO\ (sus)}$	400	-	V dc
Collector-Emitter Sustaining Voltage (I_C = 8A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) **2N6547**	$V_{CEX\ (sus)}$	450	-	
(I_C = 15A, V_{clamp} = Rated V_{CEO} = 100V, T_C = 100°C) **2N6547**		300		
Collector Cut off Current (V_{CEV} = Rated Value, $V_{BE\ (off)}$ = 1.5V dc) (V_{CEV} = Rated Value, $V_{BE\ (off)}$ = 1.5V dc, T_C = 100°C)	I_{CEV}	-	1.0 4.0	mA dc
Collector Cut off Current (V_{CE} = Rated V_{CEV}, R_{BE}, = 50Ω, T_C = 100°C)	I_{CER}	-	5.0	
Emitter Cut off Current (V_{EB} = 9.0V dc, I_C = 0)	I_{ERO}	-	1.0	

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Minimum	Maximum	Unit
Second Breakdown				
Second Breakdown Collector Current with Base Forward Biased t = 1.0s (Non-repetitive) (V_{CE} = 100V dc)	$I_{S/b}$	0.2	-	A dc
On Characteristic (1)				
DC Current Gain (I_C = 5.0A dc, V_{CE} = 2.0V dc) (I_C = 10A dc, V_{CE} = 2.0V dc)	h_{FE}	12 6.0	60 30	-
Collector-Emitter Saturation Voltage (I_C = 10A dc, I_B = 2.0A dc) (I_C = 15A dc, I_B = 3.0A dc) (I_C = 10A dc, I_B = 2.0A dc, T_C = 100°C)	$V_{CE\ (sat)}$	-	1.5 5.0 2.5	V dc
Base-Emitter Saturation Voltage (I_C = 10A dc, I_B = 2.0A dc) (I_C = 10A dc, I_B = 2.0A dc, T_C = 100°C	$V_{BE\ (sat)}$	-	1.6	
Dynamic Characteristics				
Current-Gain-Bandwidth Product (I_C = 500mA dc, V_{CE} = 10V dc, f_{test} = 1.0MHz)	f_T	6.0	28	MHz
Output Capacitance (V_{CB} = 10V dc, I_E = 0, f_{test} = 1.0MHz)	C_{ob}	125	500	pF

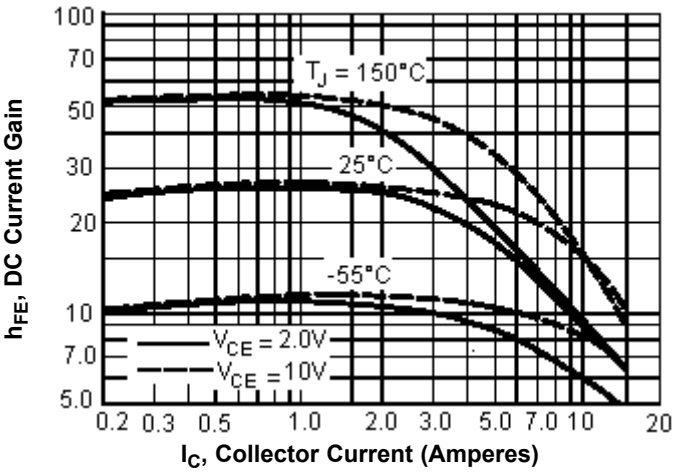
Switching Characteristics

Resistive Load					
Delay Time	(V_{CC} = 250V, I_C = 10A, I_{B1} = I_{B2} = 2.0A, t_p = 100µS, Duty Cycle ≤2.0%	t_d	-	0.05	µs
Rise Time		t_r	-	1.0	
Storage Time		t_s	-	4.0	
Fall Time		t_f	-	0.7	
Inductive Load, Clamped					
Storage Time	(I_C = 10A (pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0A, $V_{BE\ (off)}$ = 5.0V dc, T_C = 100°C)	t_s	-	5.0	µs
Fall Time		t_f	-	1.5	
Storage Time	(I_C = 10A (pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0A, $V_{BE\ (off)}$ = 5.0V dc, T_C = 25°C)	t_s	Typical 2.0		µs
Fall Time		t_f	Typical 0.09		

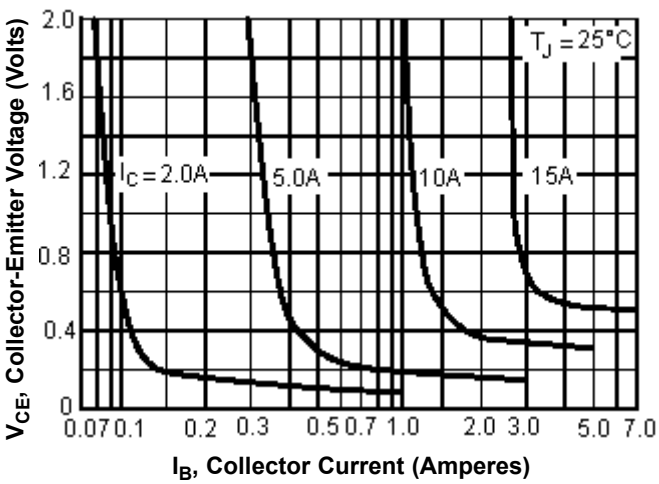
*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width = 300µs, Duty Cycle = 2%.

Typical Electrical Characteristics

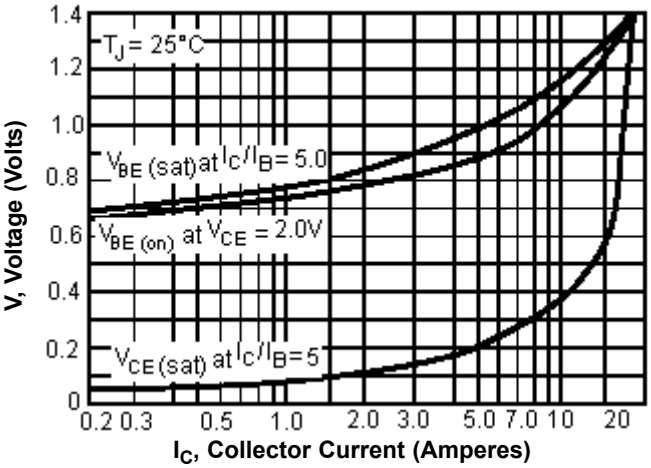
DC Current Gain



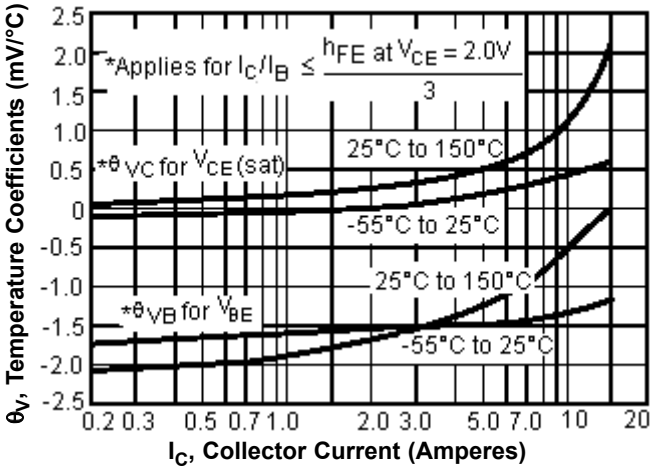
Collector Saturation Region



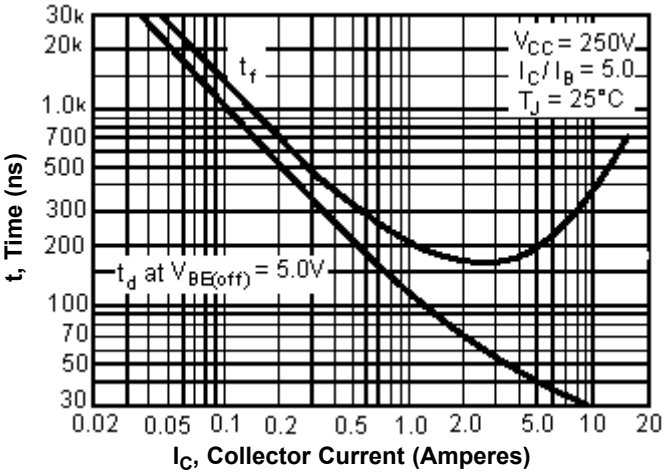
"On" Voltages



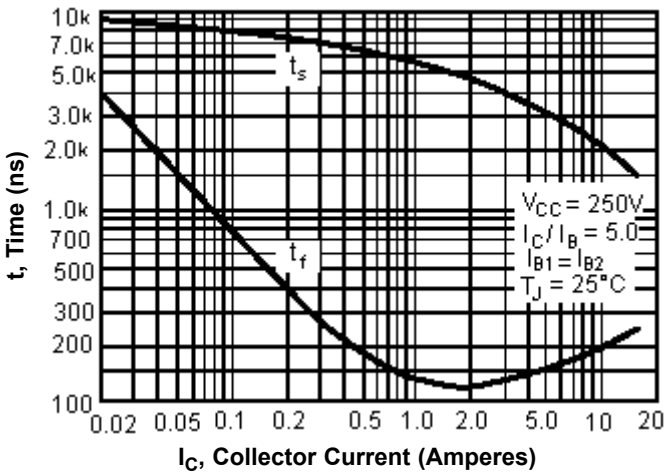
Temperature Coefficients



Turn-On Time

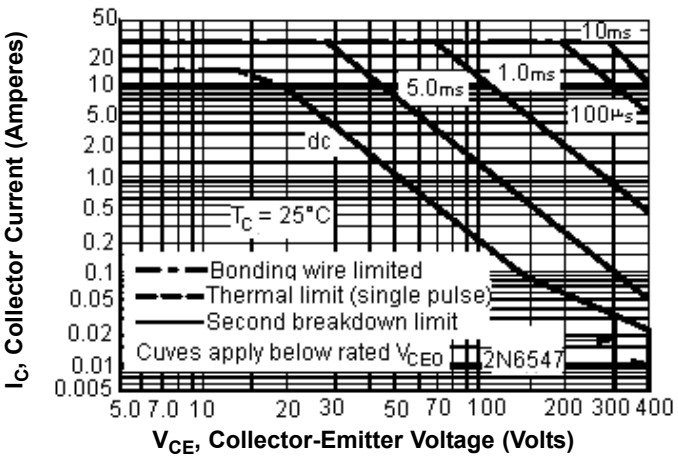


Turn-Off Time

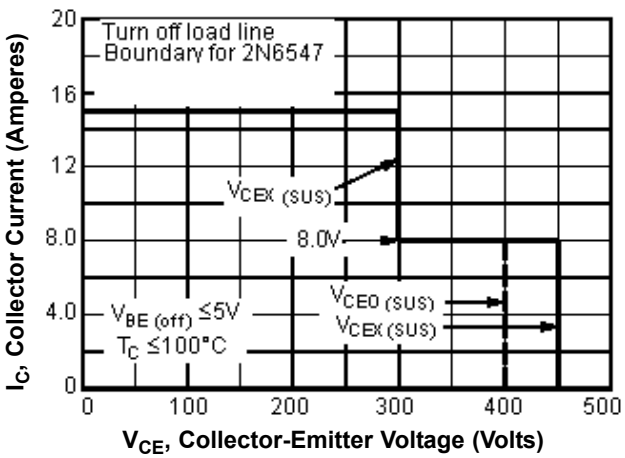


Maximum Rated Safe Operating Areas

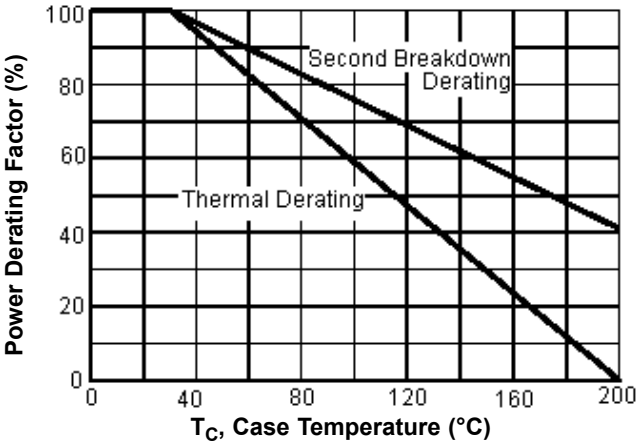
Forward Bias Safe Operating Area



Reverse Bias Safe Operating Area

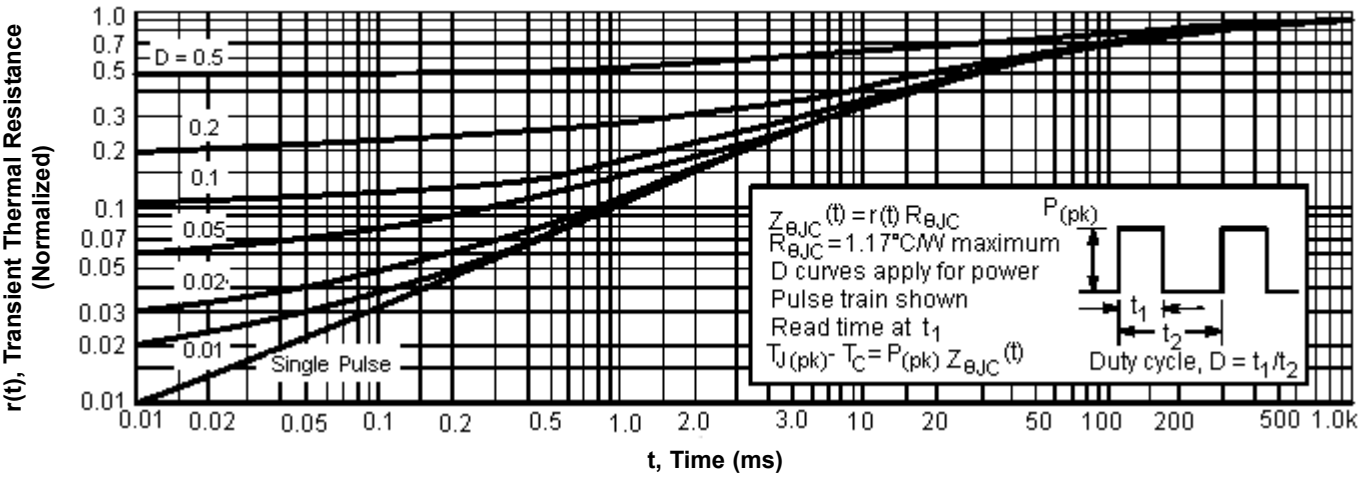


Power Derating



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown may be found at any case temperature by using the appropriate curve. $T_{J(pk)}$ may be calculated from the data. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Thermal Response



Part Number Table

Description	Part Number
Transistor, NPN, TO-3	2N6547

Disclaimer This data sheet and its contents (the "Information") belong to the Premier Farnell Group (the "Group") or are licensed to it. No licence is granted for the use of it other than for information purposes in connection with the products to which it relates. No licence of any intellectual property rights is granted. The Information is subject to change without notice and replaces all data sheets previously supplied. The Information supplied is believed to be accurate but the Group assumes no responsibility for its accuracy or completeness, any error in or omission from it or for any use made of it. Users of this data sheet should check for themselves the Information and the suitability of the products for their purpose and not make any assumptions based on information included or omitted. Liability for loss or damage resulting from any reliance on the Information or use of it (including liability resulting from negligence or where the Group was aware of the possibility of such loss or damage arising) is excluded. This will not operate to limit or restrict the Group's liability for death or personal injury resulting from its negligence. SPC Multicomp is the registered trademark of the Group. © Premier Farnell plc 2008.