

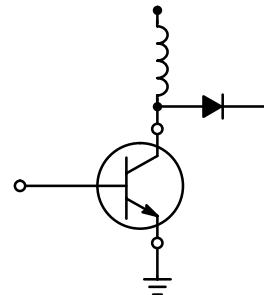
## SWITCHMODE™ Series NPN Silicon Power Transistors

The 2N6547 transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

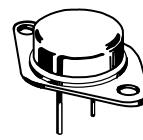
### Specification Features

- High Temperature Performance Specified for:
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



## 2N6547

15 AMPERE  
NPN SILICON  
POWER TRANSISTORS  
300 and 400 VOLTS  
175 WATTS



CASE 1-07  
TO-204AA  
(TO-3)

### MAXIMUM RATINGS (1)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	450	Vdc
Collector-Emitter Voltage	$V_{CEV}$	850	Vdc
Emitter Base Voltage	$V_{EB}$	9.0	Vdc
Collector Current — Continuous — Peak (2)	$I_C$ $I_{CM}$	15 30	Adc
Base Current — Continuous — Peak (2)	$I_B$ $I_{BM}$	10 20	Adc
Emitter Current — Continuous — Peak (2)	$I_E$ $I_{EM}$	25 35	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	175 100 1.0	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	275	$^\circ\text{C}$

# 2N6547

\*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS (1)</b>				
Collector-Emitter Sustaining Voltage ( $I_C = 100 \text{ mA}$ , $I_B = 0$ )	$V_{CEO(\text{sus})}$	300	—	Vdc
		400	—	
Collector-Emitter Sustaining Voltage ( $I_C = 8.0 \text{ A}$ , $V_{\text{clamp}} = \text{Rated } V_{CEX}$ , $T_C = 100^\circ\text{C}$ )	$V_{CEX(\text{sus})}$	350	—	Vdc
( $I_C = 15 \text{ A}$ , $V_{\text{clamp}} = \text{Rated } V_{CEO} = 100 \text{ V}$ , $T_C = 100^\circ\text{C}$ )		450	—	
Collector Cutoff Current ( $V_{CEV} = \text{Rated Value}$ , $V_{BE(\text{off})} = 1.5 \text{ Vdc}$ ) ( $V_{CEV} = \text{Rated Value}$ , $V_{BE(\text{off})} = 1.5 \text{ Vdc}$ , $T_C = 100^\circ\text{C}$ )	$I_{CEV}$	—	1.0	mAdc
		—	4.0	
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEV}$ , $R_{BE} = 50 \Omega$ , $T_C = 100^\circ\text{C}$ )	$I_{CER}$	—	5.0	mAdc
Emitter Cutoff Current ( $V_{EB} = 9.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc

## SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased $t = 1.0 \text{ s}$ (non-repetitive) ( $V_{CE} = 100 \text{ Vdc}$ )	$I_{S/b}$	0.2	—	Adc
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## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 5.0 \text{ Adc}$ , $V_{CE} = 2.0 \text{ Vdc}$ ) ( $I_C = 10 \text{ Adc}$ , $V_{CE} = 2.0 \text{ Vdc}$ )	$h_{FE}$	1 2	60	—
		6.0	30	
Collector-Emitter Saturation Voltage ( $I_C = 10 \text{ Adc}$ , $I_B = 2.0 \text{ Adc}$ ) ( $I_C = 15 \text{ Adc}$ , $I_B = 3.0 \text{ Adc}$ ) ( $I_C = 10 \text{ Adc}$ , $I_B = 2.0 \text{ Adc}$ , $T_C = 100^\circ\text{C}$ )	$V_{CE(\text{sat})}$	—	1.5	Vdc
		—	5.0	
		—	2.5	
Base-Emitter Saturation Voltage ( $I_C = 10 \text{ Adc}$ , $I_B = 2.0 \text{ Adc}$ ) ( $I_C = 10 \text{ Adc}$ , $I_B = 2.0 \text{ Adc}$ , $T_C = 100^\circ\text{C}$ )	$V_{BE(\text{sat})}$	—	1.6	Vdc
		—	1.6	

## DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product ( $I_C = 500 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f_{\text{test}} = 1.0 \text{ MHz}$ )	$f_T$	6.0	28	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f_{\text{test}} = 1.0 \text{ MHz}$ )	$C_{ob}$	125	500	pF

## SWITCHING CHARACTERISTICS

Resistive Load					
Delay Time	$(V_{CC} = 250 \text{ V}, I_C = 10 \text{ A},$ $I_{B1} = I_{B2} = 2.0 \text{ A}, t_p = 100 \mu\text{s},$ $\text{Duty Cycle} \leq 2.0\%)$	$t_d$	—	0.05	$\mu\text{s}$
Rise Time		$t_r$	—	1.0	$\mu\text{s}$
Storage Time		$t_s$	—	4.0	$\mu\text{s}$
Fall Time		$t_f$	—	0.7	$\mu\text{s}$
Inductive Load, Clamped					
Storage Time	$(I_C = 10 \text{ A(pk)}, V_{clamp} = \text{Rated } V_{CEX}, I_{B1} = 2.0 \text{ A},$ $V_{BE(off)} = 5.0 \text{ Vdc, } T_C = 100^\circ\text{C})$	$t_s$	—	5.0	$\mu\text{s}$
Fall Time		$t_f$	—	1.5	$\mu\text{s}$
Typical					
Storage Time	$(I_C = 10 \text{ A(pk)}, V_{clamp} = \text{Rated } V_{CEX}, I_{B1} = 2.0 \text{ A},$ $V_{BE(off)} = 5.0 \text{ Vdc, } T_C = 25^\circ\text{C})$	$t_s$	—	2.0	$\mu\text{s}$
Fall Time		$t_f$	—	0.09	$\mu\text{s}$

\*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle = 2%.

## TYPICAL ELECTRICAL CHARACTERISTICS

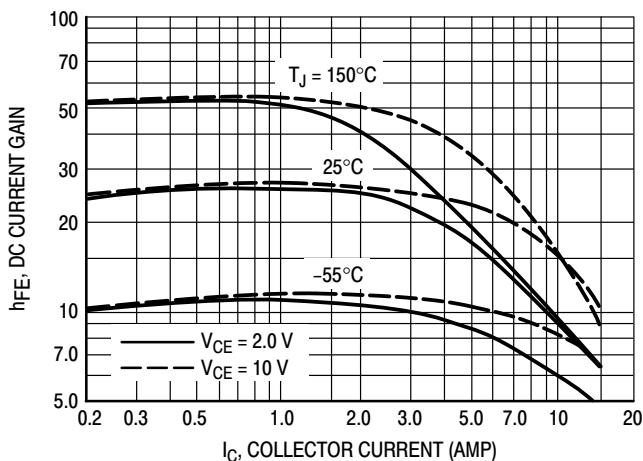


Figure 1. DC Current Gain

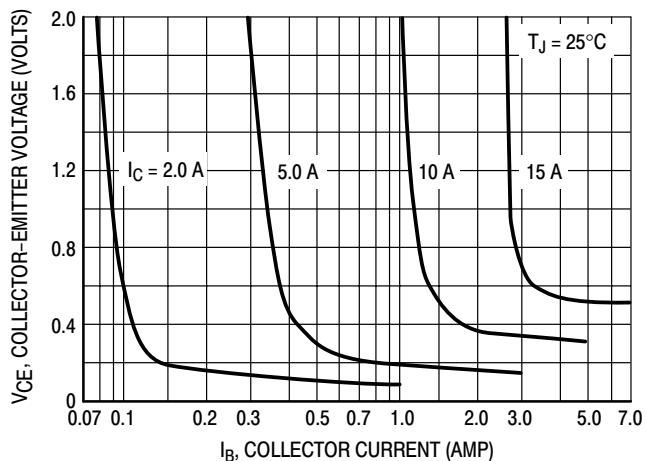


Figure 2. Collector Saturation Region

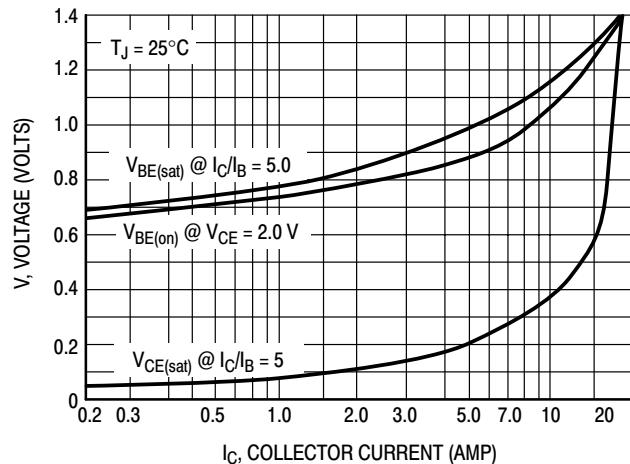


Figure 3. "On" Voltages

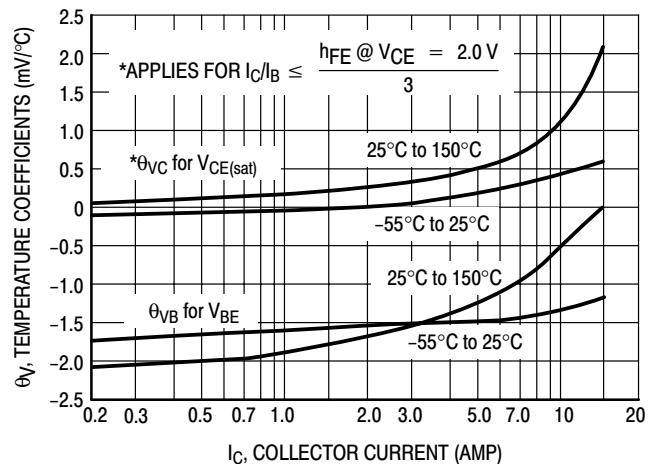


Figure 4. Temperature Coefficients

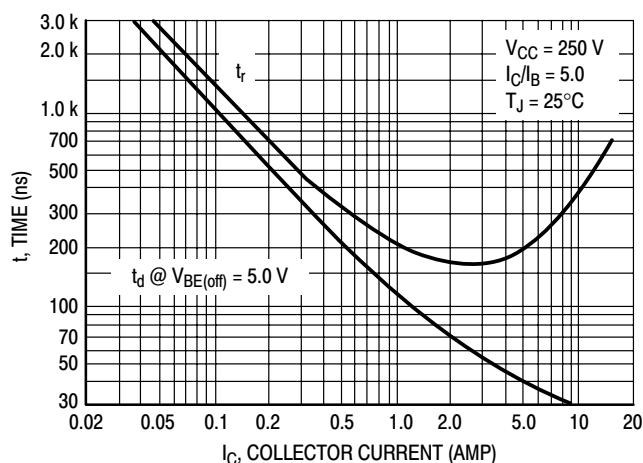


Figure 5. Turn-On Time

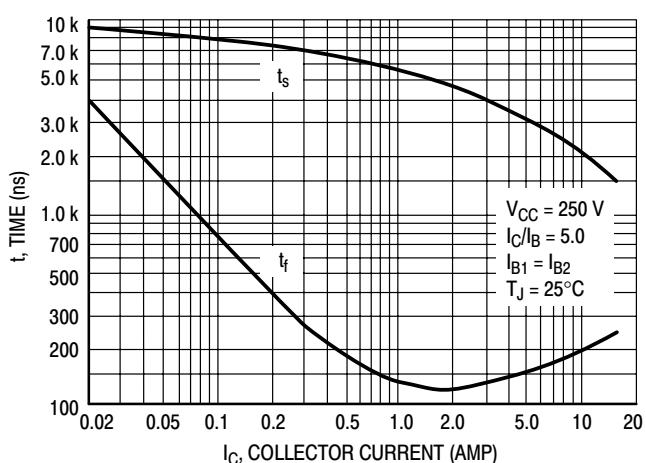


Figure 6. Turn-Off Time

## MAXIMUM RATED SAFE OPERATING AREAS

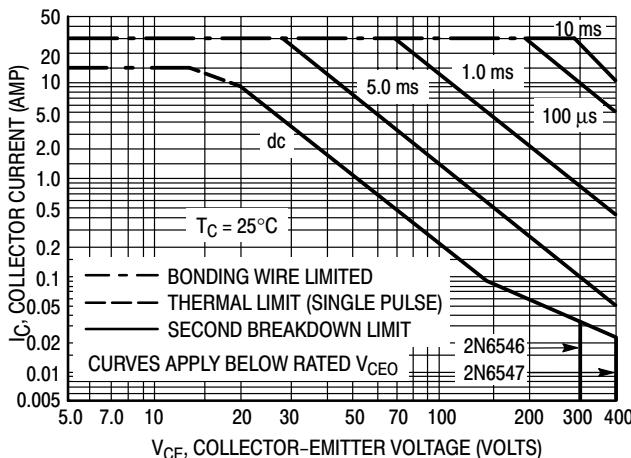


Figure 7. Forward Bias Safe Operating Area

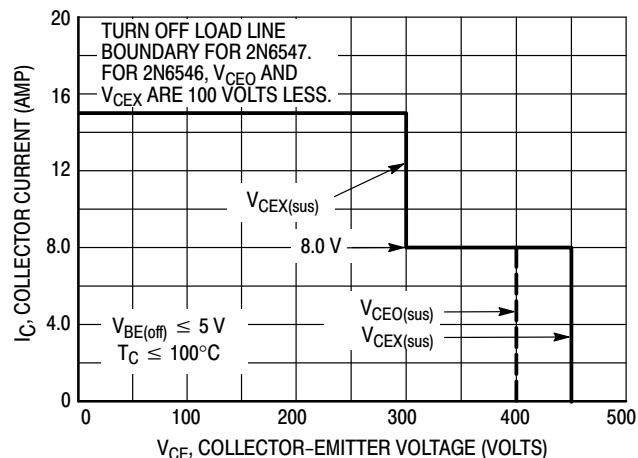


Figure 8. Reverse Bias Safe Operating Area

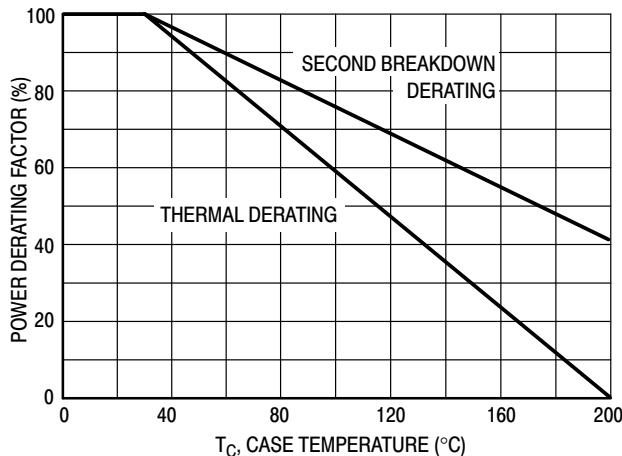


Figure 9. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

$T_{J(pk)}$  may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

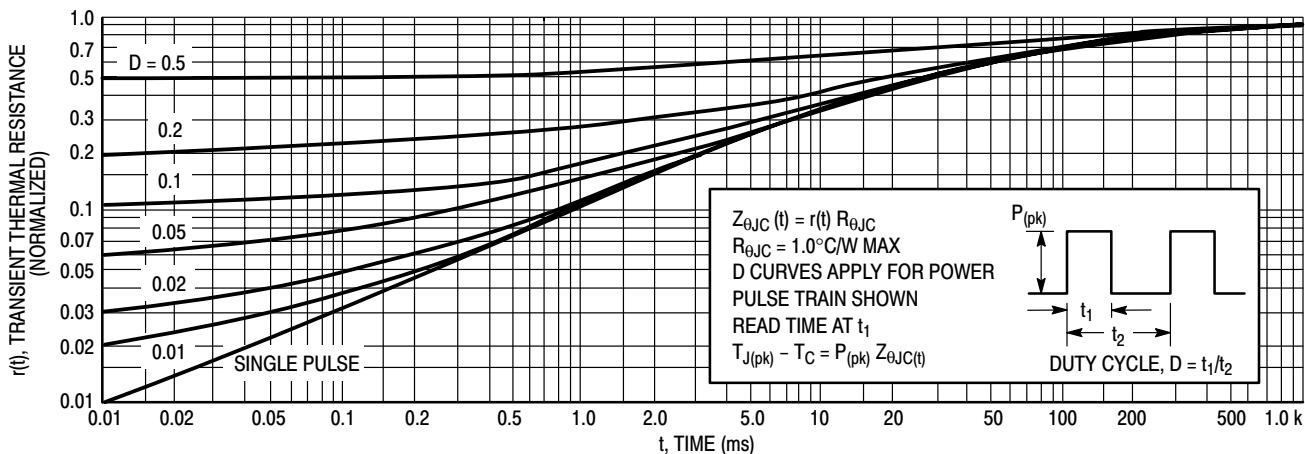
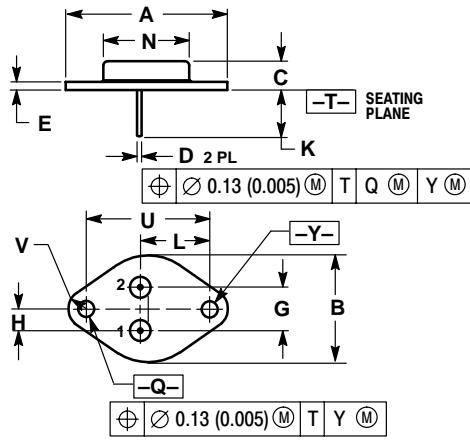


Figure 10. Thermal Response

## PACKAGE DIMENSIONS

CASE 1-07  
TO-204AA (TO-3)  
ISSUE Z

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550	REF	39.37	REF
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430	BSC	10.92	BSC
H	0.215	BSC	5.46	BSC
K	0.440	0.480	11.18	12.19
L	0.665	BSC	16.89	BSC
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187	BSC	30.15	BSC
V	0.131	0.188	3.33	4.77

## STYLE 1:

1. BASE
2. Emitter

CASE: COLLECTOR

## **Notes**

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