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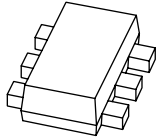
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Kind regards,

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# 2N7002PV

60 V, 350 mA N-channel Trench MOSFET

Rev. 1 — 5 August 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- AEC-Q101 qualified

### 1.3 Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

### 1.4 Quick reference data

Table 1. Quick reference data

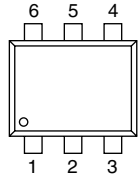
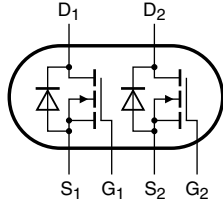
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_{amb} = 25\text{ °C}$	-	-	60	V
$V_{GS}$	gate-source voltage	$T_{amb} = 25\text{ °C}$	-	-	$\pm 20$	V
$I_D$	drain current	$T_{amb} = 25\text{ °C};$ $V_{GS} = 10\text{ V}$	<a href="#">[1]</a> -	-	350	mA
$R_{DS(on)}$	drain-source on-state resistance	$T_j = 25\text{ °C};$ $V_{GS} = 10\text{ V};$ $I_D = 500\text{ mA}$	-	1	1.6	$\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.



## 2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1		
2	G1	gate1		
3	D2	drain2		
4	S2	source2		
5	G2	gate2		
6	D1	drain1		

msd901

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
2N7002PV	-	plastic surface-mounted package; 6 leads	SOT666

## 4. Marking

Table 4. Marking codes

Type number	Marking code
2N7002PV	ZF

## 5. Limiting values

Table 5. Limiting values

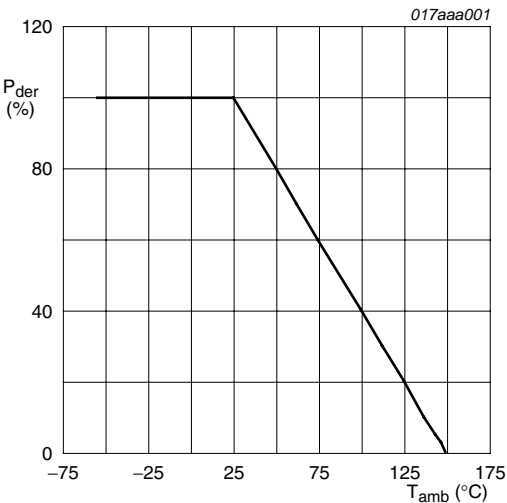
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per transistor</b>					
$V_{DS}$	drain-source voltage	$T_{amb} = 25\text{ °C}$	-	60	V
$V_{GS}$	gate-source voltage	$T_{amb} = 25\text{ °C}$	-	±20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$	[1]		
		$T_{amb} = 25\text{ °C}$	-	350	mA
		$T_{amb} = 100\text{ °C}$	-	250	mA
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C}$ ; single pulse; $t_p \leq 10\text{ }\mu\text{s}$	-	1.2	A

Table 5. Limiting values ...continued  
In accordance with the Absolute Maximum Rating System (IEC 60134).

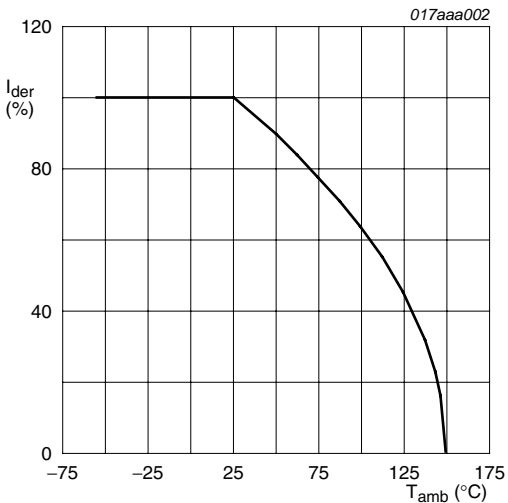
Symbol	Parameter	Conditions	Min	Max	Unit
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2] -	330	mW
			[1] -	390	mW
		T <sub>sp</sub> = 25 °C	-	1090	mW
Source-drain diode					
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1] -	350	mA
Per device					
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2] -	500	mW
T <sub>j</sub>	junction temperature			150	°C
T <sub>amb</sub>	ambient temperature		−55	+150	°C
T <sub>stg</sub>	storage temperature		−65	+150	°C

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.  
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



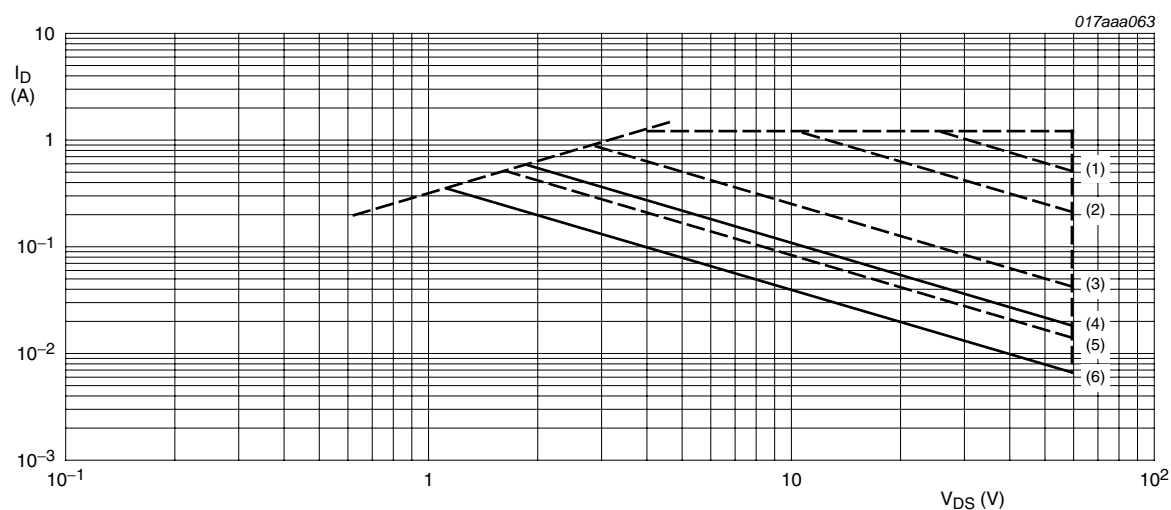
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig 1. Normalized total power dissipation as a function of ambient temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature



- $I_{DM}$  = single pulse
- (1)  $t_p = 100 \mu s$
  - (2)  $t_p = 1 ms$
  - (3)  $t_p = 10 ms$
  - (4) DC;  $T_{sp} = 25 ^\circ C$
  - (5)  $t_p = 100 ms$
  - (6) DC;  $T_{amb} = 25 ^\circ C$ ; drain mounting pad  $1 cm^2$

**Fig 3. Per transistor: Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage**

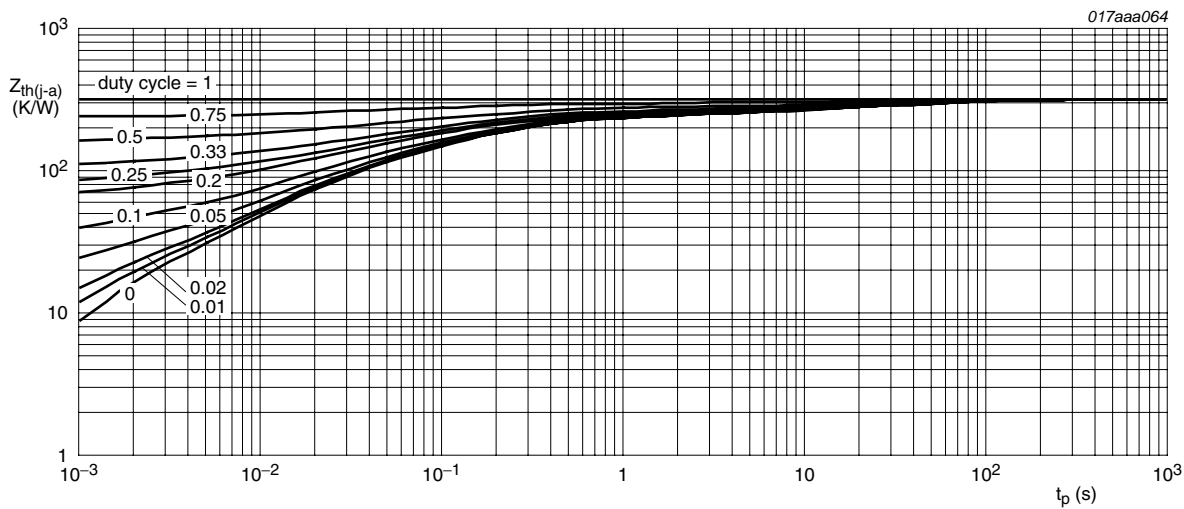
## 6. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] -	330	380	K/W
			[2] -	280	320	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point	-	-	-	115	K/W
<b>Per device</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] -	-	250	K/W

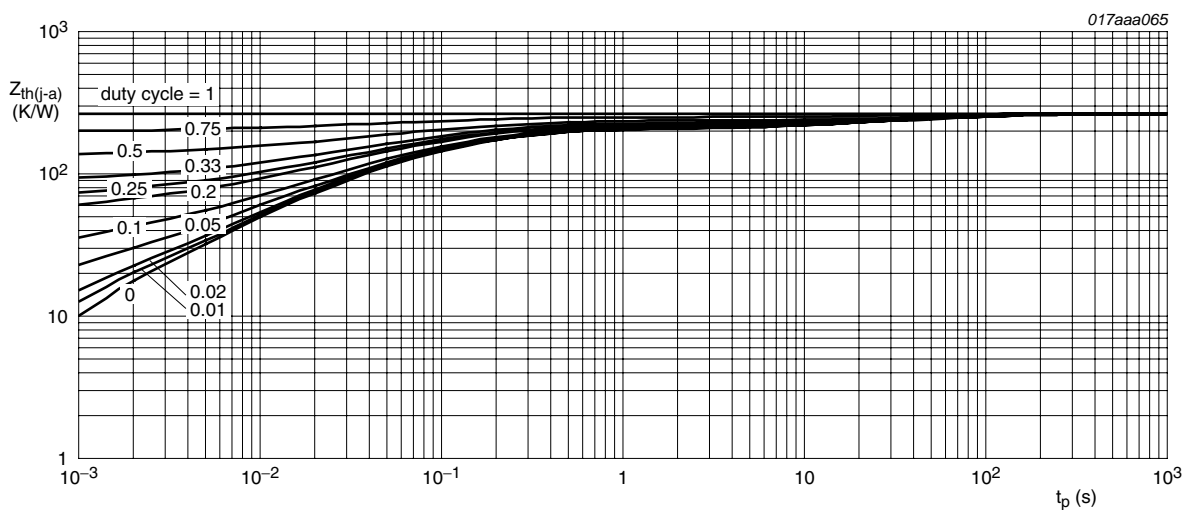
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $1 cm^2$ .



FR4 PCB, standard footprint

Fig 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm²

Fig 5. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 7. Characteristics

**Table 7. Characteristics**

$T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 250\text{ }\mu\text{A}$ ; $V_{DS} = V_{GS}$	1.1	1.75	2.4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60\text{ V}$ ; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	-	1	$\mu\text{A}$
		$T_j = 150\text{ }^{\circ}\text{C}$	-	-	10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 20\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance		[1]			
		$V_{GS} = 5\text{ V}$ ; $I_D = 50\text{ mA}$	-	1.3	2	$\Omega$
		$V_{GS} = 10\text{ V}$ ; $I_D = 500\text{ mA}$	-	1	1.6	$\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}$ ; $I_D = 200\text{ mA}$	[1]	-	400	mS
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 300\text{ mA}$ ;	-	0.6	0.8	nC
$Q_{GS}$	gate-source charge	$V_{DS} = 30\text{ V}$ ;	-	0.2	-	nC
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}$	-	0.2	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 10\text{ V}$ ;	-	30	50	pF
$C_{oss}$	output capacitance	$f = 1\text{ MHz}$	-	7	-	pF
$C_{rss}$	reverse transfer capacitance		-	4	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 50\text{ V}$ ;	-	3	6	ns
$t_r$	rise time	$R_L = 250\text{ }\Omega$ ;	-	4	-	ns
$t_{d(off)}$	turn-off delay time	$V_{GS} = 10\text{ V}$ ;	-	10	20	ns
$t_f$	fall time	$R_G = 6\text{ }\Omega$	-	5	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 115\text{ mA}$ ; $V_{GS} = 0\text{ V}$	0.47	0.75	1.1	V

[1] Pulse test:  $t_p \leq 300\text{ }\mu\text{s}$ ;  $\delta \leq 0.01$ .

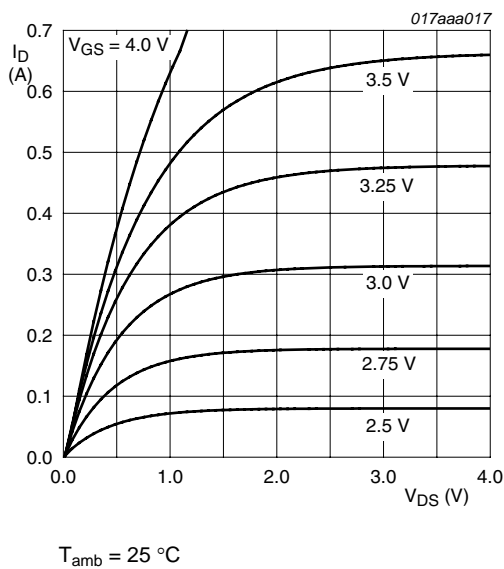


Fig 6. Per transistor: Output characteristics: drain current as a function of drain-source voltage; typical values

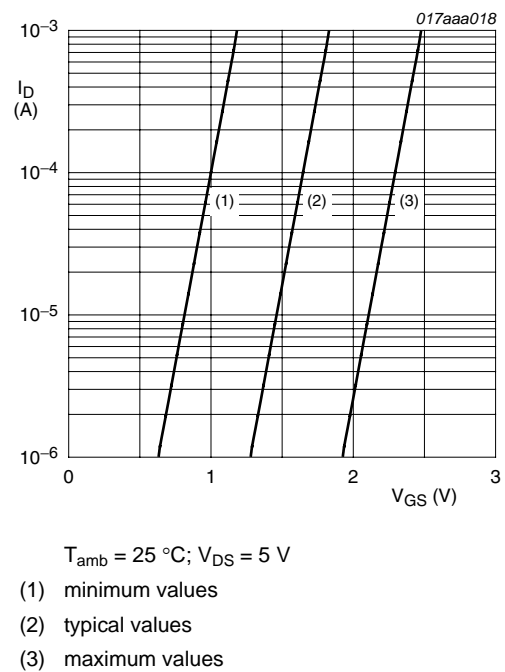


Fig 7. Per transistor: Sub-threshold drain current as a function of gate-source voltage

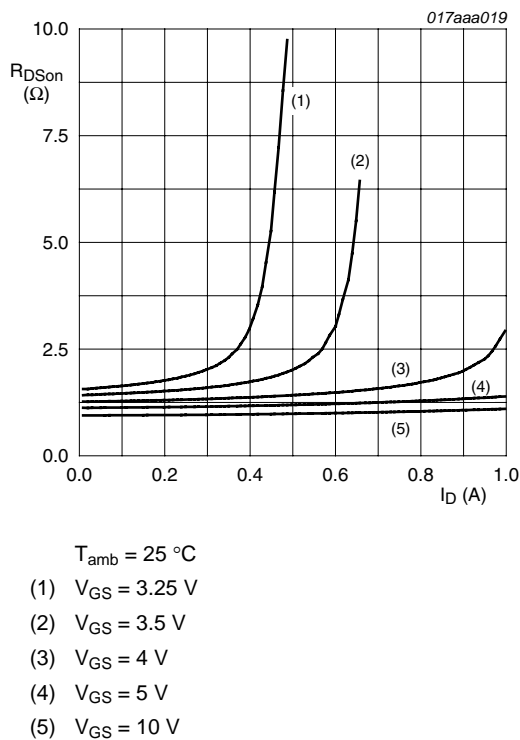


Fig 8. Per transistor: Drain-source on-state resistance as a function of drain current; typical values

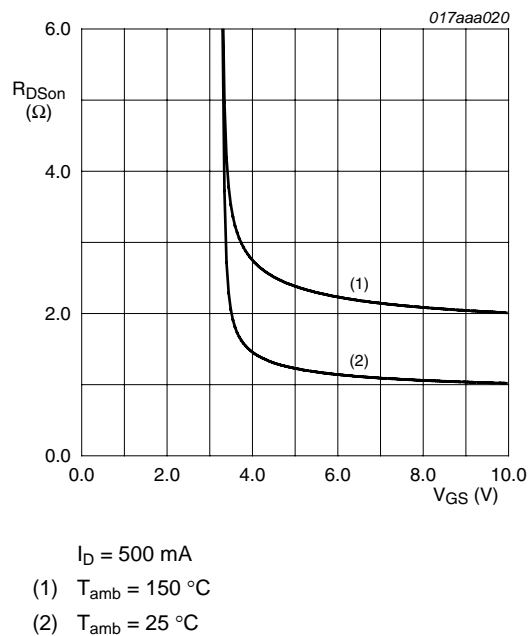
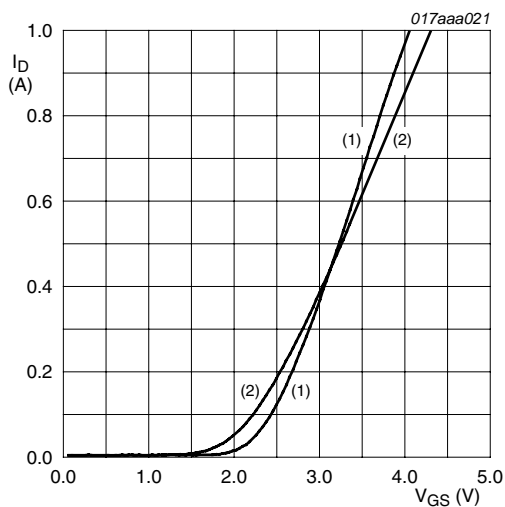


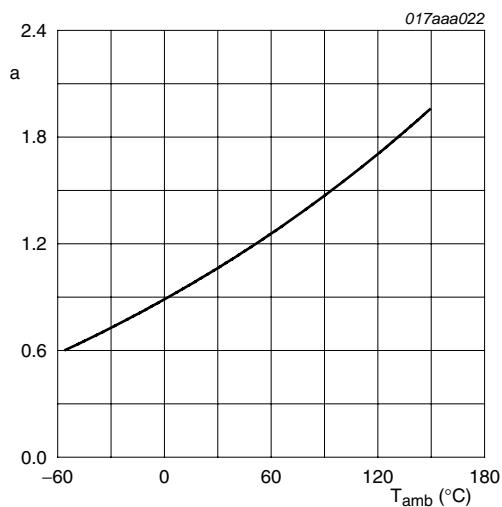
Fig 9. Per transistor: Drain-source on-state resistance as a function of gate-source voltage; typical values





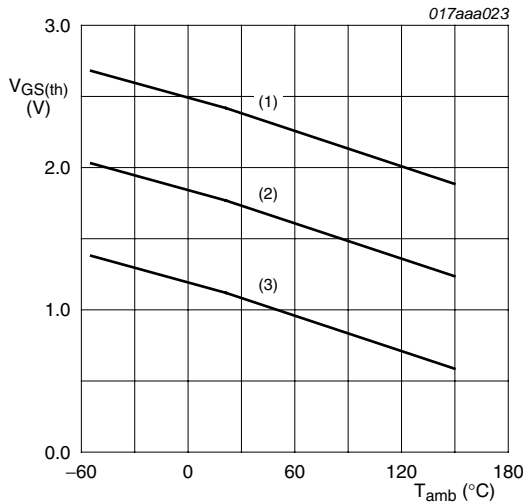
$V_{DS} > I_D \times R_{DSon}$   
(1)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
(2)  $T_{amb} = 150\text{ }^{\circ}\text{C}$

Fig 10. Per transistor: Transfer characteristics: drain current as a function of gate-source voltage; typical values



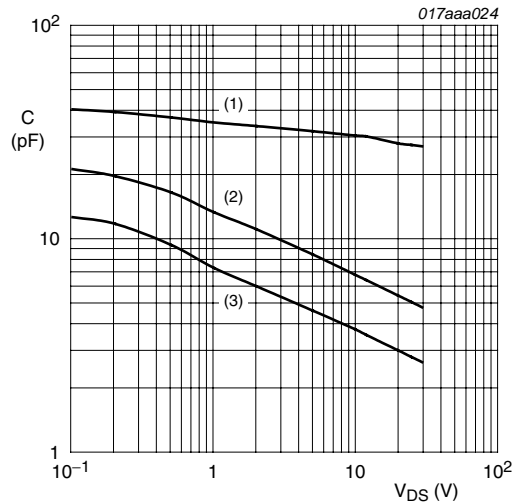
$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

Fig 11. Per transistor: Normalized drain-source on-state resistance as a function of ambient temperature; typical values



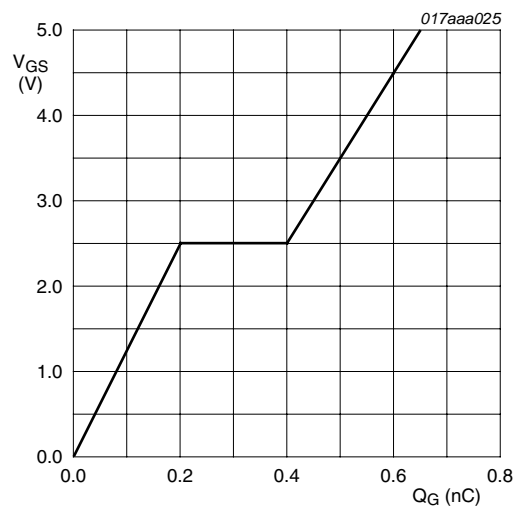
$I_D = 0.25\text{ mA}; V_{DS} = V_{GS}$   
(1) maximum values  
(2) typical values  
(3) minimum values

Fig 12. Per transistor: Gate-source threshold voltage as a function of ambient temperature



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$   
(1)  $C_{iss}$   
(2)  $C_{oss}$   
(3)  $C_{rss}$

Fig 13. Per transistor: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 300\text{ mA}$ ;  $V_{DS} = 30\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig 14. Per transistor: Gate-source voltage as a function of gate charge; typical values

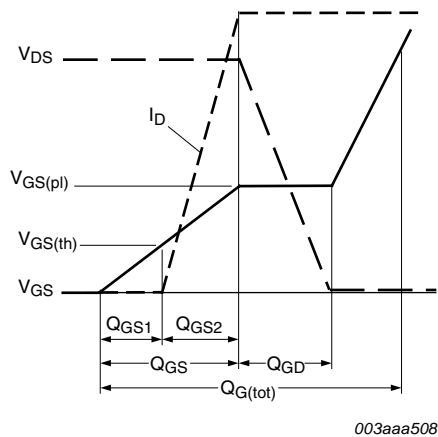
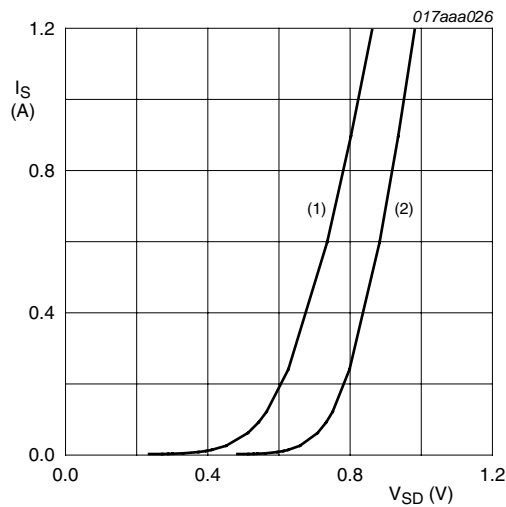


Fig 15. Per transistor: Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

- (1)  $T_{amb} = 150\text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig 16. Per transistor: Source current as a function of source-drain voltage; typical values

## 8. Test information

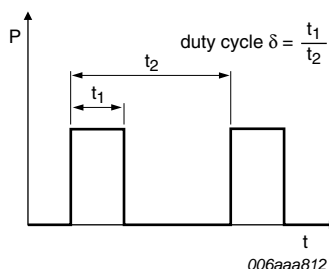


Fig 17. Duty cycle definition

### 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline

Plastic surface-mounted package; 6 leads

SOT666

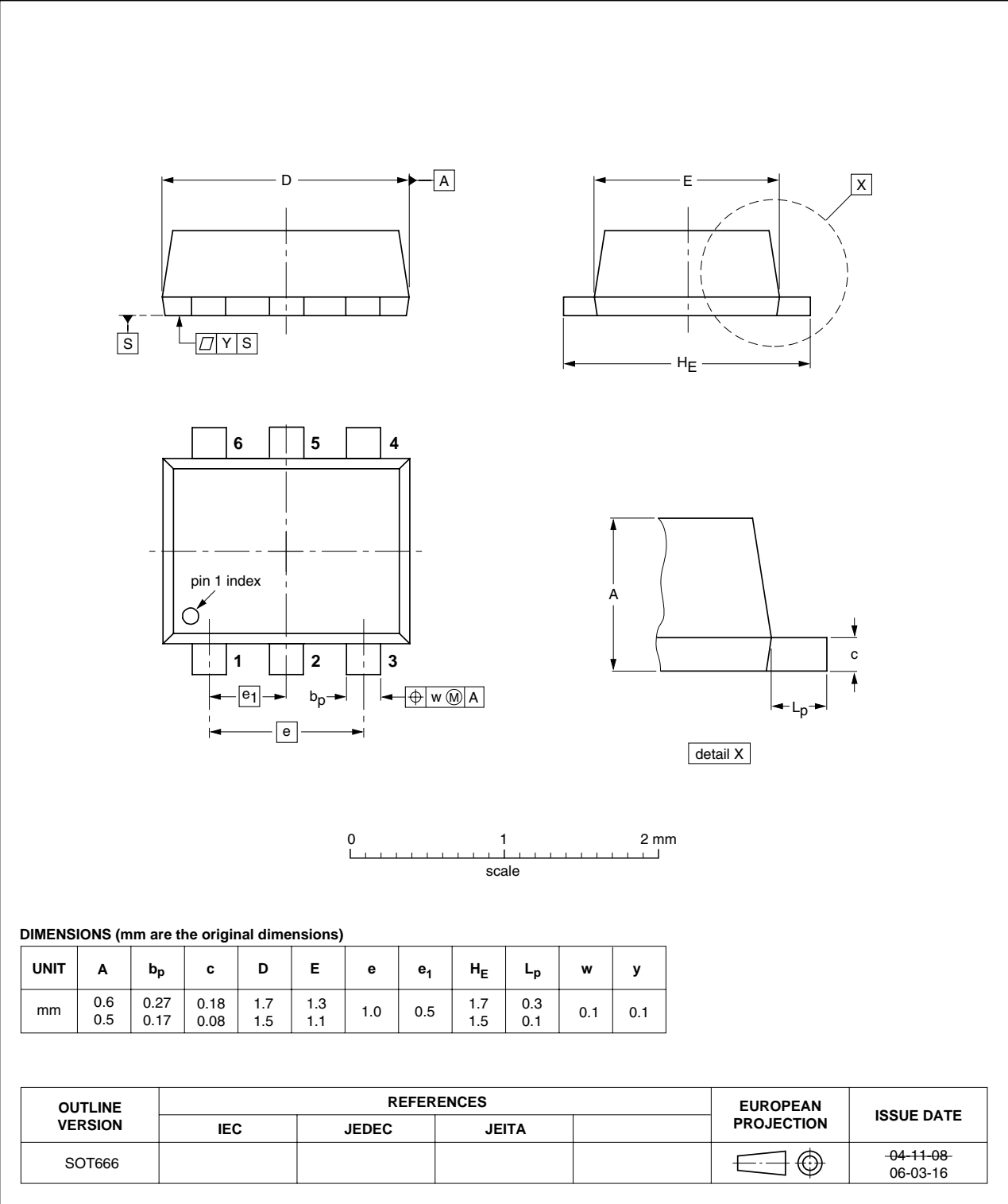
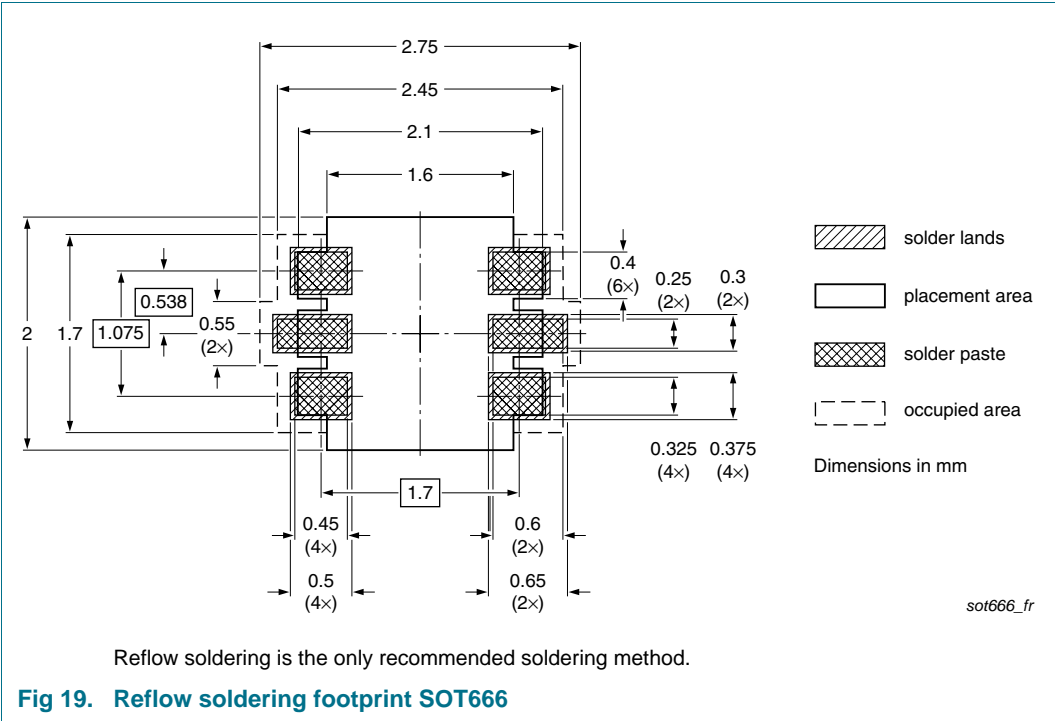


Fig 18. Package outline SOT666

10. Soldering



## 11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
2N7002PV v.1	20100805	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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