

2N7002W

60V N-Channel Enhancement Mode MOSFET

FEATURES

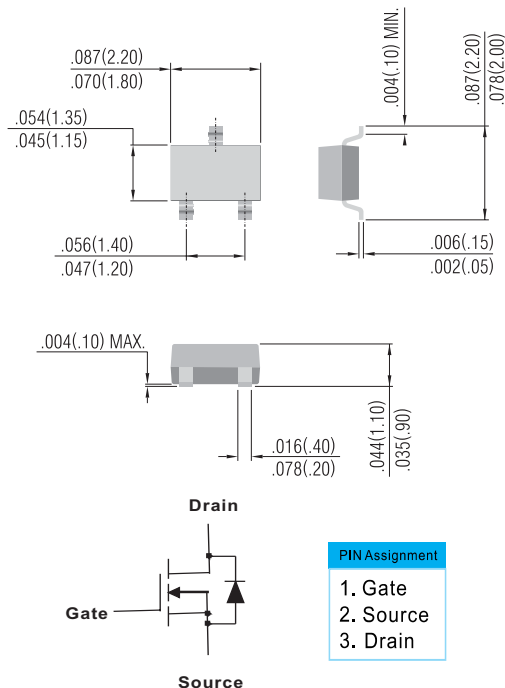
- $R_{DS(ON)}$ V_{GS} @10V, I_{DS} @500mA=5 Ω
- $R_{DS(ON)}$ V_{GS} @4.5V, I_{DS} @75mA=7.5 Ω
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Specially Designed for Battery Operated Systems, Solid-State Relays Drivers : Relays, Displays, Lamps, Solenoids, Memories, etc.
- In compliance with EU RoHS 2002/95/EC directives

MECHANICAL DATA

- Case: SOT-323 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Marking : 72W

SOT-323

Unit: inch (mm)



Maximum RATINGS and Thermal Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	115	mA
Pulsed Drain Current ¹⁾	I_{DM}	800	mA
Maximum Power Dissipation	P_D	$T_A=25^{\circ}\text{C}$ 200 $T_A=75^{\circ}\text{C}$ 120	mW
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to + 150	$^{\circ}\text{C}$
Junction-to Ambient Thermal Resistance(PCB mounted) ²	$R_{\theta JA}$	625	$^{\circ}\text{C/W}$

Note: 1. Maximum DC current limited by the package
2. Surface mounted on FR4 board, $t \leq 10$ sec

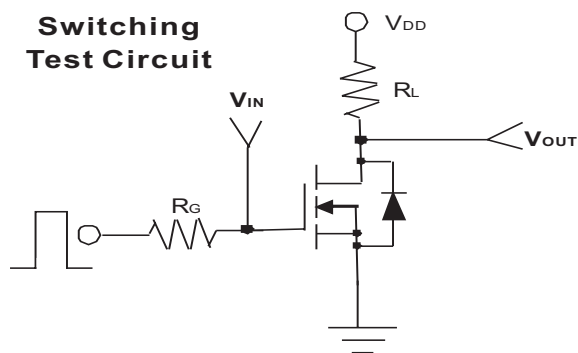
PAN JI T RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN,FUNCTIONS AND RELIABILITY WITHOUT NOTICE

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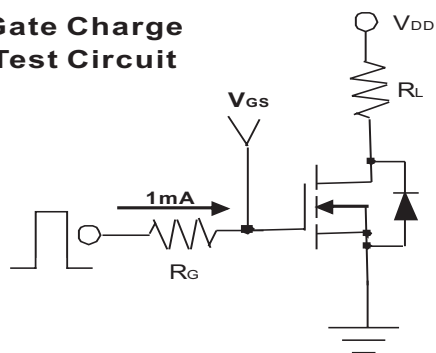
ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=10\mu A$	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=75mA$	-	-	7.5	Ω
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=500mA$	-	-	5	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate Body Leakage	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Forward Transconductance	g_{fS}	$V_{DS}=15V, I_D=250mA$	200	-	-	mS
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=500mA$ $V_{GS}=4.5V$	-	0.6	0.7	nC
Gate-Source Charge	Q_{gs}		-	0.1	-	
Gate-Drain Charge	Q_{gd}		-	0.08	-	
Turn-On Delay Time	t_{on}	$V_{DD}=10V, R_L=20\Omega$ $I_D=500mA, V_{GEN}=10V$ $R_G=10\Omega$	-	9	15	ns
Turn-Off Delay Time	t_{off}		-	21	26	
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $f=1.0MHz$	-	-	50	pF
Output Capacitance	C_{oss}		-	-	25	
Reverse Transfer Capacitance	C_{rss}		-	-	5	
Source-Drain Diode						
Max. Diode Forward Current	I_s	-	-	-	250	mA
Diode Forward Voltage	V_{SD}	$I_s=250mA, V_{GS}=0V$	-	0.93	1.2	V

Switching Test Circuit



Gate Charge Test Circuit



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Typical Characteristics Curves ($T_J=25^\circ\text{C}$, unless otherwise noted)

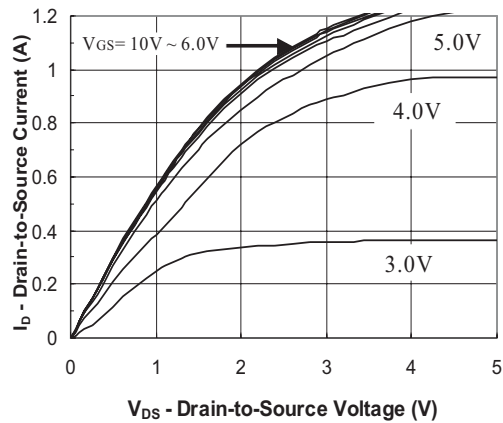


FIG.1- Output Characteristic

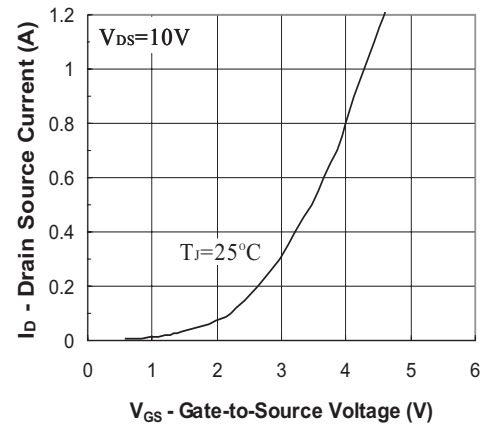


FIG.2- Transfer Characteristic

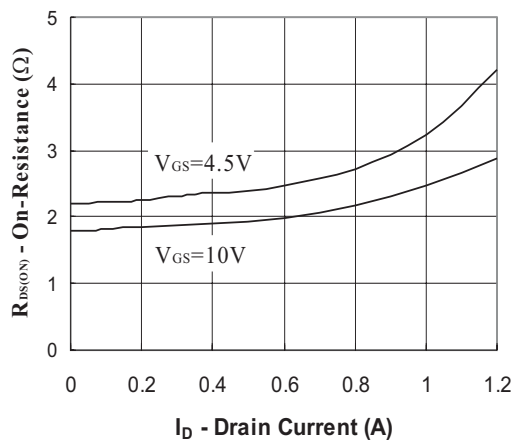


FIG.3- On Resistance vs Drain Current

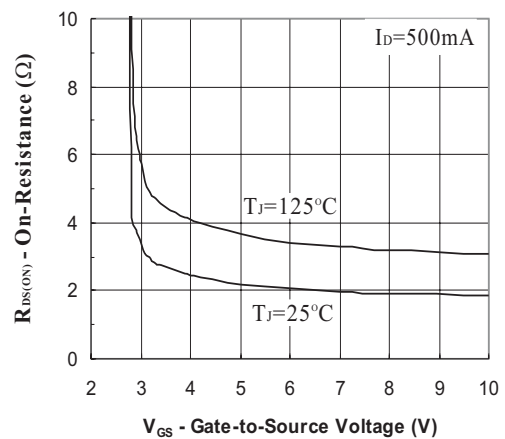


FIG.4- On Resistance vs Gate to Source Voltage

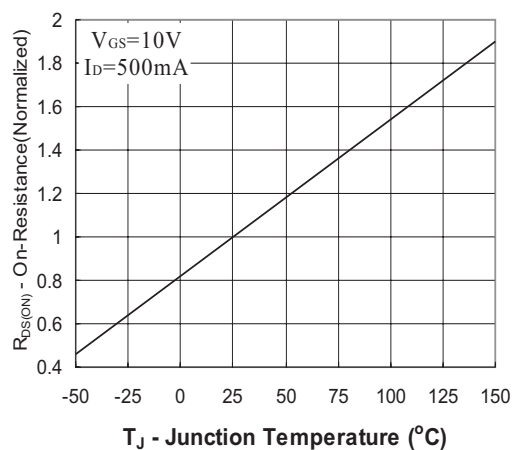


FIG.5- On Resistance vs Junction Temperature

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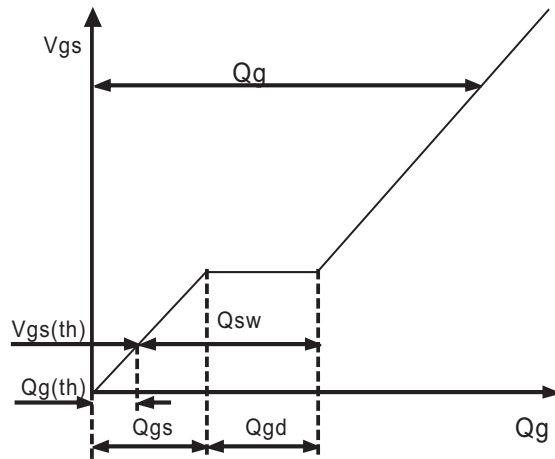


Fig.6 - Gate Charge Waveform

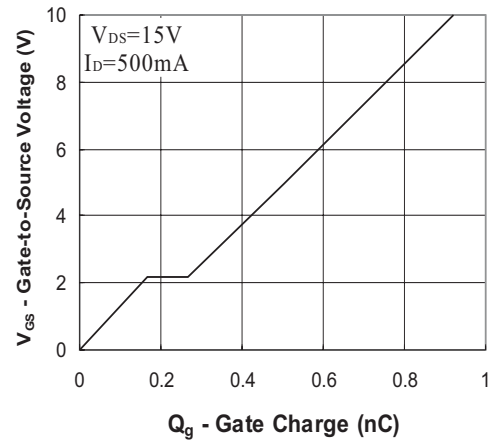


Fig.7 - Gate Charge

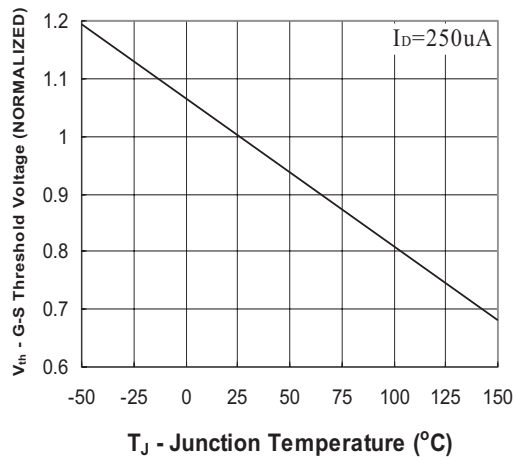


Fig.8 - Threshold Voltage vs Temperature

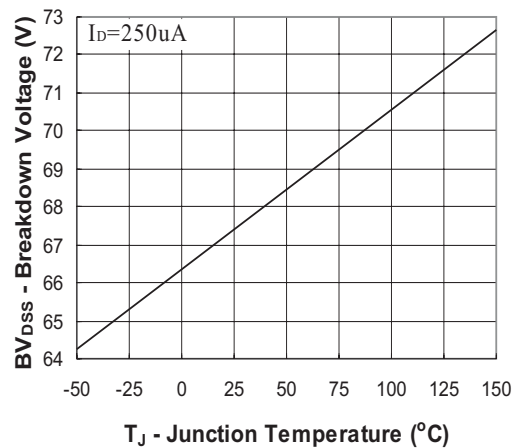


Fig.9 - Breakdown Voltage vs Junction Temperature

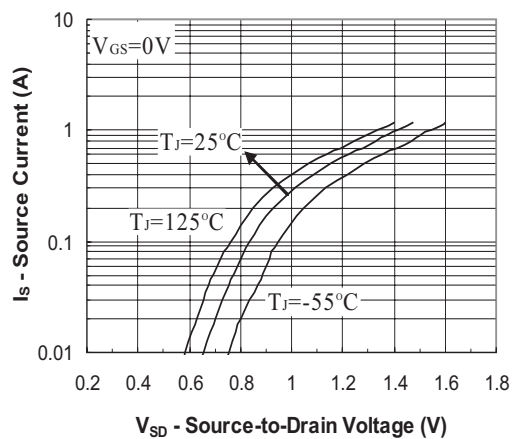


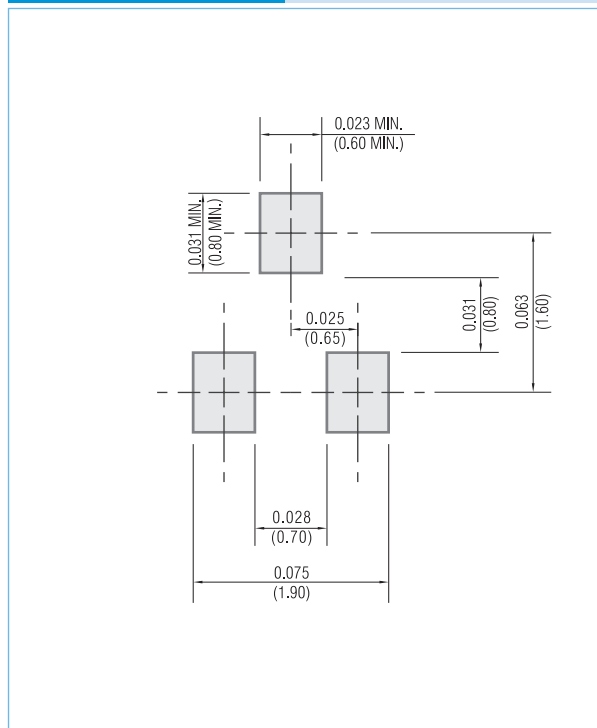
Fig.10 - Source-Drain Diode Forward Voltage

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MOUNTING PAD LAYOUT

SOT-323

Unit: inch (mm)



ORDER INFORMATION

- Packing information
 - T/R - 12K per 13" plastic Reel
 - T/R - 3K per 7" plastic Reel

LEGAL STATEMENT

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