**75Ω RF Digital Attenuator
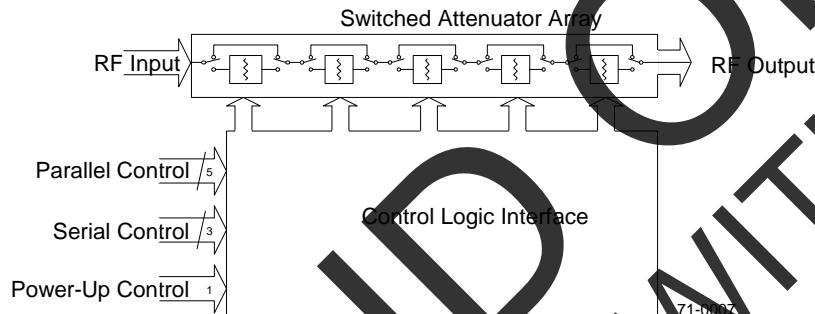5-bit, 15.5 dB, 1 – 2000 MHz**

Product Description

The PE4307 is a high linearity, 5-bit RF Digital Step Attenuator (DSA) covering a 15.5 dB attenuation range in 0.5 dB steps. The device is pin compatible with the PE430x series. This 75-ohm RF DSA provides both parallel (latched or direct mode) and serial CMOS control interface, operates on a single 3-volt supply and maintains high attenuation accuracy over frequency and temperature. It also has a unique control interface that allows the user to select an initial attenuation state at power-up. The PE4307 exhibits very low insertion loss and low power consumption. This functionality is delivered in a 4x4 mm QFN footprint.
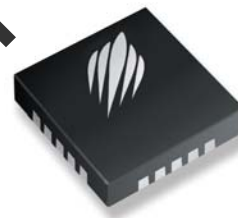
The PE4307 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features
- Attenuation: 0.5 dB steps to 15.5 dB
- Flexible parallel and serial programming interfaces
- Latched or direct mode
- Unique power-up state selection
- Positive CMOS control logic
- High attenuation accuracy and linearity over temperature and frequency
- Very low power consumption
- Single-supply operation
- 75Ω impedance
- Pin compatible with PE430x series
- Packaged in a 20-lead 4x4 mm QFN

Figure 1. Functional Schematic Diagram

Figure 2. Package Type
20-lead 4x4 mm QFN

Table 1. Electrical Specifications @ +25°C, V_{DD} = 3.0V

Parameter	Test Condition	Frequency	Minimum	Typical	Maximum	Unit
Operation Frequency			1		2000	MHz
Insertion Loss[1]		1 MHz ≤ 1.2 GHz	-	1.4	1.95	dB
Attenuation Accuracy	Any Bit or Bit Combination	1 MHz ≤ 1.2 GHz	-	-	±(0.15 + 4% of atten setting) Not to exceed +0.25 dB	dB dB
1 dB Compression[3,4]		1 MHz ≤ 1.2 GHz	30	34	-	dBm
Input IP3[1,2,4]	Two-tone inputs up to +18 dBm	1 MHz ≤ 1.2 GHz	-	52	-	dBm
Return Loss	Zo = 75 ohms	1 MHz ≤ 1.2 GHz	10	13	-	dB
Switching Speed	50% control to 0.5 dB of final value		-	-	1	µs

Notes: 1. Device Linearity will begin to degrade below 1 MHz
2. Max input rating in *Table 3* & Figures on Pages 4 to 6 for data across frequency
3. Note Absolute Maximum in *Table 3*
4. Measured in a 50Ω system
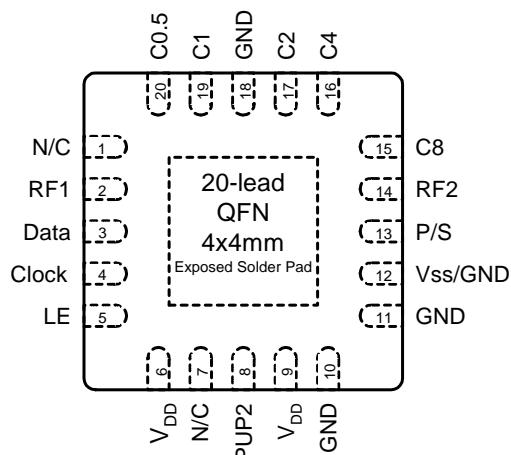
Figure 15. Pin Configuration (Top View)

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	N/C	No connect
2	RF1	RF port (Note 1)
3	Data	Serial interface data input (Note 4)
4	Clock	Serial interface clock input
5	LE	Latch Enable input (Note 2)
6	V_{DD}	Power supply pin
7	N/C	No connect
8	PUP2	Power-up selection bit
9	V_{DD}	Power supply pin
10	GND	Ground connection
11	GND	Ground connection
12	V_{ss}/GND	Negative supply voltage or GND connection (Note 3)
13	P/S	Parallel/Serial mode select
14	RF2	RF port (Note 1)
15	C8	Attenuation control bit, 8 dB
16	C4	Attenuation control bit, 4 dB
17	C2	Attenuation control bit, 2 dB
18	GND	Ground connection.
19	C1	Attenuation control bit, 1 dB
20	C0.5	Attenuation control bit, 0.5 dB
Paddle	GND	Ground for proper operation

Notes:
1. Both RF ports must be held at 0 V_{DC} or DC blocked with an external series capacitor
2. Latch Enable (LE) has an internal 100 kΩ resistor to V_{DD}
3. Connect pin 12 to GND to enable internal negative voltage generator. Connect pin 12 to V_{SS} (-V_{DD}) to bypass and disable internal negative voltage generator
4. Place a 10 kΩ resistor in series, as close to pin as possible to avoid frequency resonance. See "Resistor on 3" paragraph

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	150	°C
P_{IN}	Input power (50Ω)		+30	dBm
V_{ESD}	ESD voltage (Human Body Model)		500	V

Table 4. Operating Ranges

Parameter	Min	Typ	Max	Unit
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
I_{DD} Power Supply Current			100	µA
Digital Input High	0.7xV_{DD}			V
Digital Input Low			0.3xV_{DD}	V
Digital Input Leakage			1	µA
Input Power			+24	dBm
Temperature range	-40		85	°C

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rate specified in *Table 3.*

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Switching Frequency

The PE4307 has a maximum 25 kHz switching rate.

Resistor on Pin 3

A 10 kΩ resistor on the input to Pin 3 (see *Figure 5*) will eliminate package resonance between the RF input pin and the digital input. Specified attenuation error versus frequency performance is dependent upon this condition.

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Evaluation Kit

The Digital Attenuator Evaluation Kit was designed to ease customer evaluation of the PE4307 DSA.

J9 is used in conjunction with the supplied DC cable to supply V_{DD}, GND, and $-V_{DD}$. If use of the internal negative voltage generator is desired, then connect $-V_{DD}$ (black banana plug) to ground. If an external $-V_{DD}$ is desired, then apply -3V.

J1 should be connected to the LPT1 port of a PC with the supplied control cable. The evaluation software is written to operate the DSA in serial mode, so switch 7 (P/S) on the DIP switch SW1 should be ON with all other switches off. Using the software, enable or disable each attenuation setting to the desired combined attenuation. The software automatically programs the DSA each time an attenuation state is enabled or disabled.
Note: Jumper J6 supplies power to the evaluation board support circuits.

To evaluate the Power Up options, first disconnect the control cable from the evaluation board. The control cable must be removed to prevent the PC port from biasing the control pins.

During power up with P/S=1 high and LE=1, the default power-up signal attenuation is set to the value present on the five control bits on the five parallel data inputs (C0.5 to C8). This allows any one of the 32 attenuation settings to be specified as the power-up state.
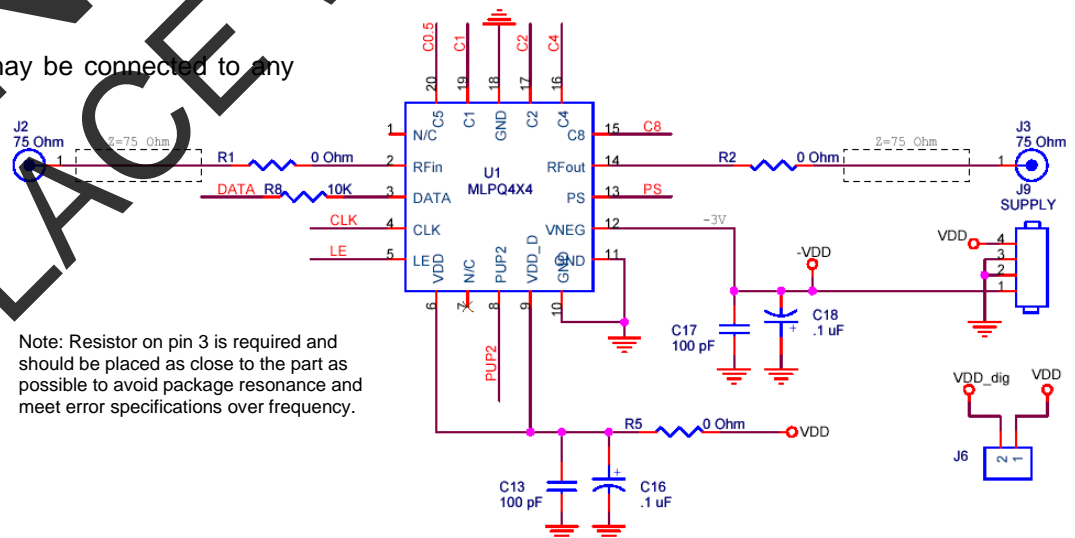
During power up with P/S=0 high and LE=0, the control bits are automatically set to one of two possible values presented through the PUP interface. These two values are selected by the power-up control bit, PUP2, as shown in *Table 6*.

Pins 1 and 7 are open and may be connected to any bias.

Figure 4. Evaluation Board Layout
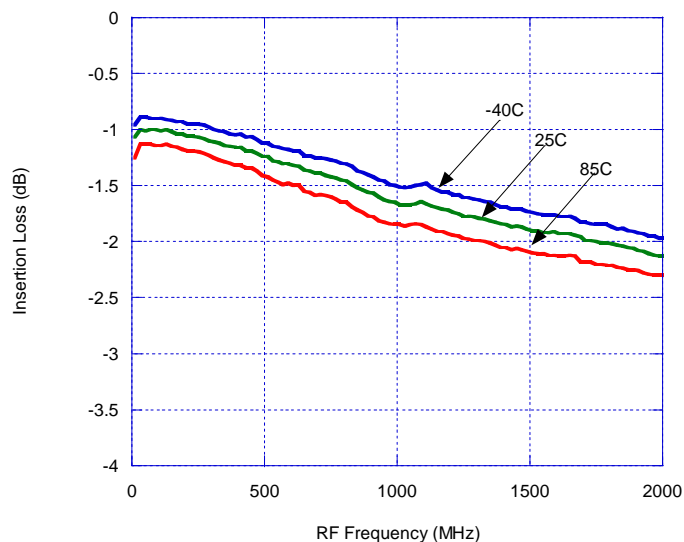Peregrine Specification 101/0112

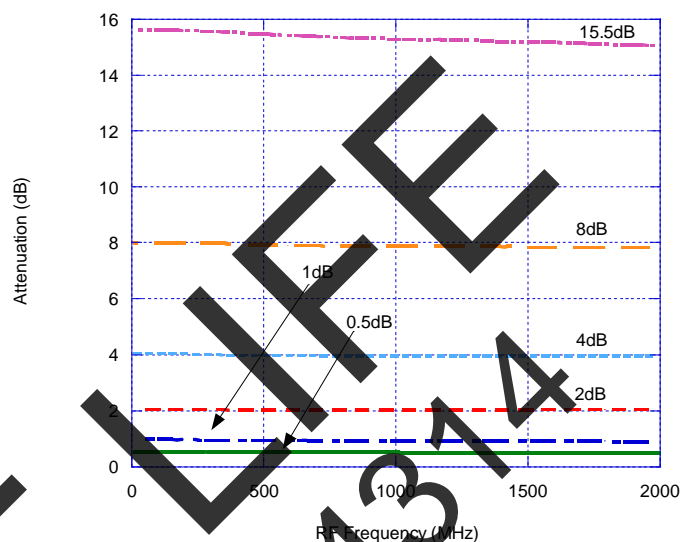## Figure 5. Evaluation Board Schematic
Peregrine Specification 102/0142

Note: Resistor on pin 3 is required and should be placed as close to the part as possible to avoid package resonance and meet error specifications over frequency.
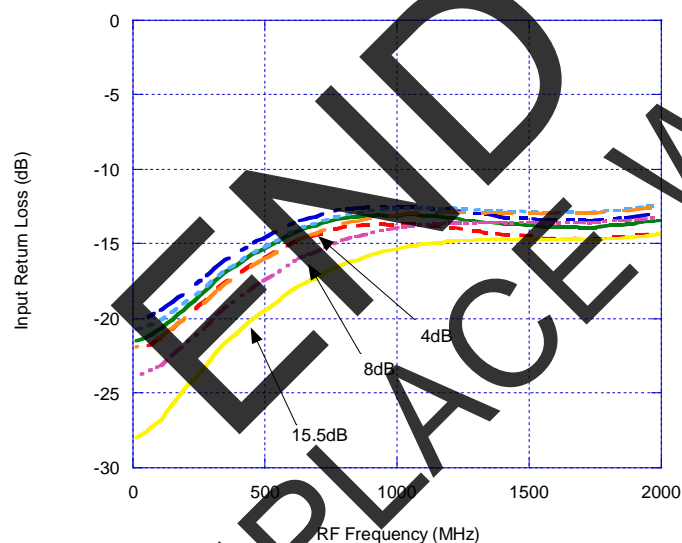
Typical Performance Data @ 25°C, V_{DD} = 3.0V

Figure 6. Insertion Loss (Zo = 75 ohms)

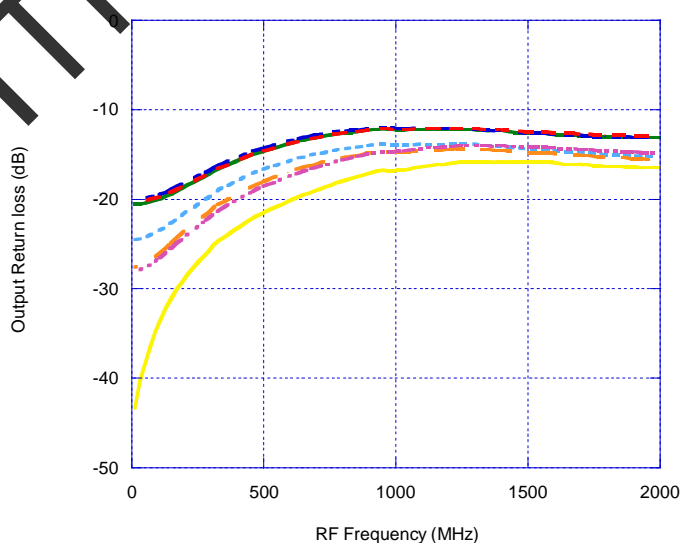### Figure 7. Attenuation at Major steps

Figure 8. Input Return Loss at Major Attenuation Steps (Zo = 75 ohms)

Figure 9. Output Return Loss at Major Attenuation Steps (Zo = 75 ohms)

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Typical Performance Data @ 25°C, V_{DD} = 3.0V

Figure 10. Attenuation Error Vs. Frequency
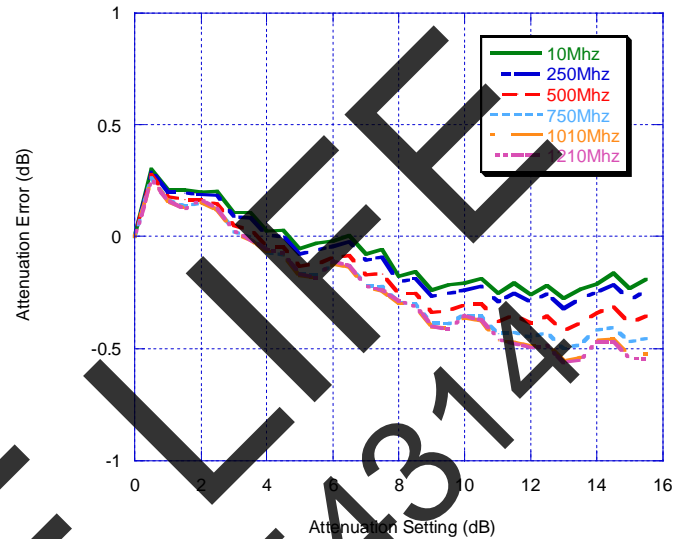

Figure 11. Attenuation Error Vs. Attenuatio Setting
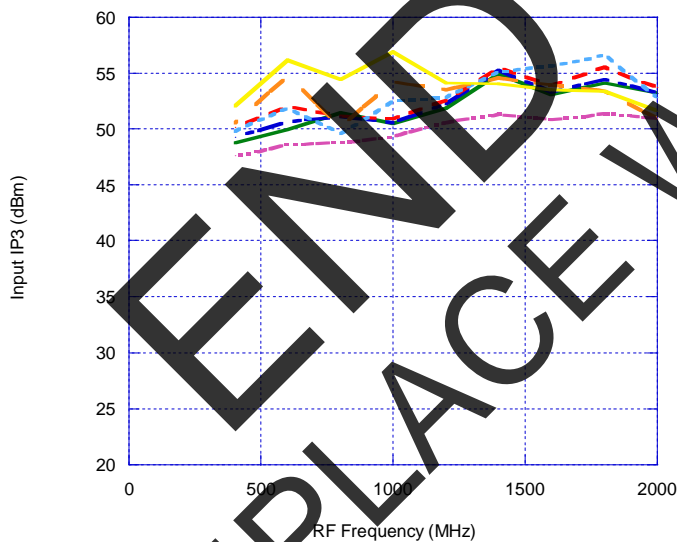

Figure 12. Input IP3 vs. Frequency (Zo = 50 ohms)

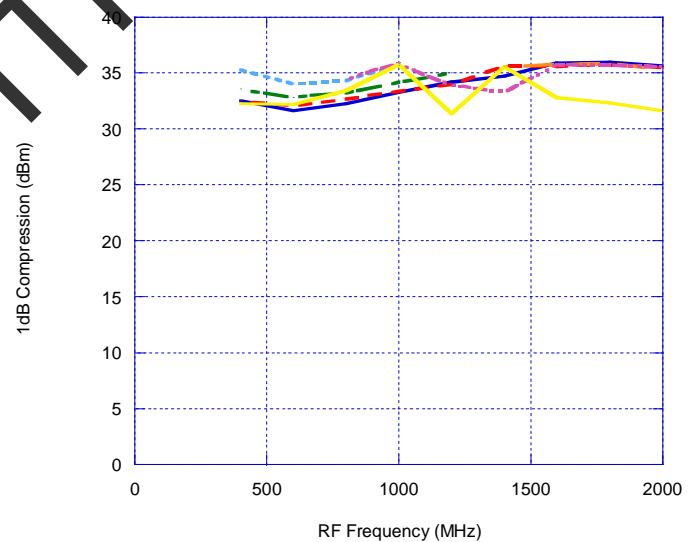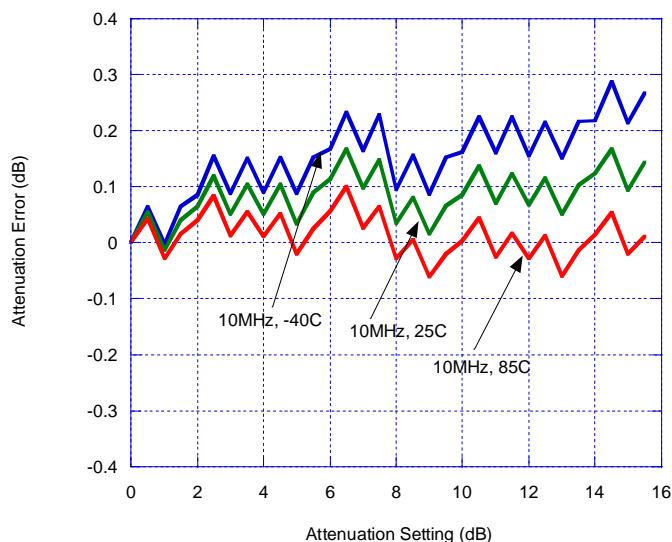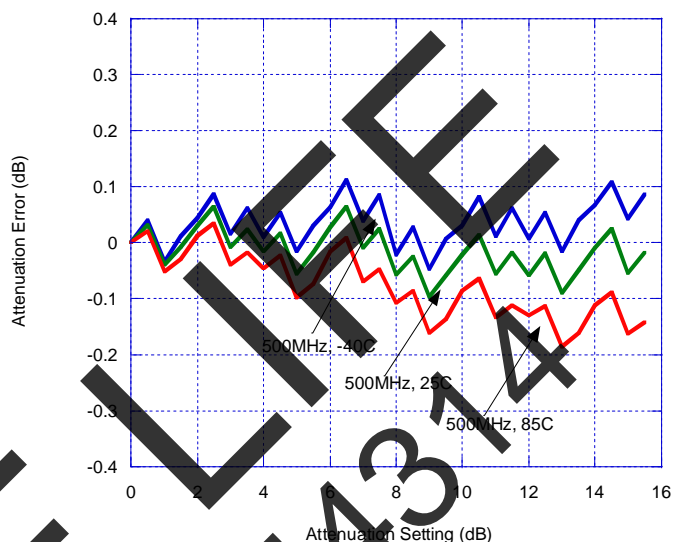### Figure 13. Input 1 dB Compression (Zo = 50 ohms)

Note: Positive attenuation error indicates higher attenuation than target value

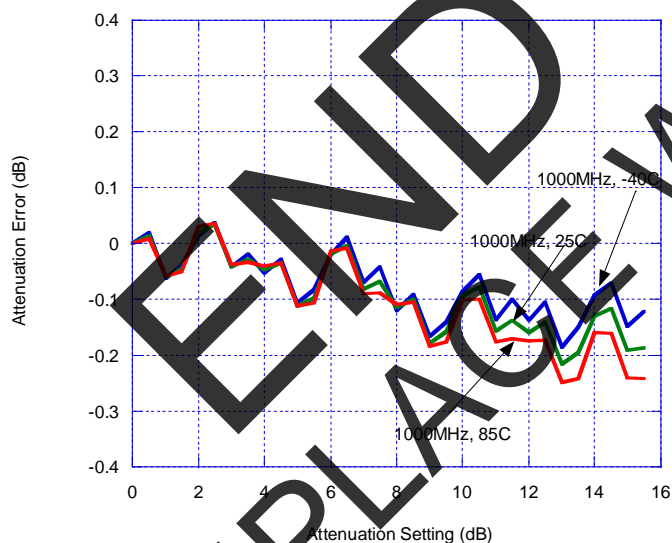## Typical Performance Data @ 25°C, V_{DD} = 3.0V

Figure 14. Attenuation Error Vs. Attenuation Setting

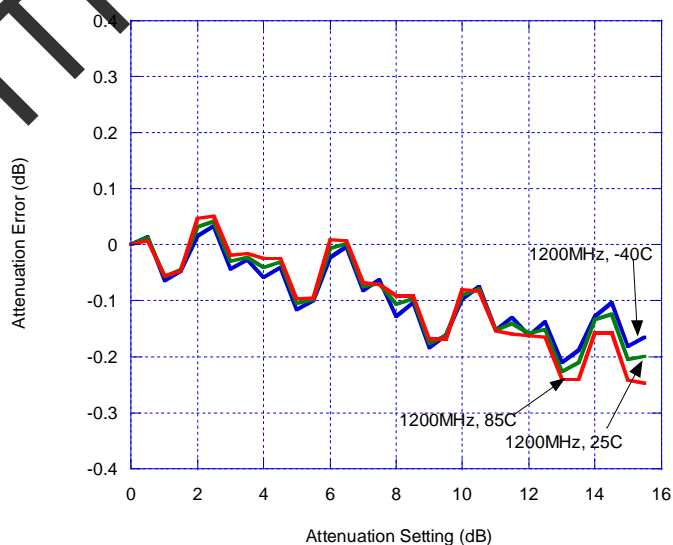### Figure 15. Attenuation Error Vs. Attenuation Setting

Figure 16. Attenuation Error Vs. Attenuation Setting

Figure 17. Attenuation Error Vs. Attenuation Setting

Note: Positive attenuation error indicates higher attenuation than target value

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Programming Options

Parallel/Serial Selection
Either a parallel or serial interface can be used to control the PE4307. The P/S bit provides this selection, with P/S = LOW selecting the parallel interface and P/S = HIGH selecting the serial interface.

Parallel / Direct Mode Interface
The parallel interface consists of five CMOS-compatible control lines that select the desired attenuation state, as shown in *Table 5*.

The parallel interface timing requirements are defined by *Figure 19* (Parallel Interface Timing Diagram), *Table 9* (Parallel Interface AC Characteristics), and switching speed (*Table 1*).

For *latched* parallel programming, the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per *Figure 19*) to latch new attenuation state into device.

For *direct* parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct Mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Table 5. Truth Table

P/S	C8	C4	C2	C1	C0.5	Attenuation State
0	0	0	0	0	0	Reference Loss
0	0	0	0	0	1	0.5 dB
0	0	0	0	1	0	1 dB
0	0	0	1	0	0	2 dB
0	0	1	0	0	0	4 dB
0	1	0	0	0	0	8 dB
0	1	1	1	1	1	15.5 dB

Note: Not all 32 possible combinations of C0.5-C8 are shown in table

Serial Interface
The PE4307's serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. The latch is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The start bit (B5) of the data should always be low to prevent an unknown state in the device. The timing for this operation is defined by *Figure 18* (Serial Interface Timing Diagram) and *Table 8* (Serial Interface AC Characteristics).

Power-up Control Settings
The PE4307 always assumes a specifiable attenuation setting on power-up. This feature exists for both the Serial and Parallel modes of operation, and allows a known attenuation state to be established before an initial serial or parallel control word is provided.

When the attenuator powers up in Serial mode (P/S = 1), the five control bits are set to whatever data is present on the five parallel data inputs (C0.5 to C8). This allows any one of the 32 attenuation settings to be specified as the power-up state.
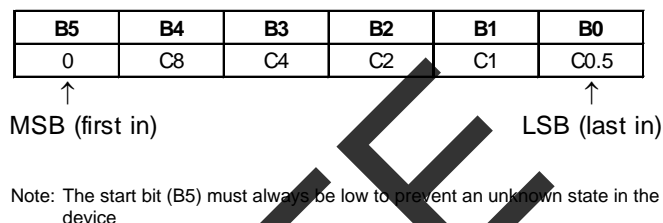
When the attenuator powers up in Parallel mode (P/S = 0) with LE = 0, the control bits are automatically set to one of two possible values. These two values are selected by the power-up control bit, PUP2, as shown in *Table 6* (Power-Up Truth Table, Parallel Mode).

Table 6. Power-Up Truth Table, Parallel Interface Mode

P/S	LE	PUP2	Attenuation State
0	0	0	Reference Loss
0	0	1	8 dB
0	1	X	Defined by **C0.5-C8**

Note: Power up with LE=1 provides normal parallel operation with C0.5-C8, and PUP2 is not active

Figure 18. Serial Interface Timing Diagram

Table 7. 5-Bit Attenuator Serial Programming Register Map

B5	B4	B3	B2	B1	B0
0	C8	C4	C2	C1	C0.5

↑ MSB (first in)   ↑ LSB (last in)

Note: The start bit (B5) must always be low to prevent an unknown state in the device

Figure 19. Parallel Interface Timing Diagram

Table 8. Serial Interface AC Characteristics

V_{DD} = 3.0V, -40°C < T_A < 85°C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
f_{Clk}	Serial data clock frequency (Note 1)		10	MHz
t_{ClkH}	Serial clock HIGH time	30		ns
t_{ClkL}	Serial clock LOW time	30		ns
t_{LESUP}	LE set-up time after last clock falling edge	10		ns
t_{LEPW}	LE minimum pulse width	30		ns
t_{SDSUP}	Serial data set-up time before clock rising edge	10		ns
t_{SDHLD}	Serial data hold time after clock falling edge	10		ns

Note 1: f_{Clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify fclk specification

Table 9. Parallel Interface AC Characteristics

V_{DD} = 3.0V, -40°C < T_A < 85°C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
t_{LEPW}	LE minimum pulse width	10	--	ns
t_{PDSUP}	Data set-up time before rising edge of LE	10	--	ns
t_{PDHLD}	Data hold time after falling edge of LE	10	--	ns

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Figure 20. Package Drawing
20-lead 4x4 mm QFN

TOP VIEW

BOTTOM VIEW

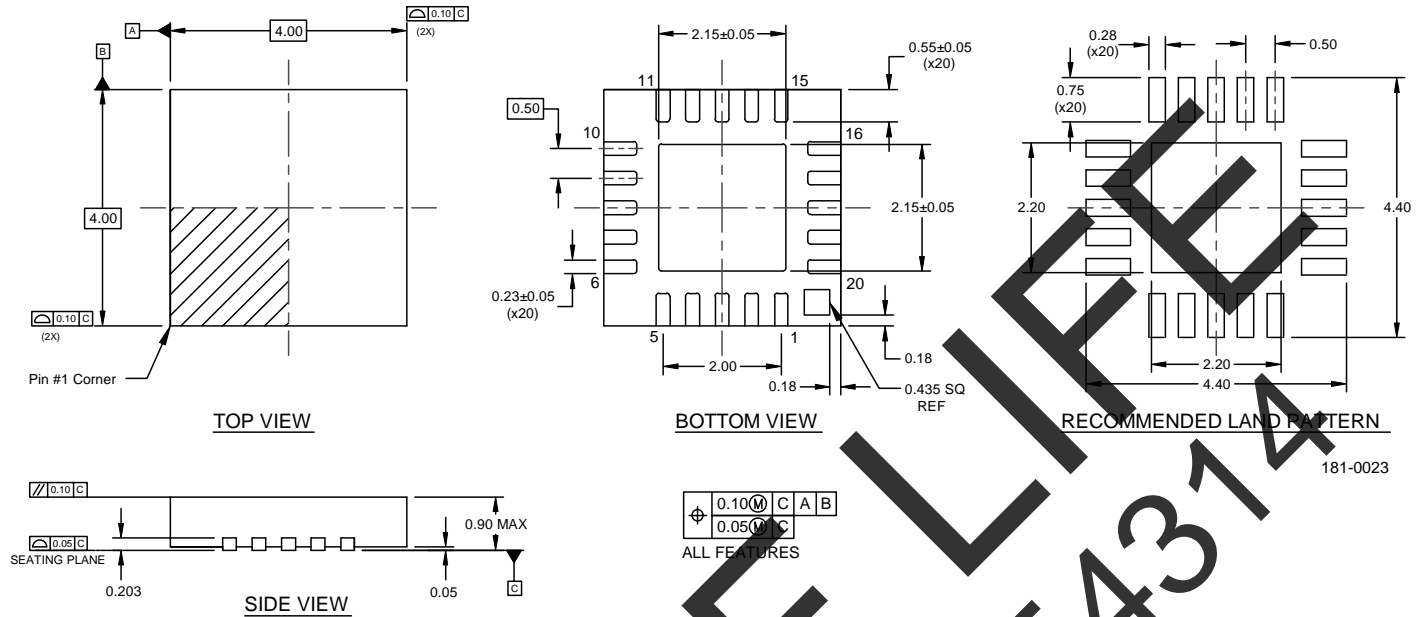RECOMMENDED LAND PATTERN

181-0023

SIDE VIEW

ALL FEATURES

Figure 21. Top Marking Specifications

4307
YYWW
ZZZZZ

YYWW = Date Code
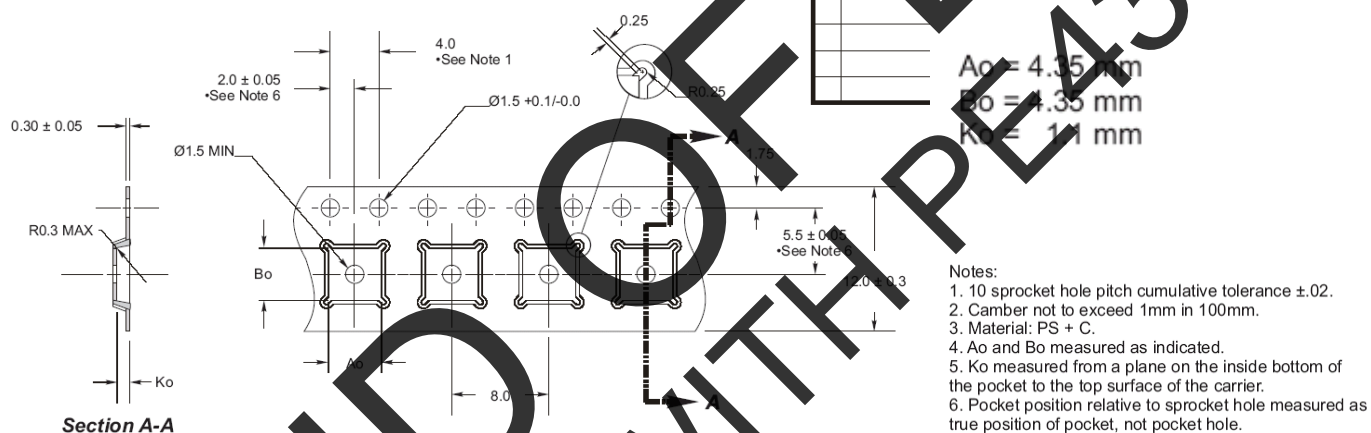ZZZZZ = Last five digits of PSC Lot Number

Figure 22. Tape and Reel Drawing

Section A-A

Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: PS + C.
4. Ao and Bo measured as indicated.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Table 10. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4307-01	4307	PE4307-20MLP 4x4mm-75A	20-lead 4x4 mm QFN	75 units / Tube
4307-02	4307	PE4307-20MLP 4x4mm-3000C	20-lead 4x4 mm QFN	3000 units / T&R
4307-00	PE4307-EK	PE4307-20MLP 4x4mm-EK	Evaluation Kit	1 / Box
4307-52	4307	PE4307G-20MLP 4x4mm-3000C	Green 20-lead 4x4 mm QFN	3000 units / T&R

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