NOTICE OF REVISION (NOR)

(See MIL-STD-480 for instructions)
This revision described below has been authorized for the document listed.

DATE (YYMMDD) 91-11-21

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Information and Regulatory Affairs, Office of Management and Budget, Washington, DC 20503.

1. ORIGINATOR NAME AND ADDRESS
Defense Electronics Supply Center
Dayton, Ohio 45444-5277

2. CAGE CODE 67268

3. NOR NO. 5962-R012-92

4. CAGE CODE 67268

5. DOCUMENT NO. 5962-89534

6. TITLE OF DOCUMENT
Microcircuits, Digital, CMOS, 80-Bit Numeric Processor Extension, Monolithic Silcon

7. REVISION LETTER
(Current) B
(New) C

8. ECP NO.
Not Required due to nature of changes

9. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES

All

10. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "C"
Revisions description column; add "Changes in accordance with NOR 5962-R012-92".
Revisions date column; add "91-11-21".

Sheet 3: Add Para. 1.5 as follow:
1.5 Digital logic testing for device classes Q and V.
Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) - - - - - 98.5 percent

11. THIS SECTION FOR GOVERNMENT USE ONLY

a. CHECK ONE
[x] EXISTING DOCUMENT SUPPLEMENTED BY THIS NOR MAY BE USED IN MANUFACTURE.
[ ] REVISED DOCUMENT MUST BE RECEIVED BEFORE MANUFACTURER MAY INCORPORATE THIS CHANGE.
[ ] CUSTODIAN OF MASTER DOCUMENT SHALL MAKE ABOVE REVISION AND FURNISH REVISED DOCUMENT TO:

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	SIGNATURE AND TITLE	DATE (YYMMDD)
DESC-ECC	Monica Poelking Chief, Custom Microelectronics	91-11-21
12. ACTIVITY ACCOMPLISHING REVISION	REVISION COMPLETED (Signature)	DATE (YYMMDD)
DESC-ECC	Tim H. Noh	91-11-21

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 02 and 03. Add case outline Y. Editorial changes throughout.	1990 AUG 8	Don Cool
B	Technical changes in absolute maximum ratings and recommended operating conditions. Editorial changes throughout.	91-08-29	Don Cool

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B		
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32		

REV STATUS OF SHEETS														
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Tim H. Noh

CHECKED BY
Tim H. Noh

APPROVED BY
D R Cool

DRAWING APPROVAL DATE
89-03-01

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, 80-BIT NUMERIC PROCESSOR EXTENSION, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89534**

SHEET 1 OF 32

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

5962	-	89534	01	M	X	X
Federal stock class designator	RHA designator (See 1.2.1)		Device type (See 1.2.2)	Device class designator (See 1.2.3)	Case outline (See 1.2.4)	Lead finish (See 1.2.5)

_____ V _____/
Drawing number

1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	80387-16	Numeric processor extension, 80-bit
02	80387-20	Numeric processor extension, 80-bit
03	80387-25	Numeric processor extension, 80-bit

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
X	P-AC (68-pin, 1.180" x 1.180" x .345"), pin grid array package
Y	See figure 1 (68-terminal, .970" x .970" x .115"), ceramic quad flat package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Voltage on any pin (referenced to GND)	-0.5 V dc to V_{CC} +0.5 V
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	2.1 W
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases X and Y	See MIL-M-38510, appendix C
Junction temperature (T_J)	+200°C
Lead temperature (soldering, 10 seconds)	+260°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.75 V dc to 5.25 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum high level input voltage (V_{IH}):	
Logic inputs	2.0 V dc
Clock input	3.7 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Frequency of operation:	
Device type 01	16 MHz
Device type 02	20 MHz
Device type 03	25 MHz

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagrams. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} = 5.25\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		1, 2, 3	All	-0.3 1/	+0.8	V
Input high voltage	V_{IH}				2.0	V_{CC}+0.3 1/	
386CLK2 input low voltage	V_{CL}				-0.3 1/	+0.8	
386CLK2 input low voltage	V_{CH}					V_{CC}+0.3 1/	
Output low voltage	V_{OL}	I_{OL}= 4 mA, D0-D31				0.45	
		I_{OL}= 2.5 mA, $\overline{READYO}$, $\overline{ERROR}$, $\overline{BUSY}$, PEREQ				0.45	
Output high voltage	V_{OH}	I_{OH} = -1 mA, D0-D31			2.4		
		I_{OH}= 2.5 mA, $\overline{READYO}$, $\overline{ERROR}$, $\overline{BUSY}$, PEREQ			2.4		
Input leakage current,	I_{LI}	$0\ V \le V_{IN} \le V_{CC}$			-15	+15	µA
Output leakage current	I_{LO}	$0.45\ V \le V_{OUT} \le V_{CC}$			-15	+15	
Supply current	I_{CC}	CLK2 = 32 Mhz CLK2 = 40 Mhz CLK2 = 50 Mhz 2/		01 02 03		250 310 390	mA
Input capacitance	C_{IN}	Fc = 1 Mhz, see 4.3.1c	4	All		10	pF
Output or I/O capacitance	C_{OUT}					12	
CLK2 capacitance	C_{CLK}					20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} = 5.25\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Functional tests		See 4.4.1d	7, 8	All			
Operating frequency period		Half of CLK2 frequency 3/	9, 10, 11	01 02 03	4 4 4	16 20 25	MHz
386CLK2 period	t_1	At 2 V 3/		01 02 03	31 25 20	125 125 125	ns
386CLK2 high time 1/	t_{2a}			01 02 03	9 8 7		
386CLK2 high time 1/	t_{2b}	At 3.7 V 3/		01 02 03	5 5 4		
386CLK2 low time 1/	t_{3a}	At 2 V 3/		01 02 03	9 8 7		
386CLK2 low time 1/	t_{3b}	At 0.8 V 3/		01 02 03	7 6 5		
386CLK2 fall time 1/	t_4	3.7 V to 0.8 V 3/		01 02 03		8 8 7	
386CLK2 rise time 1/	t_5	0.8 V to 3.7 V 3/		01 02 03		8 8 7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} = 5.25\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
386CLK2/387CLK2 ratio 1/		3/	9, 10, 11	All	10/16	14/10	ns
387CLK2 period	t_1	At 2.0 V 3/		01 02 03	31 25 20	125 125 125	
387CLK2 high time 1/	t_{2a}			01 02 03	9 8 7		
387CLK2 high time 1/	t_{2b}	At 3.7 V 3/		01 02 03	5 5 4		
387CLK2 low time 1/	t_{3a}	At 2.0 V 3/		01 02 03	9 8 7		
387CLK2 low time 1/	t_{3b}	At 0.8 V 3/		01 02 03	7 6 5		
387CLK2 fall time 1/	t_4	3.7 V to 0.8 V 3/		01 02 03		8 8 7	
387CLK2 rise time 1/	t_5	0.8 V to 3.7 V 3/		01 02 03		8 8 7	
READY out delay	t_7	C_L = 75 pF 3/ 4/		01 02 03	4 3 3	34 31 24	
READY out delay	t_7	C_L = 25 pF 3/		01 02 03	4 3 3	31 27 21	
PEREQ out delay	t_7	C_L = 75 pF 3/ 4/		01 02 03	5 5 4	34 34 33	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} = 5.25\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
BUSY out delay	t_7	C_L = 75 pF 3/ 4/	9, 10, 11	All	5 5 4	34 29 29	ns
ERROR out delay	t_7			01 02 03	5 5 4	34 34 33	
BUSY out delay	t_7	C_L = 25 pF 3/		03	4	27	
D31-D0 out delay	t_8	C_L = 120 pF 3/ 4/		01 02 03	1/ 1 1 0	54 54 50	
D31-D0 setup time	t_{10}	3/		All	11		
D31-D0 hold time	t_{11}				11		
D31-D0 float time 1/	t_{12}	C_L = 120 pF 3/ 4/ 5/		01 02 03	6 6 5	33 27 24	
PEREQ float time 1/	t_{13}	C_L = 75 pF 3/ 4/ 5/		01 02 03	1 1 1	60 50 40	
BUSY float time	t_{13}	3/		01 02 03	1 1 1	60 50 40	
ERROR float time	t_{13}			01 02 03	1 1 1	60 50 40	
$\overline{READYO}$ float time	t_{13}			01 02 03	1 1 1	60 50 40	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} = 5.25\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{ADS}$ setup time	t_{14}	3/	9, 10, 11	All	26 21 16		ns
$\overline{ADS}$ hold time	t_{15}			01 02 03	5 5 4		
W/$\overline{R}$ setup time	t_{14}			03	26 21 16		
W/$\overline{R}$ hold time	t_{15}			01 02 03	5 5 4		
$\overline{READY}$ setup time	t_{16}			All	21 12 9		
$\overline{READY}$ hold time	t_{17}				4		
$\overline{CMD}$ setup time	t_{16}			01 02 03	21 19 16		
$\overline{CMD}$ hold time	t_{17}			01 02 03	2 4 4		
$\overline{NPS1}$, NPS2 setup time	t_{16}			01 02 03	21 19 16		
$\overline{NPS1}$, NPS2 hold time	t_{17}			01 02 03	2 2 4		
STEN setup time	t_{16}	3/	9, 10, 11	01 02 03	21 21 15		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} = 5.25\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
STEN hold time	t_{17}	3/	9, 10, 11	All	2		ns
RESETIN setup time	t_{18}			01 02 03	13 12 10		
RESETIN hold time	t_{19}			01 02 03	4 4 3		
RESETIN (duration)	t_{30}			All	40		387CLK2
RESETIN inactive to 1st opcode write	t_{31}				50		
BUSY (duration)	t_{32}				6		386CLK2
ERROR(in) active to BUSY inactive	t_{33}				6		
PEREQ inactive to ERROR active	t_{34}				6		
READY active to BUSY active	t_{35}				4	4	
READY (opcode write to opcode/operand write	t_{36}				6		
READY (operand write to operand write)	t_{37}				8		

1/ Guaranteed, if not tested, to the limits specified.
2/ I_{CC} is measured at steady state, maximum capacitance loading on the outputs, and worst case dc level at the inputs, 386CLK2 at the same frequency as 387CLK2.
3 See figure 4.
4 Capacitive load for 25 Mhz equals 50 pF.
5 Float condition occurs when maximum output current becomes less than I_{LO} in magnitude.

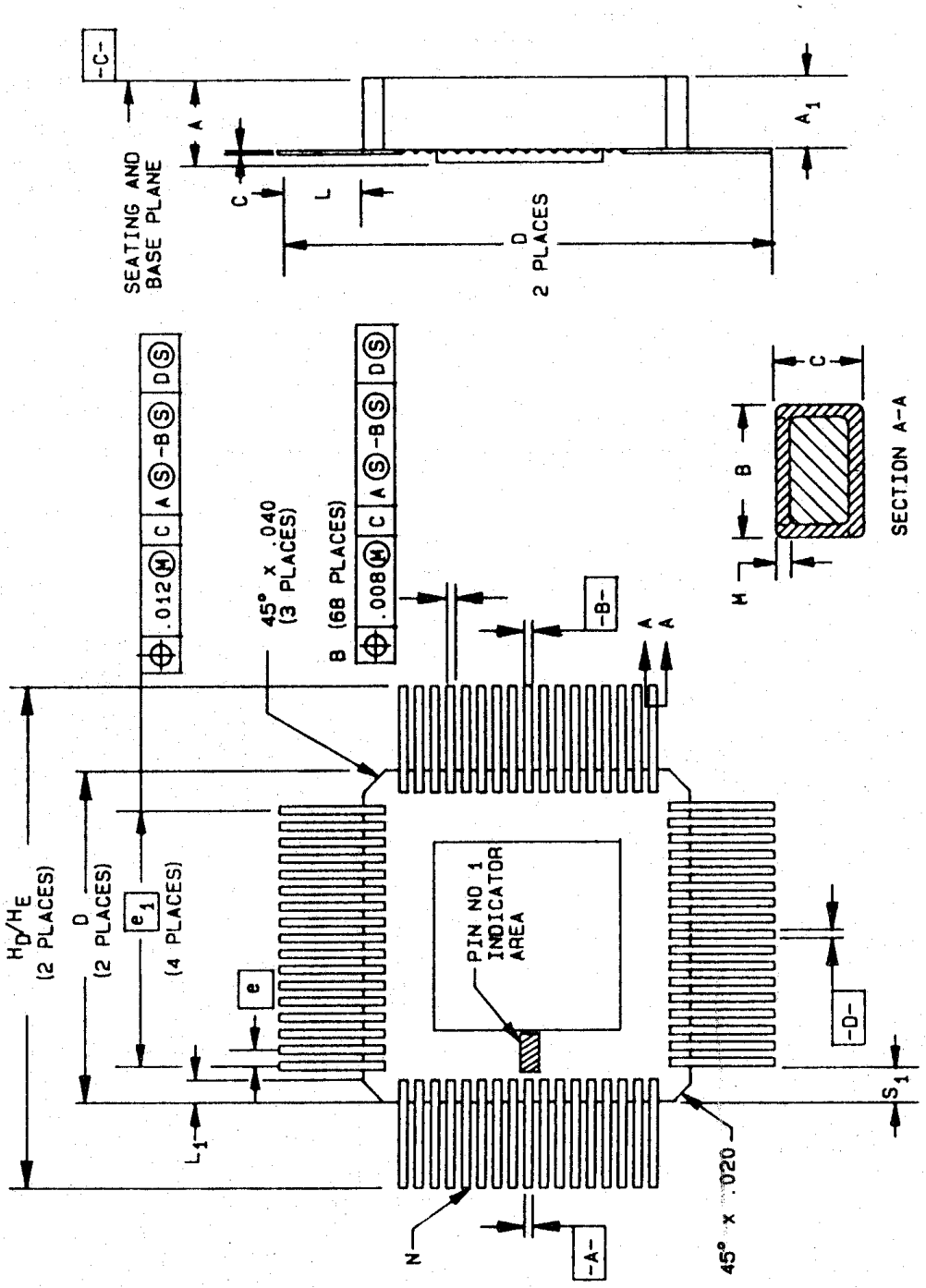


FIGURE 1. Case outline Y.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE **A**		5962-89534
		REVISION LEVEL B	SHEET 11

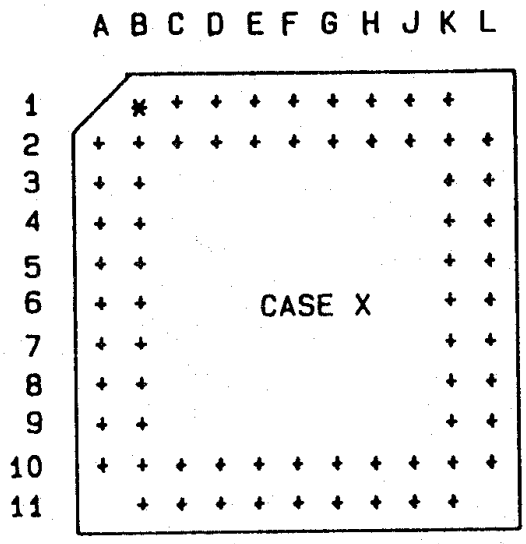
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.080	.115	2.03	2.92
A_1	.070	.090	1.78	2.29
B	.016	.021	0.41	0.53
C	.008	.012	0.20	0.30
D	.926	.970	23.52	24.64
e	.050 BSC		1.27 BSC	
e_1	.800 BSC		20.32 BSC	
H_D/H_E	1.640	1.870	41.66	47.50
L	.350	.450	8.89	11.43
L_1	.040	.060	1.02	1.52
M	---	.0015	---	0.038
N	68			
N_D/N_E	17			
S_1	.050	---	1.27	---

FIGURE 1. Case outline y - Continued.

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are for general information only.
3. Unless otherwise specified, tolerance for three place decimals is ±.005.
4. The index feature for terminal 1 identification, optical orientation, or handling purposes shall be within the shaded index areas shown on planes 1 and 2. Terminal 1 identification is optional on the surface closest to the seating plane.
5. Corner shapes (square notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
6. Dimension N: Number of terminals per package edge.
7. Dimensioning is in accordance with ANSI Y14.5M 1982.
8. Lead coplanarity shall be within .004 inch (0.10 mm) .050 inch (1.27 mm) from package body.
9. No overhang of the lead on the braze pad is allowed.
10. Dimensions B and C apply to base metal only. Dimension M applies to plating thickness.
11. The leads on this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars, carriers, etc.) are now shown on the drawing; however, when microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government are spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.

FIGURE 1. Case outline Y - Continued.



PIN SIDE VIEW
*PIN 1

Case outline X				
A2 - D9	B5 - D13	D10 - D24	H1 - D1	K7 - $\overline{ADS}$
A3 - D11	B6 - D15	D11 - D25	H2 - D0	K8 - $\overline{READY}$
A4 - D12	B7 - V	E1 - V_{CC}	H10 - D30	K9 - No connect
A5 - D14	B8 - D17	E2 - V_{CC}	H11 - D31	K10 - 386CLK2
A6 - V_{CC}	B9 - D19	E10 - D26	J1 - V_{SS}	K11 - 387CLK2
A7 - D16	B10 - D20	E11 - D27	J2 - V_{CC}	L2 - $\overline{ERROR}$
A8 - D18	B11 - D22	F1 - V_{CC}	J10 - V_{SS}	L3 - $\overline{READYO}$
A9 - V_{CC}	C1 - D7	F2 - V_{SS}	J11 - CKM	L4 - STEN
A10 - D21	C2 - D6	F10 - V_{CC}	K1 - PEREQ	L5 - V_{SS}
B1 - D8	C10 - D23	F11 - V_{SS}	K2 - BUSY	L6 - $\overline{NPSI}$
B2 - V_{SS}	C11 - V_{SS}	G1 - D3	K3 - Tie high	L7 - V_{CC}
B3 - D10	D1 - D5	G2 - D2	K4 - W/$\overline{R}$	L8 - $\overline{CMDO}$
B4 - V_{CC}	D2 - D4	G10 - D28	K5 - V_{CC}	L9 - Tie high
		G11 - D29	K6 - NPS2	L10 - RESETIN

FIGURE 2. Terminal connections.

Case outlines Y									
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
01	V_{SS}		18	D15		35	V_{SS}		52	V_{CC}
02	V_{CC}		19	V_{SS}		36	V_{CC}		53	V_{SS}
03	D4		20	V_{CC}		37	D28		54	NPS2
04	D5		21	V_{SS}		38	D29		55	$\overline{NPS1}$
05	D6		22	D16		39	V_{CC}		56	V_{SS}
06	D7		23	D17		40	D30		57	W/$\overline{R}$
07	D8		24	D18		41	D31		58	STEN
08	D9		25	D19		42	CKM		59	Tie high
09	D10		26	D20		43	386CLK2		60	$\overline{READYO}$
10	D11		27	D21		44	387CLK2		61	$\overline{BUSY}$
11	D12		28	D22		45	RESET IN		62	$\overline{ERROR}$
12	V_{SS}		29	D23		46	NC		63	PEREQ
13	V_{CC}		30	D24		47	Tie high		64	D0
14	D13		31	D25		48	$\overline{READY}$		65	D1
15	D14		32	V_{CC}		49	V_{SS}		66	D2
16	V_{SS}		33	D26		50	$\overline{CMDO}$		67	D3
17	V_{CC}		34	D27		51	$\overline{ADS}$		68	V_{CC}

FIGURE 2. Terminal connections - Continued.

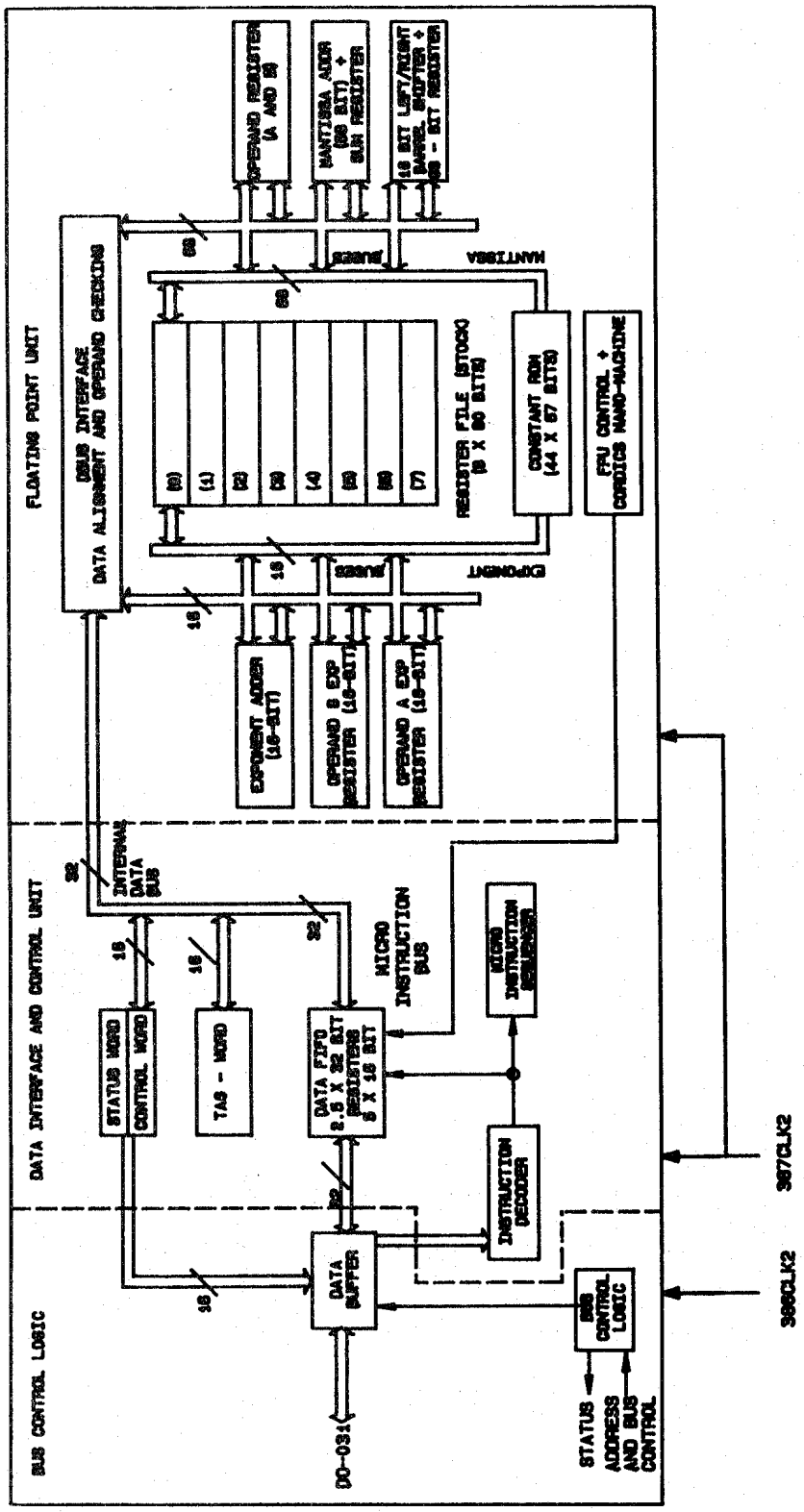
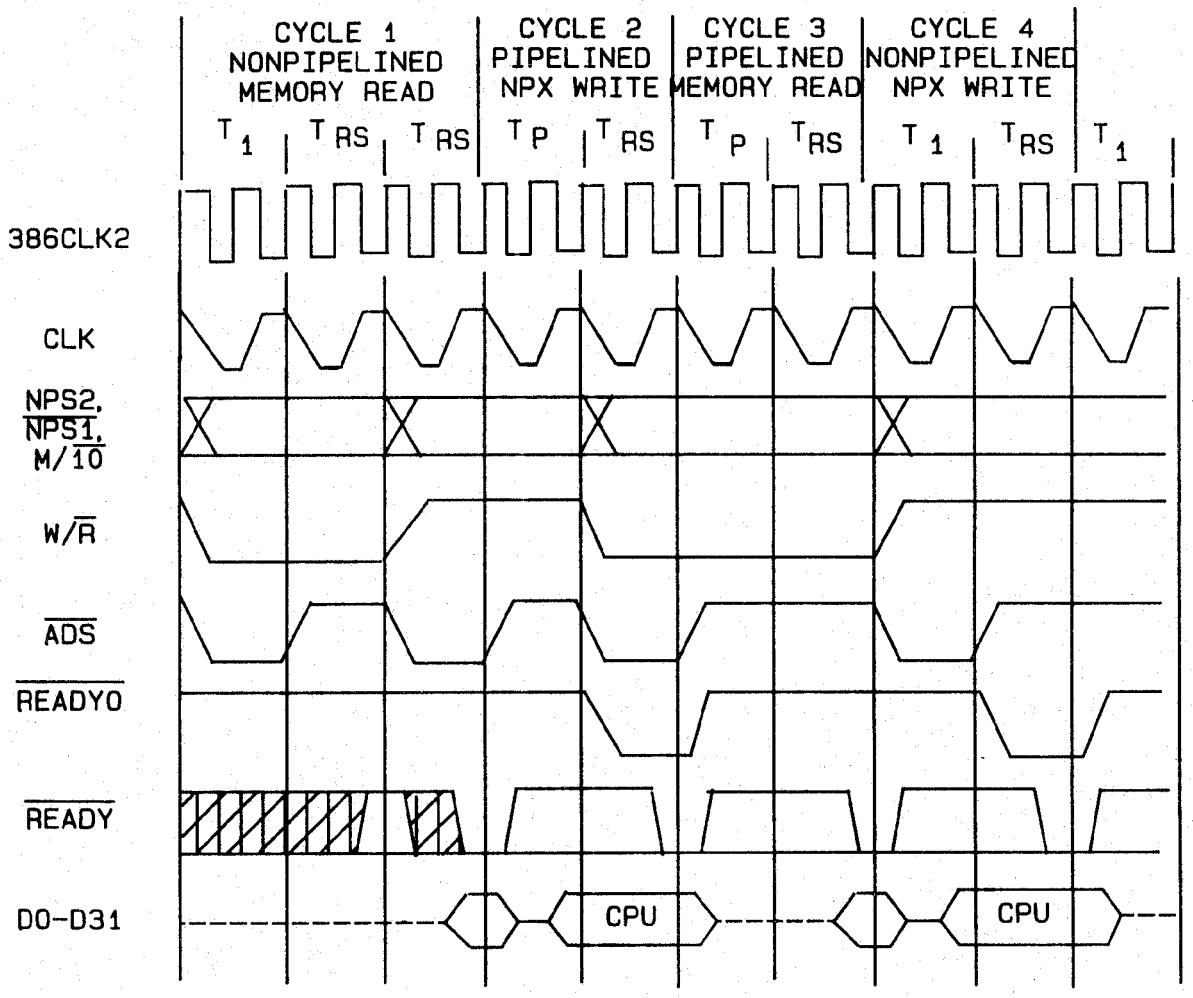


FIGURE 3. Functional block diagram.

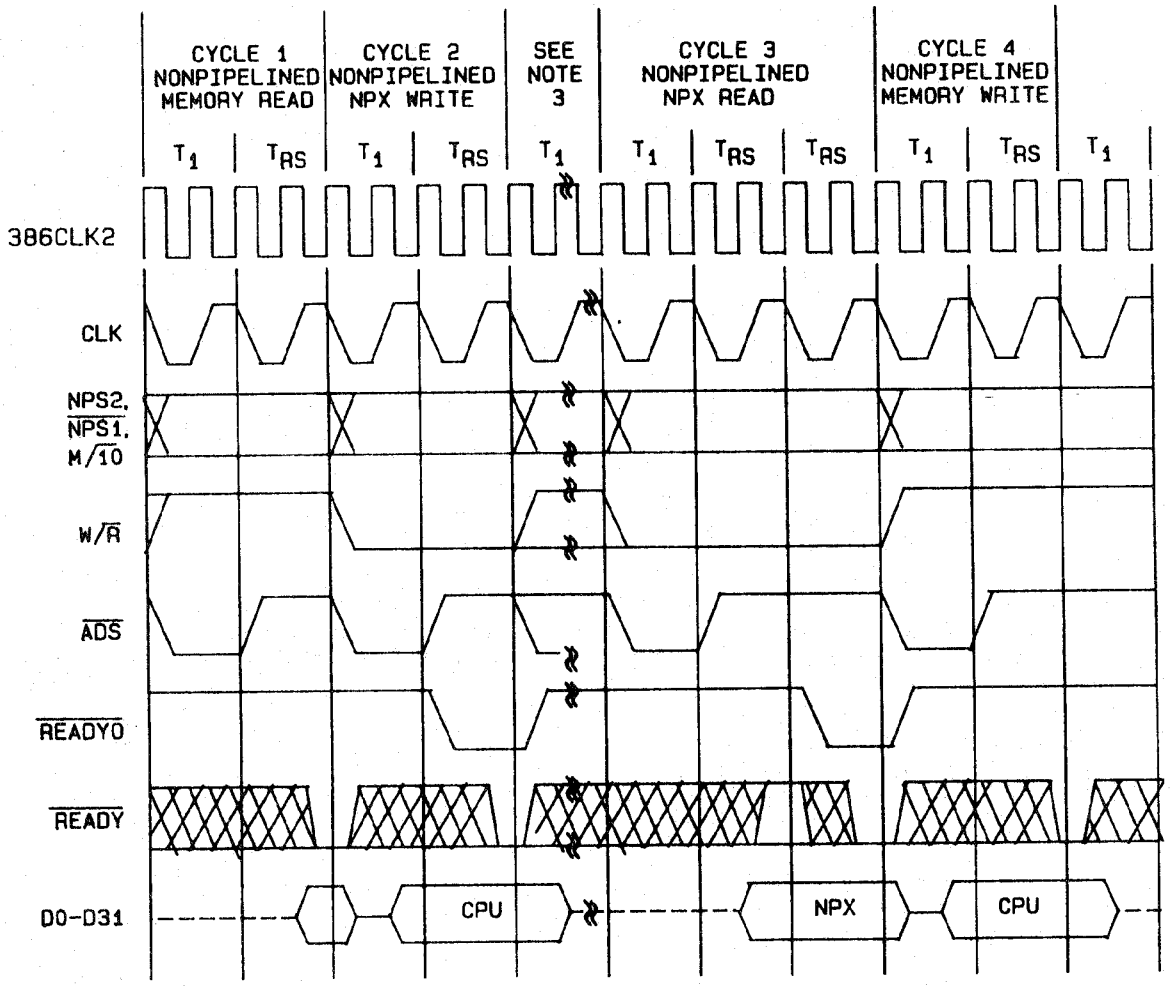
Fastest transitions to and from pipelined cycles



NOTES:
1. Cycle 1 through cycle 4 represent the operand transfer cycle for an instruction involving a transfer of two 32-bit loads in total.
2. The opcode write cycles and other overhead are not shown.
3. Note that the next cycle will be a pipelined cycle if both READY and ADS are sampled active at the end of a T_{RS} state of the current cycle.

FIGURE 4. Switching waveforms and test circuit.

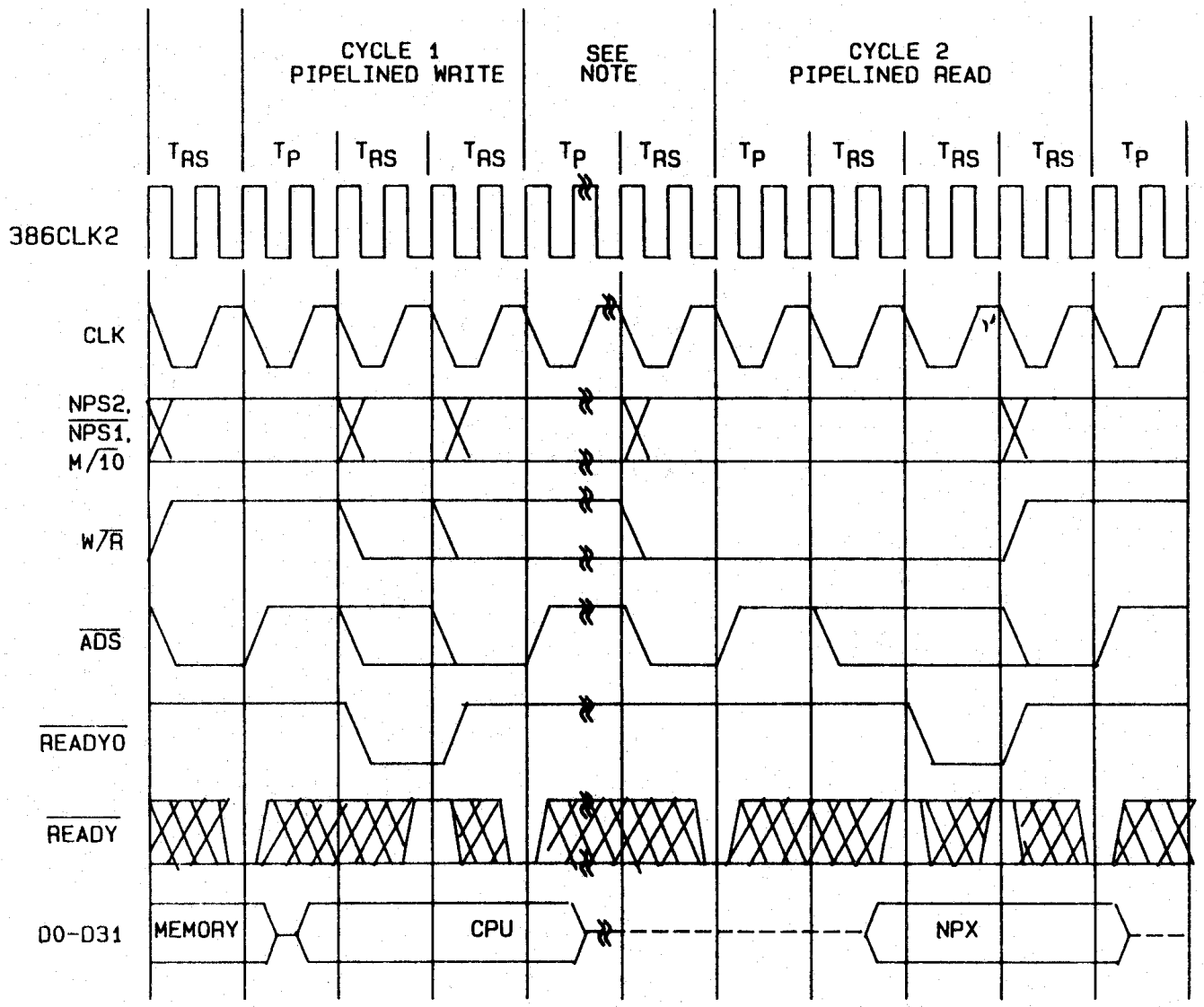
Nonpipelined read and write cycles



NOTES:
1. Cycles 1 and 2 represent part of the operand transfer cycle for instructions involving either 4-byte or 8-byte operand loads.
2. Cycles 3 and 4 represent part of the operand transfer cycle for a store operation.
3. Cycles 1 and 2 could repeat here or T_1 states for various non-operand transfer cycles and overhead.

FIGURE 4. Switching waveforms and test circuit - Continued.

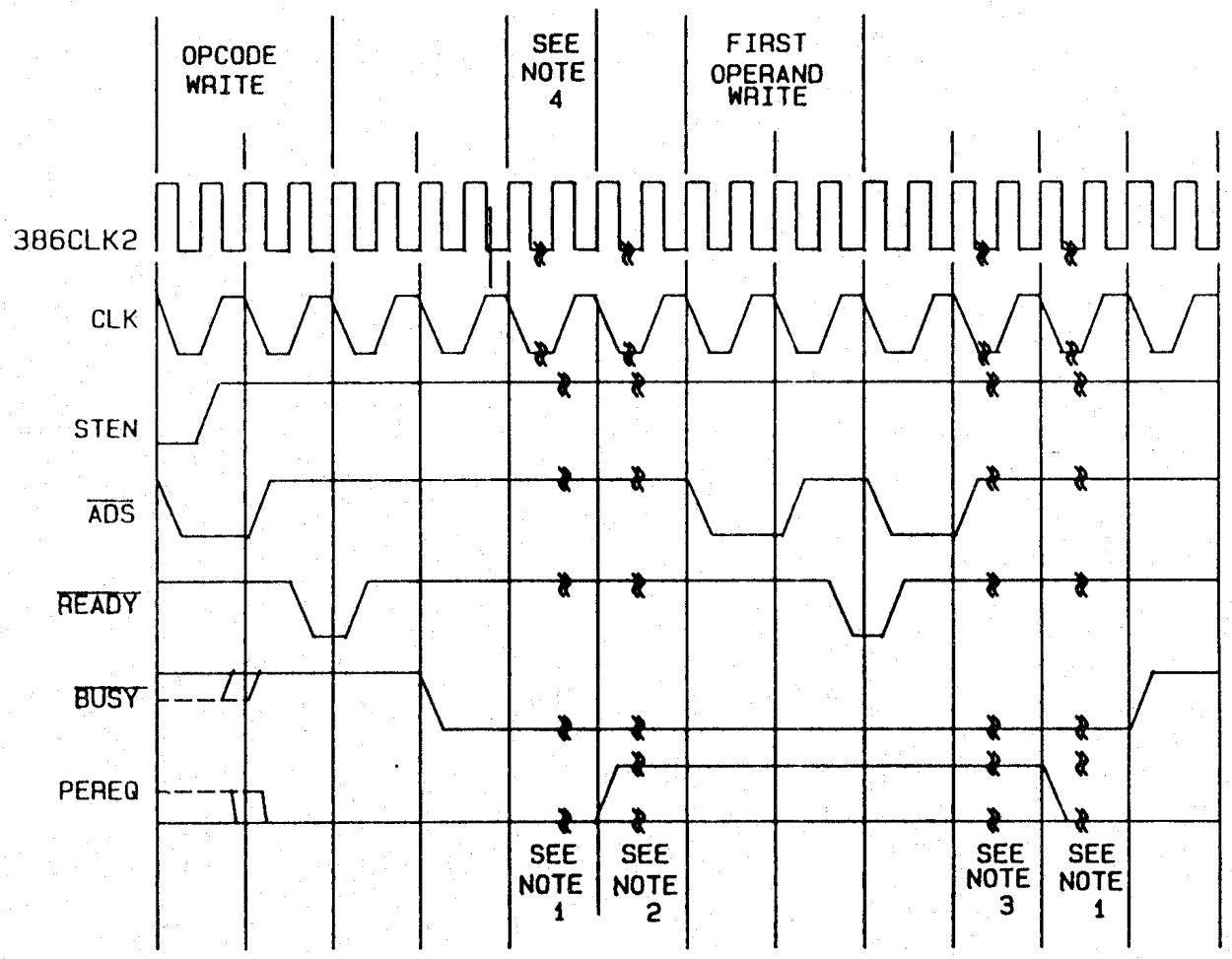
Pipelined cycles with wait states



NOTE: Cycles between operand write to the NPX and storing result.

FIGURE 4. Switching waveforms and test circuit - Continued.

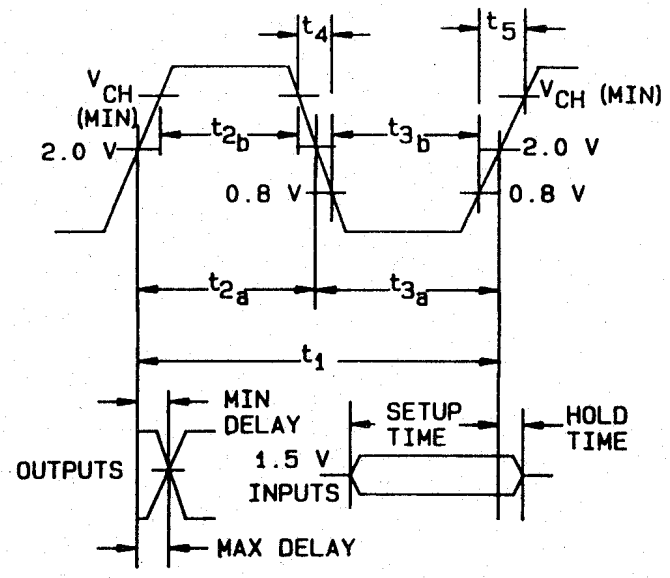
STEN, $\overline{BUSY}$ and PEREQ timing relationship



Notes:
1. Instruction dependent.
2. PEREQ is an asynchronous input to the 80386; it may not be asserted (instruction dependent).
3. More operand transfers.
4. Memory read (operand) cycle is not shown.

FIGURE 4. Switching waveforms and test circuit - Continued.

386CLK2/387CLK2 waveform and measurement points for input/output ac specifications



Test circuit

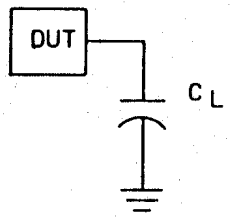
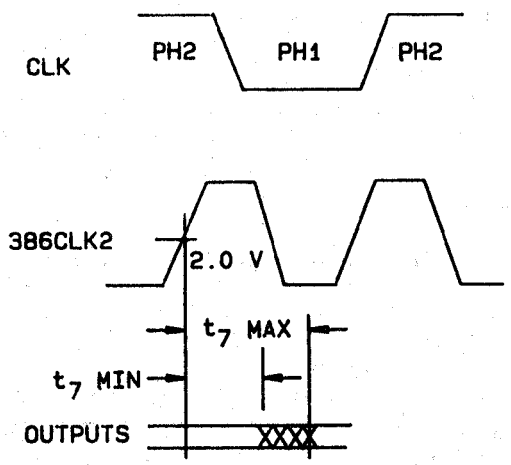


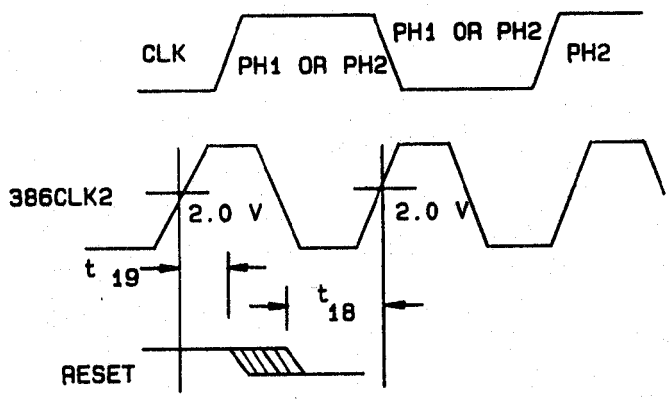
FIGURE 4. Switching waveforms and test circuit - Continued.

Output signals



NOTE: $\overline{\text{ERROR}}$ referenced to 387CLK2.

Reset signal



NOTE: The second internal processor phase following RESET high to low transition is PH2.

FIGURE 4. Switching waveforms and test circuit - Continued.

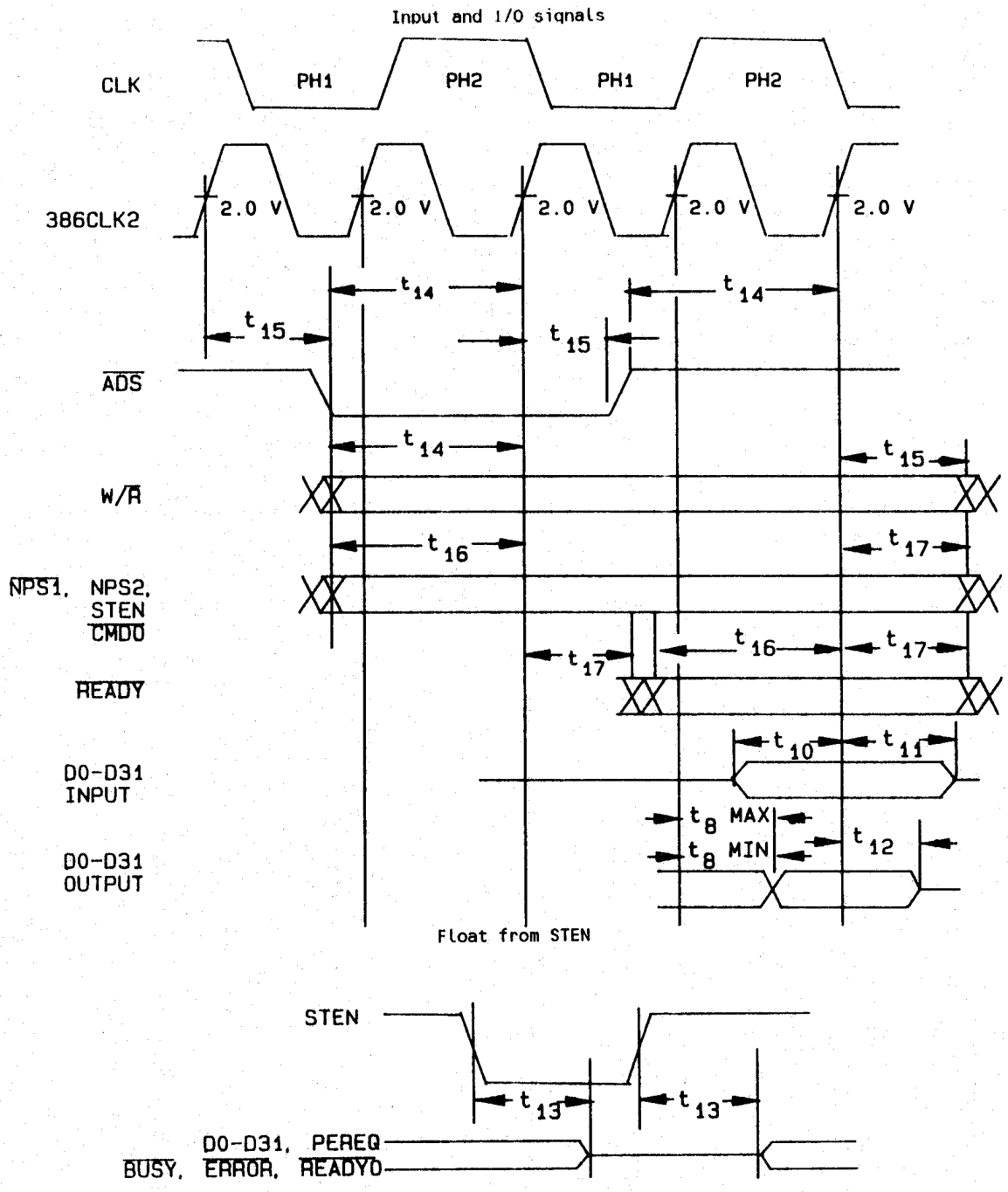
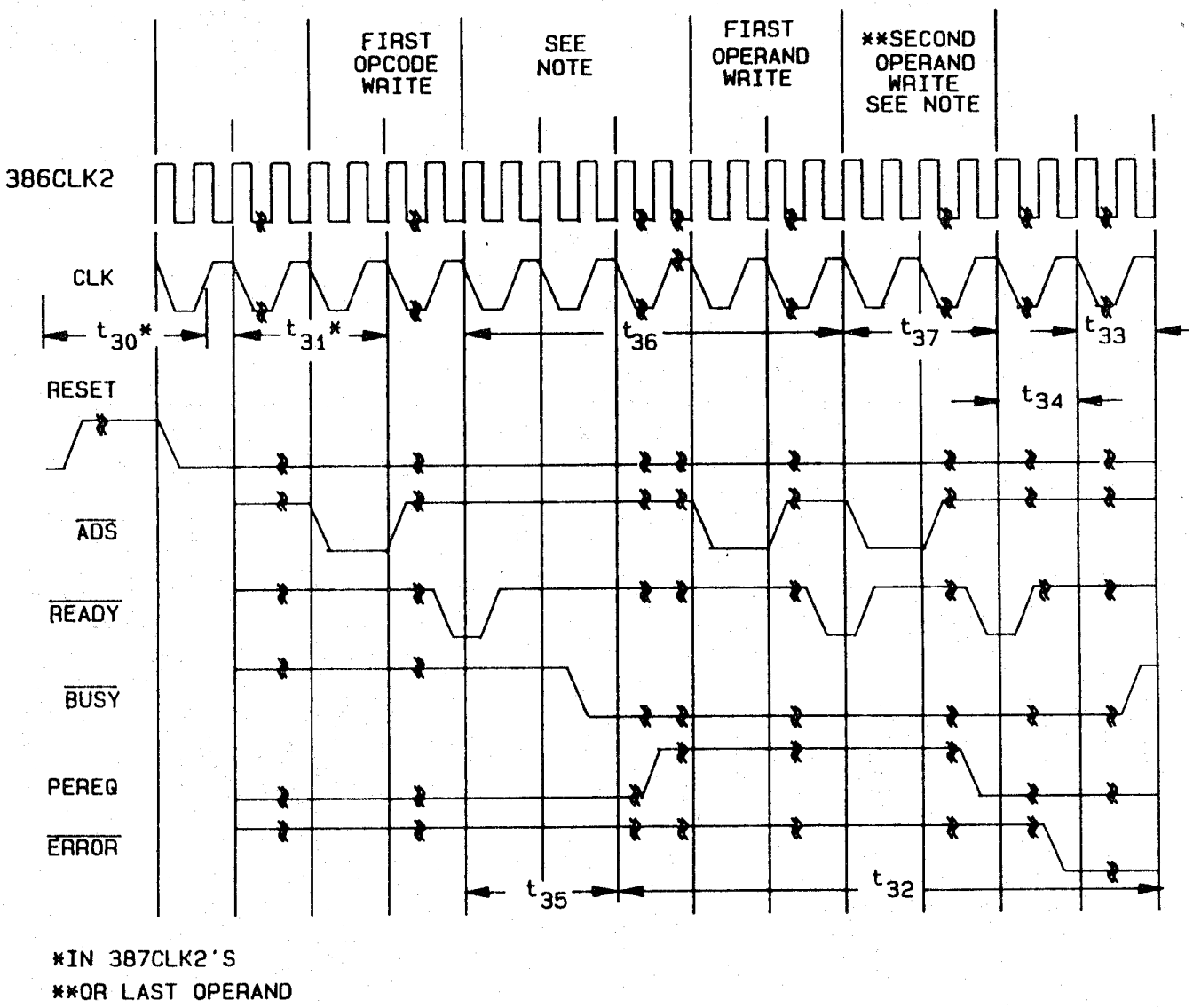


FIGURE 4. Switching waveforms and test circuit - Continued.

Other parameters



NOTE: Memory read (operand) cycle is not shown.

FIGURE 4. Switching waveforms and test circuit - Continued.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

3.12 PIN supersession information. The PIN supersession information shall be as specified in the appendix.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) $T_A = +125^\circ C$, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1, 7, 9	---	1, 7, 9
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group B end-point electrical parameters (see 4.4)	---	---	1, 2, 3, 7, 8, 9, 10, 11	---	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8, 10	---	2, 8, 10	---
Group D end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8, 10	2, 8, 10	2, 8, 10	2, 8, 10
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroup 1 and 7.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IO} measurement) shall be measured only for the initial test and after process and design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. For device class M, subgroups 7 and 8 tests shall include verification of the device functionality. These tests shall be maintained and available from the approved source of supply upon request. For device classes B and S, subgroups 7 and 8 tests shall include verification of the device functionality. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.5 Pin descriptions.

386CLK2	This input uses the 80386 CLK2 signal to time the bus control logic. Several other 80387 signals are referenced to the rising edge of this signal. When CKM = 1 (synchronous mode) this pin also clocks the data interface and control unit and the floating point unit of the 80387. This pin requires MOS level input. The signal on this pin is divided by two to produce the internal clock signal CLK.
387CLK2	When CKM = 0 (asynchronous mode) this pin provides the clock for the data interface and control unit and the floating point unit of the 80387. In this case, the ratio of the frequency of the 387CLK2 to the 386CLK2 must lie within the range 10:16 to 14:10. When CKM = 1 (synchronous mode) this pin is ignored; 386CLK2 is used instead for the data interface and control unit and the floating-point unit. This pin requires TTL-level input.
CKM	This pin is a strapping option. When it is strapped to V_{CC}, the 80387 operates in the asynchronous mode. These modes relate to clocking of the data interface and control unit and the floating point unit only; the bus control logic always operates synchronously with respect to the 80386.
RESETIN	A low to high transition on this pin causes the 80387 to terminate its present activity and to enter a dormant state. RESETIN must remain high for at least 40 387CLK2 periods. The high to low transitions of the RESETIN must be synchronous with 386CLK2, so that the phase of the internal clock of the bus control logic (which is the 386CLK2 divided by 2) is the same phase of the internal clock of the 80386. After RESETIN goes low, at least 50 387CLK2 periods must pass before the first NPX instruction is written to the 80387. This pin should be connected to the 80386 RESET pin. Status of other pins after a reset shall be as indicated follows:

Pin name	Pin value
READY, BUSY	high
PEREQ, ERROR	low
D31-D0	3-state

PEREQ — When active, the pin signals to the 80386 CPU that the 80387 is ready for data transfer to/from its data FIFO. When all data is written to or read from the data FIFO, PEREQ is deactivated. This signal always goes inactive before BUSY goes inactive. This signal is referenced to the 386CLK2. It should be connected to the 80386 PEREQ input. Refer to figure 3 for timing relationships between this and the BUSY and the ERROR pins.

BUSY — When active, the pin signal to the 80386 CPU that the 80387 is currently executing an instruction. This signal is referenced to the 386CLK2. It should be connected to the 80386 BUSY pin. Refer to figure 3 for timing relationships between this and the PEREQ and the ERROR pins.

ERROR — This pin reflects the ES bits of the status register. When active, it indicates that an unmasked exception has occurred (except that, immediately after a reset, it indicates to the 80386 that an 80387 is present in the system). This signal can be changed to inactive state only by the following instructions (without a preceding WAIT): FNINIT, FNCLEX, FNSTENV, and FNSAVE. This signal is referenced to 387CLK2. It should be connected to the 80386 ERROR pin. Refer to figure 3 for the timing relationships between this and the PEREQ and BUSY pins.

D31-D0 — These bidirectional pins are used to transfer data and opcodes between the 80386 and 80387. They are normally connected directly to the corresponding 80386 data pins. High state indicates a value on one. D0 is the least significant data bit. Timings are referenced to 386CLK2.

W/R — This signal indicates to the 80387 whether the 80386 bus cycle in progress is a read or a write cycle. This pin should be connected directly to the 80386 W/R pin. High indicates a write cycle; low, a read cycle. This input is ignored if any of the signals STEN, NPS1, or NPS2 is inactive. Setup and hold times are referenced to 386CLK2.

ADS — This input, in conjunction with the READY input indicates when the 80387 bus control logic may sample W/R and the chip select signals. Setup and hold times are referenced to 386CLK2. This pin should be connected to the 80386 ADS pin.

READY — This input indicates to the 80387 when an 80386 bus cycle is to be terminated. It is used by the bus control logic to trace bus activities. Bus cycles can be extended indefinitely until terminated by READY. This input should be connected to the same signal that drives the 80386 READY input. Setup and hold times are referenced to 386CLK2.

READYO	This pin is activated at such a time that write cycles are terminated after two clocks and read cycles after three clocks. In configurations where no extra wait states are required, it can be used to directly drive the 80386 READY input. This pin is activated only during bus cycles that select the 80387. This signal is referenced to 386CLK2.
STEN	This pin serves as a chip select for the 80387. When inactive, this pin forces BUSY, PEREQ, ERROR, and READYO outputs into floating state. D31-D0 are normally floating and leave floating state only if STEN is active and additional conditions are met. STEN also causes the chip to recognize its other chip select inputs. STEN makes it easier to do on board testing (using the overdrive method) of other chips in systems containing the 80387. STEN should be pulled up with a resistor so that it can be pulled down when testing. In boards that do not use on board testing, STEN should be connected to V_{CC}. Setup and hold times as NPS1, NPS2, and CMD0 (i.e., if STEN changes state during an 80387 bus cycle, it should change state during the same CLK period as the NPS1, NPS2, and CMD0 signals).
NPS1	When active (along with STEN and NPS2 in the first period of an 80386 bus cycle), this signal indicates that the purpose of the bus cycle is to communicate with the 80387. This pin should be connected directly to the 80386 M/IO pin, so that the 80387 is selected only when the 80386 performs I/O cycles. Setup and hold times are referenced to 386CLK2.
NPS2	When active (along with STEN and NPS1 in the first period of an 80386 bus cycle), this signal indicates that the purpose of the bus cycle is to communicate with the 80387. This pin should be connected directly to the 80386 A31 pin, so that the 80387 is selected only when the 80386 uses one of the I/O addresses reserved for the 80387 (800000F8 or 800000FC). Setup and hold times are referenced to 386CLK2.
CMD0	During a write cycle, this signal indicates whether an opcode (CMD0 active) or data (CMD0 inactive) is being sent to the 80387. During a read cycle, it indicates whether the control or the status register (CMD0 active) or the data register (CMD0 inactive) is being read. CMD0 should be connected directly to the A2 output of the 80386. Setup and hold times are referenced to 386CLK2.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY (Part 1 or 2)	QPL-38510	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

APPENDIX

PIN SUPERSESSION INFORMATION

10. SCOPE

10.1 Scope. This appendix contains the PIN supersession information to support the one part - one part number system. For new system designs, after the date of this document the NEW PIN shall be used in lieu of the OLD PIN. For existing system designs prior to the date of this document the NEW PIN can be used in lieu of the OLD PIN. This is a mandatory part of the document. The information contained herein is intended for compliance. The PIN supersession data shall be as follows:

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. SUPERSESSION DATA

NEW PIN	OLD PIN
5962-8953401MXX	5962-8953401XX
5962-8953401MYX	5962-8953401YX
5962-8953402MXX	5962-8953402XX
5962-8953402MYX	5962-8953402YX
5962-8953403MXX	5962-8953403XX
5962-8953403MYX	5962-8953403YX

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 91-08-29

Approved sources of supply for SMD 5962-89534 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8953401MXX	34649	MG80387-16
5962-8953401MYX	34649	MQ80387-16
5962-8953402MXX	34649	MG80387-20
5962-8953402MYX	34649	MQ80387-20
5962-8953403MXX	34649	MG80387-25
5962-8953403MYX	34649	MQ80387-25

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051 Point of contact: 5000 W. Williams Field Road Chandler, AZ 85224

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.