REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. - jak	03-06-11	Thomas M. Hess
B	Update test condition for high level output voltage (V_{OH}) and low level output voltage (V_{OL}) in table I. Update boilerplate paragraphs to MIL-PRF-38535 requirement. - jak	10-02-12	Thomas M. Hess

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS OF SHEETS															
REV	B	B	B	B	B	B	B	B	B	B	B	B		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

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DRAWING APPROVAL DATE
89-03-07

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL D-TYPE FLIP-FLOP WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89557**

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT564	Octal D-type flip-flop with three state outputs, TTL compatible inputs

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC}) ..... -0.5 V dc to + 6.0 V dc
DC input voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK}) ..... ±20 mA
DC output current (per pin) (I_{OUT}) ..... ±50 mA
DC V_{CC} or GND current ..... ±100 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW
Lead temperature (soldering, 10 seconds) ..... +260°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C 3/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to ground.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

1.4 Recommended operating conditions. 1/

Supply voltage range (V_{CC}) ..... +4.5 V dc minimum to 5.5 V dc maximum
Input voltage range (V_{IN}) ..... 0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... 0.0 V dc to V_{CC}
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise and fall rate ($\Delta t/\Delta V$) maximum:
  V_{CC} = 4.5 V or V_{CC} = 5.5 V ..... 8 ns/V
Minimum setup time, Dn to CP (t_s):
  T_C = +25°C, V_{CC} = 4.5 V ..... 3.5 ns
  T_C = -55°C to +125°C, V_{CC} = 4.5 V ..... 3.5 ns
Minimum hold time, Dn to CP (t_h):
  T_C = +25°C, V_{CC} = 4.5 V ..... 2.5 ns
  T_C = -55°C to +125°C, V_{CC} = 4.5 V ..... 2.5 ns
Minimum pulse width, CP (t_w):
  T_C = +25°C, V_{CC} = 4.5 V ..... 5.0 ns
  T_C = -55°C to +125°C, V_{CC} = 4.5 V ..... 5.0 ns
Maximum frequency, CP (f_{MAX}):
  T_C = +25°C, V_{CC} = 4.5 V ..... 85 MHz
  T_C = -55°C to +125°C, V_{CC} = 4.5 V ..... 65 MHz

2 APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Unless otherwise specified, all voltages are referenced to ground.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 and QML-38535 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Limits 2/		Unit
					Min	Max	
High-level output voltage 3006	V_{OH} 3/	V_{IH} = 2.0 V or V_{IL} = 0.8 V I_{OH} = -50 µA	V_{CC} = 4.5 V	1, 2, 3	4.4		V
			V_{CC} = 5.5 V		5.4		
		V_{IH} = 2.0 V or V_{IL} = 0.8 V I_{OH} = -24 mA	V_{CC} = 4.5 V		3.7		
			V_{CC} = 5.5 V		4.7		
		V_{IH} = 2.0 V or V_{IL} = 0.8 V I_{OH} = -50 mA	V_{CC} = 5.5 V		3.85		
Low-level output voltage 3007	V_{OL} 3/	V_{IH} = 2.0 V or V_{IL} = 0.8 V I_{OL} = 50 µA	V_{CC} = 4.5 V	1, 2, 3		0.1	V
			V_{CC} = 5.5 V			0.1	
		V_{IH} = 2.0 V or V_{IL} = 0.8 V I_{OL} = 24 mA	V_{CC} = 4.5 V			0.5	
			V_{CC} = 5.5 V			0.5	
		V_{IH} = 2.0 V or V_{IL} = 0.8 V I_{OL} = 50 mA	V_{CC} = 5.5 V			1.65	
High-level input voltage	V_{IH} 4/		V_{CC} = 4.5 V	1, 2, 3	2.0		V
			V_{CC} = 5.5 V		2.0		
Low-level input voltage	V_{IL} 4/		V_{CC} = 4.5 V	1, 2, 3		0.8	V
			V_{CC} = 5.5 V			0.8	
Input leakage current low 3009	I_{IL}	V_{IN} = 0.0 V	V_{CC} = 5.5 V	1, 2, 3		-1.0	µA
Input leakage current high 3010	I_{IH}	V_{IN} = 5.5 V	V_{CC} = 5.5 V	1, 2, 3		1.0	
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 5/	V_{CC} = 5.5 V For input under test, $V_{IN} = V_{CC}$ - 2.1 V For all other inputs, $V_{IN} = V_{CC}$ or GND		1, 2, 3		1.6	mA
Quiescent supply current 3005	I_{CCH}	$V_{IN} = V_{CC}$ or GND V_{CC} = 5.5 V I_{OUT} = 0.0 mA		1, 2, 3		160	µA
	I_{CCL}					160	
	I_{CCZ}					160	
Three-state output leakage current high 3021	I_{OZH}	$V_{IN} = V_{CC}$ or GND V_{CC} = 5.5 V V_{OUT} = 5.5 V or 0.0 V		1, 2, 3		10.0	µA
Three-state output leakage current low 3020	I_{OZL}					-10.0	
Input capacitance 3012	C_{IN}	See 4.3.1c		4		8.0	pF
Power dissipation capacitance	C_{PD} 6/	See 4.3.1c		4		60.0	pF
Functional tests 3014		Tested at V_{CC} = 4.5 V and repeated at V_{CC} = 5.5 V, see 4.3.1d		7, 8	L	H	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits 2/		Unit
				Min	Max	
Propagation delay time, CP to On 3003	t_{PHL} 7/	V_{CC} = 4.5 V C_L = 50 pF R_L = 500Ω See figure 4	9	1.0	9.5	ns
			10, 11	1.0	11.5	
	t_{PLH} 7/		9	1.0	10.5	
			10, 11	1.0	12.5	
Propagation delay time, output enable, $\overline{OE}$ to On 3003	t_{PZH} 7/		9	1.0	9.0	
			10, 11	1.0	10.5	
	t_{PZL} 7/		9	1.0	9.0	
			10, 11	1.0	10.5	
Propagation delay time, output disable, $\overline{OE}$ to On 3003	t_{PHZ} 7/		9	1.0	10.5	
			10, 11	1.0	12.5	
	t_{PLZ} 7/		9	1.0	8.0	
			10, 11	1.0	9.5	

1/ For tests not listed in the referenced MIL-STD-883 (e.g. C_{PD}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

3/ V_{OH} and V_{OL} shall be tested at V_{CC} = 4.5 V. V_{OH} and V_{OL} are guaranteed, if not tested, for V_{CC} = 5.5 V. Limits shown apply to operation at V_{CC} = 5.0 V ±0.5 V. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum.

4/ V_{IH} and V_{IL} tests are not required, and shall be applied as forcing functions for V_{OH} and V_{OL} tests.

5/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ - 2.1 V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limits are equal to the number of inputs at a high TTL input level times 1.6 mA; and the preferred method and limits are guaranteed.

6/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption, $P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$. The dynamic current consumption, $I_S = (C_{PD} + C_L)V_{CC}f + I_{CC} + n \times d \times \Delta I_{CC}$.
For both P_D and I_S, n is the number of device inputs at TTL levels, f is the frequency of the input signal, and d is the duty cycle of the input signal.

7/ AC limits at V_{CC} = 5.5 V are equal to limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. The minimum ac limits are guaranteed for V_{CC} = 5.5 V by guardbanding the V_{CC} = 4.5 V limits to 1.5 ns minimum.

Device type	01
Case outlines	R, S, and 2
Terminal number	Terminal symbol
1	$\overline{OE}$
2	D0
3	D1
4	D2
5	D3
6	D4
7	D5
8	D6
9	D7
10	GND
11	CP
12	$\overline{O7}$
13	$\overline{O6}$
14	$\overline{O5}$
15	$\overline{O4}$
16	$\overline{O3}$
17	$\overline{O2}$
18	$\overline{O1}$
19	$\overline{O0}$
20	V_{CC}

FIGURE 1. Terminal connections.

Inputs			Outputs	Function
$\overline{OE}$	CP	Dn	$\overline{On}$	
H	H	L	Z	Hold
H	H	H	Z	Hold
H	↑	L	Z	Load
H	↑	H	Z	Load
L	↑	L	H	Data available
L	↑	H	L	Data available
L	H	L	NC	No Change in data
L	H	H	NC	No change in data

H = High voltage level
L = Low voltage level
Z = High impedance
NC = No change
↑ = Low to high transition of the clock

FIGURE 2. Truth table.

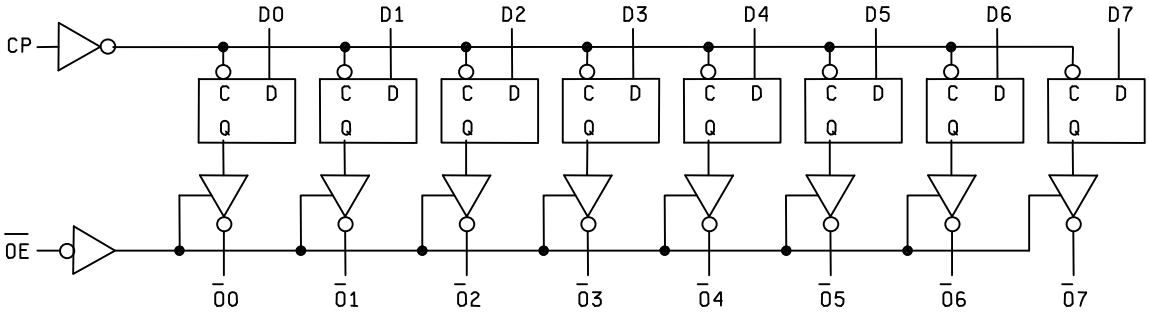


FIGURE 3. Logic diagram.

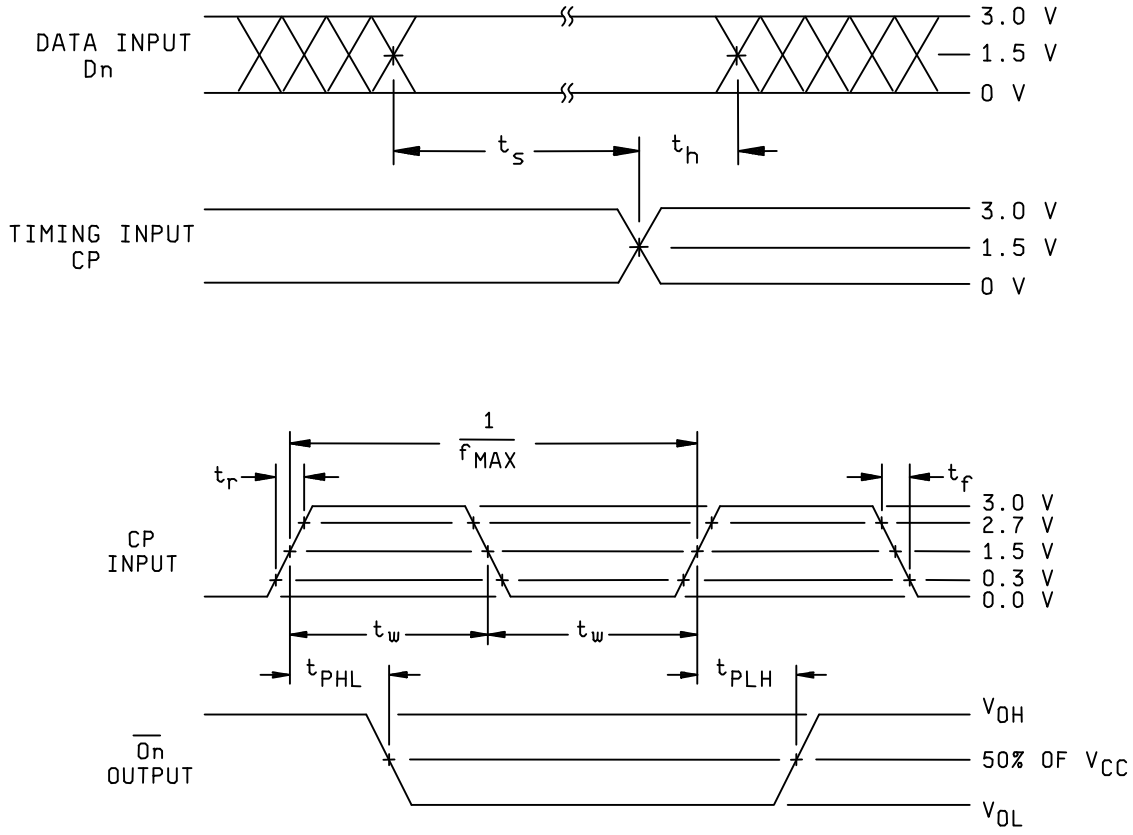
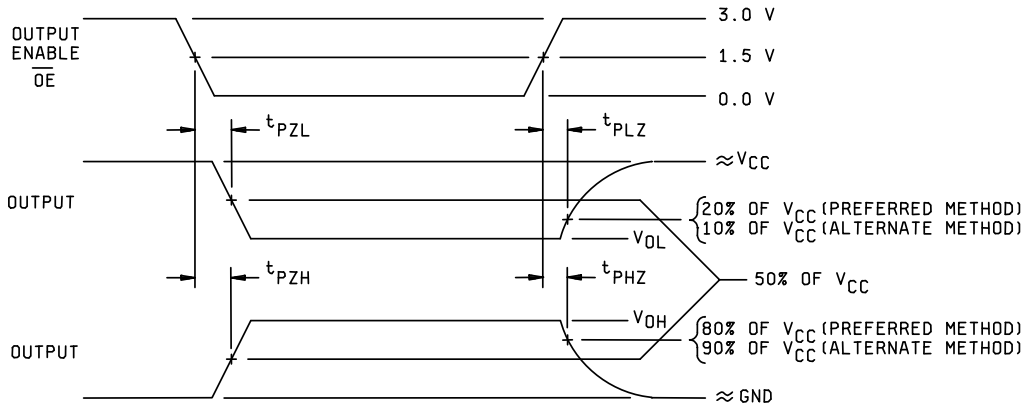
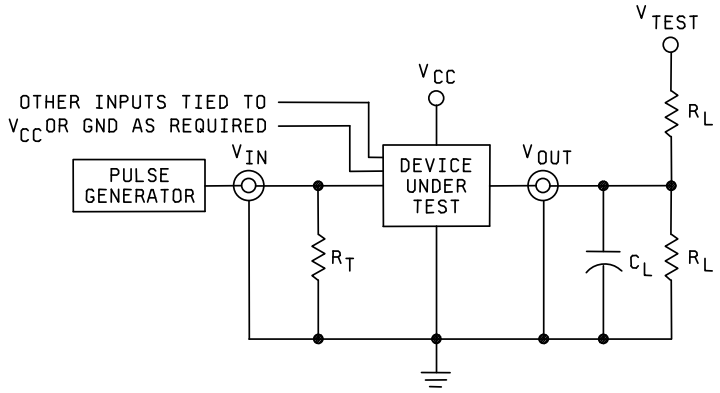


FIGURE 4. Switching waveforms and test circuit.





NOTES:

1. Preferred method:
   When measuring t_{PHZ} and t_{PZH}: V_{TEST} = GND
   When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 2 X V_{CC}
   When measuring t_{PLH} and t_{PHL}: V_{TEST} = open
   Alternate method:
   When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 2 X V_{CC}
   When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}: V_{TEST} = open
2. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
3. R_T = 50Ω or equivalent. R_L = 500Ω or equivalent.
4. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 3 ns; t_f ≤ 3 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
6. Outputs are measured one at a time with one output per measurement.

FIGURE 4. Switching waveforms and test circuit - Continued

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{PD} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Test all applicable pins on 5 devices with zero failures.

d. Subgroup 7 and 8 shall verify the truth table as specified in figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

1/ PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-02-12

Approved sources of supply for SMD 5962-89557 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8955701RA	0C7V7	54ACT564DMQB
5962-8955701SA	0C7V7	54ACT564FMQB
5962-89557012A	0C7V7	54ACT564LMQB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051