| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Update the boilerplate to current requirements as specified in MIL-PRF-38535. Editorial changes throughout. – jak | 06-11-27 | Thomas M. Hess |

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | A | A | A | A | A | A | A | A | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | | | | | | | | | | | | |

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| REV STATUS | REV | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | | |

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DRAWING APPROVAL DATE
94-06-01

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**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

**DEFENSE SUPPLY CENTER COLUMBUS**
**COLUMBUS, OHIO 43218-3990**
**http://www.dscc.dla.mil**

# MICROCIRCUIT, DIGITAL, ADVANCED CMOS, PROGRAMMABLE VIDEO SYNC GENERATOR, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

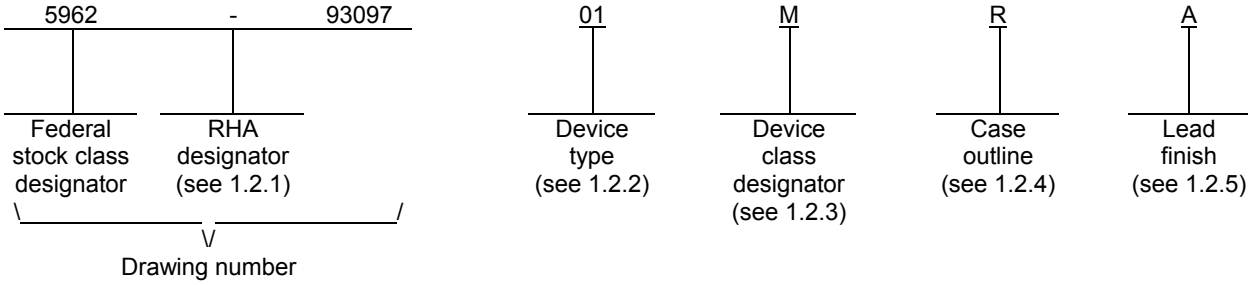
| SIZE | CAGE CODE | |
|---|---|---|
| **A** | **67268** | **5962-93097** |

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54ACT715 | Programmable video sync generator, TTL compatible inputs |
| 02 1/ | 54ACT715-R | Programmable video sync generator, TTL compatible inputs |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| R | GDIP1-T20 or CDIP2-T20 | 20 | Dual-in-line |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Device type 02 is the same as device type 01 in all respects except that device type 02 is mask programmed to default to a clock enable state.

1.3 Absolute maximum ratings. 1/ 2/ 3/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | -0.5 V dc to +7.0 V dc |
| DC input voltage ($V_{IN}$) | -0.5 V dc to $V_{CC}$ + 0.5 V dc |
| DC output voltage range ($V_{OUT}$) | -0.5 V dc to $V_{CC}$ + 0.5 V dc |
| DC input clamp current ($I_{IK}$) ($V_{IN}$ = -0.5 V and $V_{CC}$ + 0.5 V) | ±20 mA |
| DC output clamp current ($I_{OK}$) ($V_{OUT}$ = -0.5 V and $V_{CC}$ + 0.5 V) | ±20 mA |
| DC output source or sink current ($I_{OUT}$) | ±15 mA |
| DC $V_{CC}$ or GND current ($I_{CC}$, $I_{GND}$) (per output pin) | ±20 mA |
| Storage temperature range ($T_{STG}$) | -65°C to +150°C |
| Maximum power dissipation ($P_D$) | 500 mW |
| Lead temperature (soldering, 10 seconds) | +300°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$) | See MIL-STD-1835 |
| Junction temperature ($T_J$) | +175°C |

1.4 Recommended operating conditions. 2/ 3/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | +4.5 V dc to +5.5 V dc |
| Input voltage range ($V_{IN}$) | +0.0 V dc to $V_{CC}$ |
| Output voltage range ($V_{OUT}$) | +0.0 V dc to $V_{CC}$ |
| Maximum low level input voltage ($V_{IL}$) | 0.8 V |
| Minimum high level input voltage ($V_{IH}$) | 2.0 V |
| Case operating temperature range ($T_C$) | -55°C to +125°C |
| Minimum input edge rate ($\Delta V/\Delta t$): | |
| (from $V_{IN}$ = 0.8 V to 2.0 V, 2.0 V to 0.8 V) | 125 mV/ns |
| Maximum high level output current ($I_{OH}$) | -8 mA |
| Maximum low level output current ($I_{OL}$) | +8 mA |

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified $V_{CC}$ range and case temperature range of -55°C to +125°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at http://www.eia.org or from the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Register descriptions. The register descriptions shall be as specified on figure 3.

3.2.5 Signal specifications. The signal specifications shall be as specified on figure 4.

3.2.6 Addressing logic. The addressing logic shall be as specified on figure 5

3.2.7 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 40 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | Device type | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| High level output voltage 3006 | $V_{OH1}$ | For all inputs affecting output under test $V_{IN}$ = 2.0 V or 0.8 V For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH}$ = -50 µA | All | 4.5 V | 1, 2, 3 | 4.40 | | V |
| | | | | 5.5 V | | 5.40 | | |
| | $V_{OH2}$ | For all inputs affecting output under test $V_{IN}$ = 2.0 V or 0.8 V For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH}$ = -8 mA | All | 4.5 V | 1 | 3.86 | | |
| | | | | 5.5 V | | 4.86 | | |
| | | | | 4.5 V | 2, 3 | 3.70 | | |
| | | | | 5.5 V | | 4.70 | | |
| | $V_{OH3}$ 4/ | For all inputs affecting output under test $V_{IN}$ = 5.5 V or 0.0 V For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH}$ = -32 mA | All | 5.5 V | 1, 2, 3 | 3.85 | | |
| Low level output voltage 3007 | $V_{OL1}$ | For all inputs affecting output under test $V_{IN}$ = 2.0 V or 0.8 V For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL}$ = 50 µA | All | 4.5 V | 1, 2, 3 | | 0.10 | V |
| | | | | 5.5 V | | | 0.10 | |
| | $V_{OL2}$ | For all inputs affecting output under test $V_{IN}$ = 2.0 V or 0.8 V For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL}$ = 8 mA | All | 4.5 V | 1 | | 0.36 | |
| | | | | 5.5 V | | | 0.36 | |
| | | | | 4.5 V | 2, 3 | | 0.50 | |
| | | | | 5.5 V | | | 0.50 | |
| | $V_{OL3}$ 4/ | For all inputs affecting output under test $V_{IN}$ = 5.5 V or 0.0 V For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL}$ = 32 mA | All | 5.5 V | 1, 2, 3 | | 1.65 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | Device type | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Positive input clamp voltage 3022 | $V_{IC+}$ | For input under test $I_{IN}$ = 18 mA | All | 4.5 V | 1, 2, 3 | | 5.7 | V |
| Negative input clamp voltage 3022 | $V_{IC-}$ | For input under test $I_{IN}$ = -18 mA | All | 4.5 V | 1, 2, 3 | | -1.2 | V |
| Input current high 3010 | $I_{IH}$ | For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND | All | 5.5 V | 1 | | 0.1 | µA |
| | | | | | 2, 3 | | 1.0 | |
| Input current low 3009 | $I_{IL}$ | For input under test, $V_{IN}$ = GND For all other inputs, $V_{IN} = V_{CC}$ or GND | All | 5.5 V | 1 | | -0.1 | µA |
| | | | | | 2, 3 | | -1.0 | |
| Quiescent supply current delta, TTL input levels 3005 | $\Delta I_{CC}$ 5/ | For input under test, $V_{IN} = V_{CC}$ - 2.1 V For all other inputs, $V_{IN} = V_{CC}$ or GND | All | 5.5 V | 1 | | 1.0 | mA |
| | | | | | 2, 3 | | 1.6 | |
| Quiescent supply current, outputs high 3005 | $I_{CCH}$ | For all inputs, $V_{IN} = V_{CC}$ or GND | All | 5.5 V | 1 | | 8.0 | µA |
| | | | | | 2, 3 | | 160.0 | |
| Quiescent supply current, outputs low 3005 | $I_{CCL}$ | | All | 5.5 V | 1 | | 8.0 | µA |
| | | | | | 2, 3 | | 160.0 | |
| Input capacitance 3012 | $C_{IN}$ | See 4.4.1d $T_C$ = +25°C | All | 5.0 V | 4 | | 10.0 | pF |
| Power dissipation capacitance | $C_{PD}$ 6/ | See 4.4.1d $T_C$ = +25°C | All | 5.0 V | 4 | | 20.0 | pF |
| Maximum interlaced frequency (HMAX/2 is odd) | $f_{MAX1}$ 7/ | $C_L$ = 50 pF minimum $R_L$ = 500Ω | All | 4.5 V | 9 | 170 | | MHz |
| | | | | | 10, 11 | 130 | | |
| Maximum noninterlaced frequency (HMAX/2 is even) | $f_{MAX2}$ 7/ | $C_L$ = 50 pF minimum $R_L$ = 500Ω | All | 4.5 V | 9 | 190 | | MHz |
| | | | | | 10, 11 | 145 | | |
| Propagation delay time, CLOCK to any output 3003 | $t_{PLH1}$, $t_{PHL1}$ 8/ | $C_L$ = 50 pF minimum $R_L$ = 500Ω See figure 6 | All | 4.5 V | 9 | 3.5 | 16.5 | ns |
| | | | | | 10, 11 | 3.5 | 19.5 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | Device type | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Propagation delay time, CLOCK to ODD/EVEN, (scan mode) 3003 | $t_{PLH2}$, $t_{PHL2}$ 8/ | $C_L$ = 50 pF minimum $R_L$ = 500Ω See figure 6 | All | 4.5 V | 9 | 3.5 | 17.0 | ns |
| | | | | | 10, 11 | 3.5 | 22.0 | |
| Propagation delay time, LOAD to any output 3003 | $t_{PLH3}$, $t_{PHL3}$ 8/ | | All | 4.5 V | 9 | 3.0 | 16.0 | ns |
| | | | | | 10, 11 | 3.0 | 20.0 | |
| Control setup time, high or low, $\overline{ADDR}$/DATA to LOAD- or L/HBYTE to LOAD- | $t_{s1}$ 7/ | | All | 4.5 V | 9 | 4.0 | | ns |
| | | | | | 10, 11 | 4.5 | | |
| Data setup time, high or low, Dn to LOAD+ | $t_{s2}$ 7/ | | All | 4.5 V | 9 | 4.0 | | ns |
| | | | | | 10, 11 | 4.5 | | |
| Control hold time, high or low, LOAD- to $\overline{ADDR}$/DATA or LOAD- to L/HBYTE | $t_{h1}$ 7/ | | All | 4.5 V | 9, 10, 11 | 1.0 | | ns |
| Data hold time, high or low, LOAD+ to Dn | $t_{h2}$ 7/ | | All | 4.5 V | 9, 10, 11 | 2.0 | | ns |
| Recovery time, LOAD+ to CLOCK | $t_{REC}$ 7/ 9/ | | All | 4.5 V | 9 | 7.0 | | ns |
| | | | | | 10, 11 | 8.0 | | |
| LOAD pulse width, low | $t_{w1}$ 7/ | | All | 4.5 V | 9, 10, 11 | 5.5 | | ns |
| LOAD pulse width, high | $t_{w2}$ 7/ | | All | 4.5 V | 9 | 5.0 | | ns |
| | | | | | 10, 11 | 7.5 | | ns |
| CLR pulse width, high | $t_{w3}$ 7/ | | All | 4.5 V | 9 | 6.5 | | ns |
| | | | | | 10, 11 | 9.5 | | ns |
| CLOCK pulse width, high or low | $t_{w4}$ 7/ | | All | 4.5 V | 9 | 3.0 | | ns |
| | | | | | 10, 11 | 4.0 | | ns |

See footnotes on next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ For tests not listed in the referenced MIL-STD-883 (e.g. $\Delta I_{CC}$), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the $I_{CC}$ and $\Delta I_{CC}$ tests, the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet the limits specified in table I as applicable, at $4.5\ V \le V_{CC} \le 5.5\ V$.

4/ Transmission driving tests are performed at $V_{CC}$ = 5.5 V dc with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IN}$ = 2.0 V or 0.8 V.

5/ This is the increase in supply current for each input that is at one of the specific TTL voltage levels rather than 0 V or $V_{CC}$. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1\ V$ (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limits are equal to the number of inputs at a high TTL input level times 1.6 mA or 1.0 mA, as applicable; and the preferred method and limits are guaranteed.

6/ Power dissipation capacitance ($C_{PD}$) determines the no load dynamic power consumption, $P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$, and the dynamic current consumption, $I_S = (C_{PD} + C_L)V_{CC}f + I_{CC} + n \times d \times \Delta I_{CC}$. For both $P_D$ and $I_S$, n is the number of device inputs at TTL levels, f is the frequency of the input signal, and d is the duty cycle of the input signal.

7/ This parameter shall be guaranteed, if not tested, to the limits in table I, herein.

8/ AC limits at $V_{CC}$ = 5.5 V are equal to the limits at $V_{CC}$ = 4.5 V and guaranteed by testing at $V_{CC}$ = 4.5 V. Minimum propagation delay time limits for $V_{CC}$ = 5.5 V shall be guaranteed to be no more than 0.5 ns less than those specified at $V_{CC}$ = 4.5 V in table I, herein. For propagation delay tests, all paths must be tested.

9/ Removal of vectored reset or restart to CLOCK.

| Device type | All | | |
|---|---|---|---|
| Case outlines | R and 2 | | |
| Terminal number | Terminal symbol | Terminal number | Terminal symbol |
| 1 | D0 | 11 | CLOCK |
| 2 | D1 | 12 | VCBLANK |
| 3 | D2 | 13 | HBLHDR |
| 4 | D3 | 14 | VCSYNC |
| 5 | D4 | 15 | HSYNVDR |
| 6 | D5 | 16 | ODD/$\overline{\text{EVEN}}$ |
| 7 | D6 | 17 | $\overline{\text{LOAD}}$ |
| 8 | D7 | 18 | $\overline{\text{L}}$/HBYTE |
| 9 | CLR | 19 | $\overline{\text{ADDR}}$/DATA |
| 10 | GND | 20 | $V_{CC}$ |

| Terminal symbol | Terminal symbol description |
|---|---|
| Data inputs Dn (n = 0 to 7) | The data input pins connect to the address register and the data input register. |
| $\overline{\text{ADDR}}$/DATA | The $\overline{\text{ADDR}}$/DATA is latched into the device on the falling edge of the LOAD signal. The signal determines if an address (0) or data (1) is present on the data bus. |
| $\overline{\text{L}}$/HBYTE | The $\overline{\text{L}}$/HBYTE signal is latched into the device on the falling edge of the LOAD signal. The signal determines if data will be read into the 8 LSB's (0) or the 4 MSB's (1) of the data registers. A 1 on this pin when an ADDR/DATA is a 0 enables auto-load mode. |
| LOAD | The LOAD control pin loads data into the address or data registers on the rising edge. ADDR/DATA and L/HBYTE data is loaded into the device on the falling edge of the LOAD. The LOAD pin has been implemented as a Schmitt trigger input for better noise immunity. |
| CLR | The CLR pin is an asynchronous input that initializes the device when it is high. Initialization consists of setting all registers to their mask programmed values, and initializing all counters, comparators, and registers. The CLR pin has been implemented as a Schmitt trigger for better noise immunity. A CLR pulse should be asserted by the user immediately after power-up to ensure proper initialization of the registers – even if the user plans to (re)program the device. A CLR pulse will disable the clock on device type 01 and will enable the clock on device type 02. |
| ODD/$\overline{\text{EVEN}}$ | Output that identifies if display is in odd (high) or even (low) field of interlace when device is in interlaced mode of operation. In noninterlaced mode of operation, this output is always high. Data can be serially scanned out on this pin during scan mode. |
| VCSYNC | Outputs vertical or composite sync signal based on the value of the status register. Equalization and serration pulses will, if enabled, be the output on the VCSYNC signal in composite mode only. |
| VCBLANK | Outputs vertical or composite blanking signal based on the value of the status register. |
| HBLHDR | Outputs horizontal blanking signal, horizontal gating signal, or cursor position based on the value of the status register. |
| HSYNVDR | Outputs horizontal sync signal, vertical gating signal, or vertical interrupt signal based on the value of the status register. |

FIGURE 1. Terminal connections.

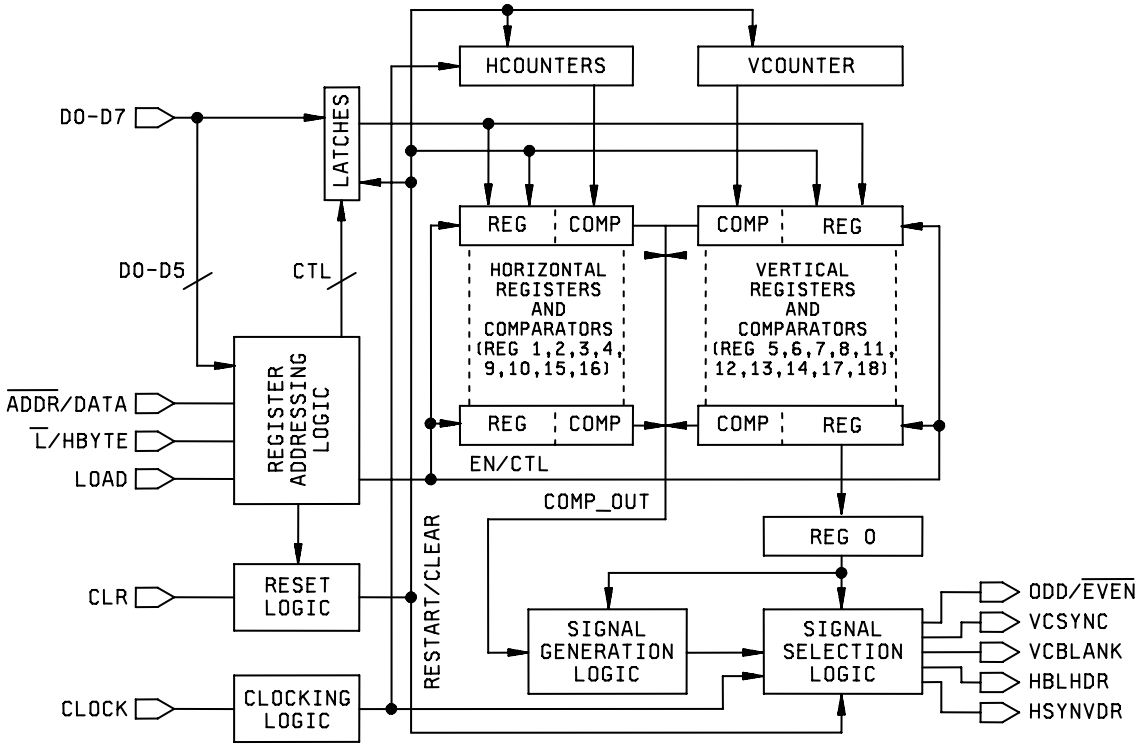



FIGURE 2. Block diagram.

| Registers | Descriptions |
|---|---|
| Status register | The status register, REG0, control the mode of operation, the signals that are output, and the polarity of these outputs. The default value for the status register is 0 (000 hex) for the device type 01 and is 512 (200 hex) for the device type 02. See detailed descriptions below. |
| Horizontal interval registers | The horizontal interval registers determine the number of clock cycles per line and the characteristics of the horizontal sync and blank pulses.<br>REG1: Horizontal front porch<br>REG2: Horizontal sync pulse end time<br>REG3: Horizontal blanking width<br>REG4: Horizontal interval width (number of clocks per line) |
| Vertical interval registers | The vertical interval registers determine the number of lines per frame and the characteristics of the vertical blank and sync pulses.<br>REG5: Vertical front porch<br>REG6: Vertical sync pulse end time<br>REG7: Vertical blanking width<br>REG8: Vertical interval width (number of lines per frame) |
| Equalization and serration pulse specification registers | These registers determine the width of equalization and serration pulses and the vertical interval over which they occur.<br>REG9: Equalization pulse width end time<br>REG10: Serration pulse width end time<br>REG11: Equalization/serration pulse vertical interval start time<br>REG12: Equalization/serration pulse vertical interval end time |
| Vertical interrupt specification interval registers | These registers determine the width of the vertical interrupt signal if used.<br>REG13: Vertical interrupt activate time<br>REG14: Vertical interrupt deactivate time |
| Cursor location registers | These registers determine the cursor position location or they generate separate horizontal and vertical gating signals.<br>REG15: Horizontal cursor position start time<br>REG16: Horizontal cursor position end time<br>REG17: Vertical cursor position start time<br>REG18: Vertical cursor position end time |

Status register descriptions:

Bits 0 through 2

| B2 | B1 | B0 | VCBLANK | VCSYNC | HBLHDR | HSYNVDR |
|---|---|---|---|---|---|---|
| 0 | 0 (default) | 0 | CBLANK | CSYNC | HGATE | VGATE |
| 0 | 0 | 1 | VBLANK | CSYNC | HBLANK | VGATE |
| 0 | 1 | 0 | CBLANK | VSYNC | HGATE | HSYNC |
| 0 | 1 | 1 | VBLANK | VSYNC | HBLANK | HSYNC |
| 1 | 0 | 0 | CBLANK | CSYNC | CURSOR | VINT |
| 1 | 0 | 1 | VBLANK | CSYNC | HBLANK | VINT |
| 1 | 1 | 0 | CBLANK | VSYNC | CURSOR | HSYNC |
| 1 | 1 | 1 | VBLANK | VSYNC | HBLANK | HSYNC |

FIGURE 3. Register descriptions.

Bits 3 and 4

| B3 | B4 | Mode of operation |
|---|---|---|
| 0 (Default) | 0 | Interlaced double serration and equalization |
| 0 | 1 | Noninterlaced double serration |
| 1 | 0 | Illegal state |
| 1 | 1 | Noninterlaced single serration and equalization |

Bits 5 through 8 and 9 through 11

| Bit numbers | Descriptions |
|---|---|
| Bits 5 through 8 | These bits control the polarity of the outputs. A value of 0 in these bit locations indicates an output pulse active low. A value of 1 indicates active high pulse.<br>B5: VCBLANK polarity<br>B6: VCSYNC polarity<br>B7: HBLHDR polarity<br>B8: HSYNVDR polarity |
| Bits 9 through 11 | Bits 9 through 11 enable several different features of the device.<br>B9: Enable equalization/serration pulses (0); disable equalization/serration pulses (1).<br>B10: Disable system clock (0); enable system clock (1). The default values are 0 for B10 in device type 01 and 1 in the device type 02.<br>B11: Disable counter test mode (0); enable counter test mode (1). This bit is not intended for the user but is for internal testing only. |

FIGURE 3. Register descriptions – Continued.

| Signal specifications | Descriptions |
|---|---|
| Horizontal sync and blank specifications | All horizontal signals are defined by start and end time. The start and end times are specified in number of clock cycles per line. The start of the horizontal line is considered pulse 1 not 0. All values of the horizontal timing registers are referenced to the falling edge of the horizontal blank signal. Since the first clock edge, clock #1, causes the first falling edge of the horizontal blank reference pulse, edges referenced to this first horizontal edge are n + 1 clocks away, where n is the width of the timing in question. Registers 1, 2, and 3 are programmed in this manner. The horizontal counters start at 1 and count until HMAX. The value of HMAX must be divisible by 2. This limitation is imposed because during interface operation, this value is internally divided by 2 in order to generate serration and equalization pulses at twice the horizontal frequency. Horizontal signals will change on the falling edge of the clock signal. Signal specifications are shown below.<br>Horizontal period (HPER) = REG(4) x ckper<br>Horizontal blanking width = (REG(3) – 1) x ckper<br>Horizontal sync width = (REG(2) – REG(1)) x ckper<br>Horizontal front porch = (REG(1) – 1) x ckper |

FIGURE 4. Signal specifications.

| Signal specifications | Descriptions |
|---|---|
| Vertical sync and blank specifications | All vertical signals are defined in terms of number of lines per frame. This is true in both interlaced and noninterlaced modes of operation. Care must be taken to not specify the vertical registers in terms of lines per field. Since the first clock edge, clock # 1, causes the first falling edge of the vertical blank (first horizontal blank) reference pulse, edges referenced to this first edge are n + 1 lines away, where n is the width of the timing in question. Registers 5, 6, and 7 are programmed in this manner. Also, in the interlaced mode, vertical timing is based on half-lines. Therefore, registers 5, 6, and 7 must contain a value twice the total of the horizontal (odd and even) plus 1. In noninterlaced mode, all vertical timing is based on whole-lines. Register 8 is always based on whole-lines and does not add 1 for the first clock. The vertical counter starts at the value of 1 and counts until the value of VMAX. No restrictions exist on the values placed in the vertical registers. Vertical blank will change on the leading edge of HBLANK. Vertical sync will change on the leading edge of HSYNC.<br>Vertical frame period (VPER) = REG(8) x hper<br>Vertical field period (VPER/n) = REG(8) x hper/n<br>Vertical blanking width = (REG(7) – 1) x hper/n<br>Vertical syncing width = (REG(6) – REG(5)) x hper/n<br>Vertical front porch = (REG(5) – 1) x hper/n<br>Where n = 1 for noninterlaced; n = 2 for interlaced |
| Composite sync and blank specifications | Composite sync and blank signals are created by logically ANDing (ORing) the active low (high) signals of the corresponding vertical and horizontal components of these signals. The composite sync signal may also include serration and/or equalization pulses. The serration pulses interval occurs in place of the vertical sync interval. Equalization pulses occur preceding and/or following the serration pulses. The width and location of these pulses can be programmed through the registers shown below.<br>Horizontal equalization PW = (REG(9) – REG(1)) x ckper<br>REG9 = HFP + HEQP + 1<br>Horizontal serration PW = (REG(4)/n + REG(1) – REG(10)) x ckper<br>REG10 = HFP + (HPER/2) – HSERR + 1<br>Where n = 1 for noninterlaced single serration/equalization; n = 2 for noninterlaced double serration/equalization; n = 2 for interlaced operation. |
| Horizontal and vertical gating signals | Horizontal drive and vertical drive outputs can be utilized as general purpose gating signals. Horizontal and vertical gating signals are available for use when composite sync and blank signals are selected and the value of bit 2 of status register is 0. The vertical gating signal will change in the same manner as that specified for the vertical blank.<br>Horizontal gating signal width = (REG(16) – REG(15)) x ckper<br>Vertical gating signal width = (REG(18) – REG(17)) x hper |
| Cursor position and vertical interrupt | The cursor position and vertical interrupt signal are available when composite sync and blank signals are selected and bit 2 of the status register is set to the value of 1. The cursor position generates a signal pulse of n clocks wide during every line that the cursor is specified. The signals are generated by logically ORing (ANDing) the active low (high) signals specified by the registers used for generating horizontal and vertical gating signals. The vertical interrupt signal generates a pulse during the vertical interval specified. The vertical interrupt signal will change in the same manner as that specified for the vertical blanking signal.<br>Horizontal cursor width = (REG(16) – REG(15)) x ckper<br>Vertical cursor width = (REG(18) – REG(17)) x hper<br>Vertical interrupt width = (REG(14) – REG(13)) x hper |

FIGURE 4. Signal specifications – Continued.

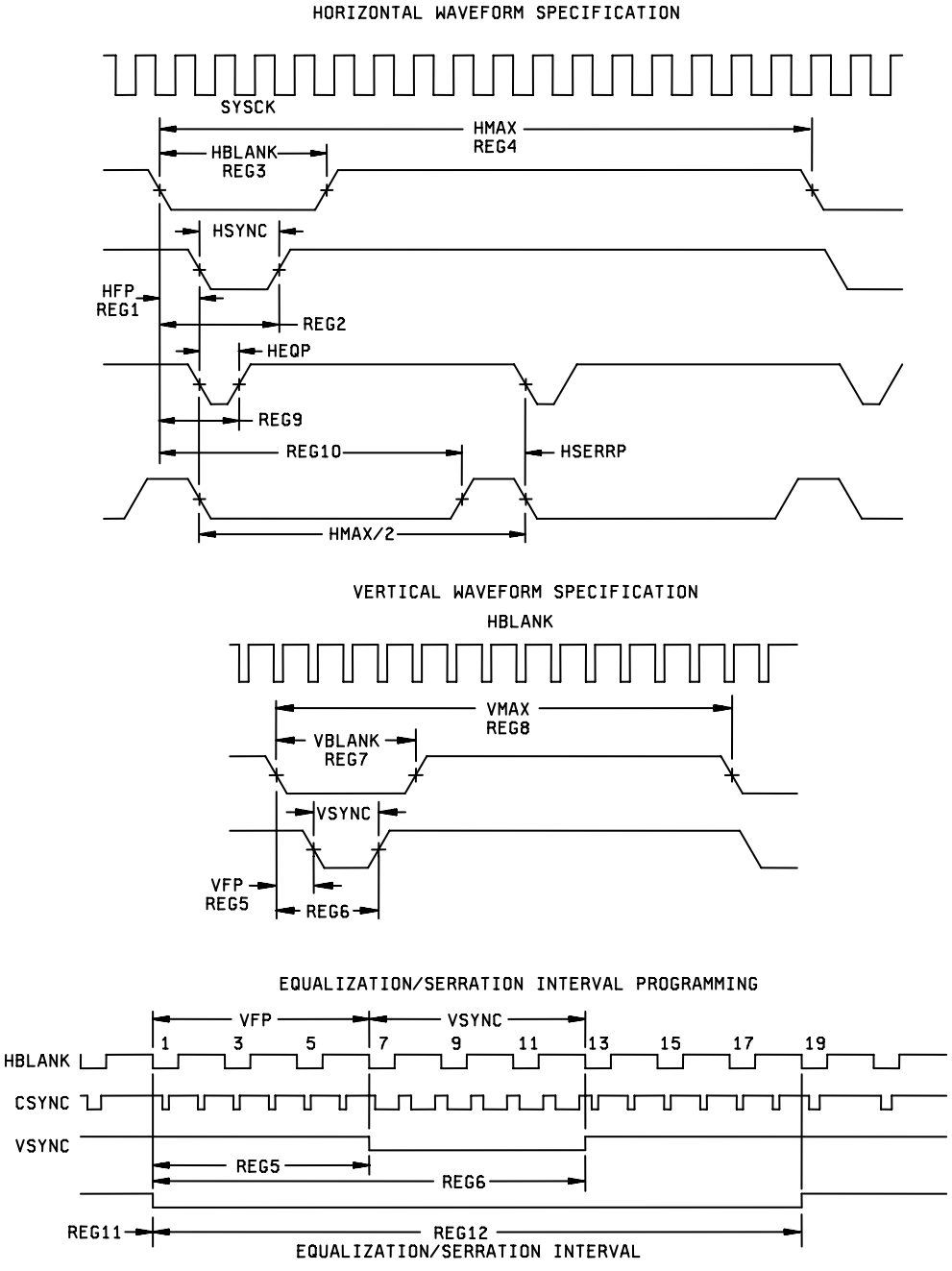


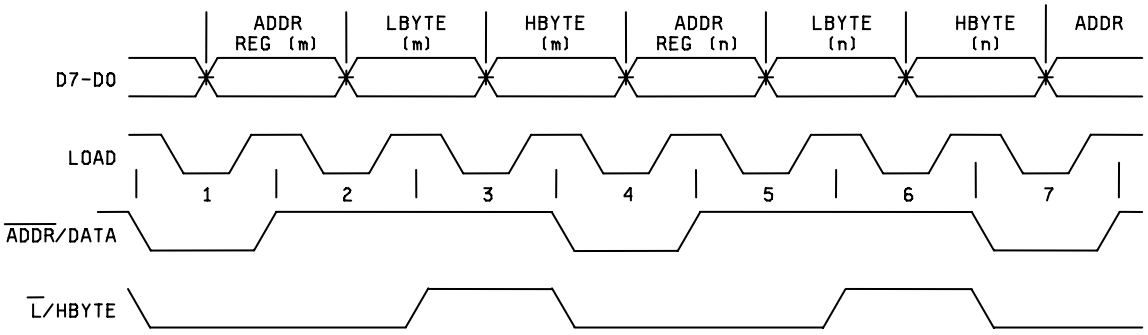

FIGURE 4. Signal specifications – Continued.

| Addressing logic | Descriptions |
|---|---|
| Address register and counter (ADDRCNTR) | Addresses for the data registers can be generated by one of two methods. Manual addressing requires that each byte of each register that needs to be loaded needs to be addressed. To load both bytes of all 19 registers would require a total of 57 load cycles (19 address and 38 data cycles). Auto addressing requires that only the initial register value be specified. The auto load sequence would require only 39 load cycles to completely program all registers (1 address and 38 data cycles). In the auto load sequence, the low order byte of the data register will be written first followed by the high order byte on the next load cycle. At the time the high byte is written, the address counter is incremented by 1. The counter has been implemented to loop on the initial value loaded into the address register. Auto addressing is initiated on the falling edge of LOAD when ADDR/DATA is 0 and L/HBYTE is 1.<br>Incrementing and loading of data registers will not commence until the falling edge of LOAD after ADDR/DATA goes to 1. The next rising edge of LOAD will load the first byte of data. Auto incrementing is disabled on the falling edge of LOAD after ADDR/DATA and L/HBYTE go low. (See the illustrations of manual and auto addressing modes below.) |
| Address decode (ADDRDEC) | The ADDRDEC logic decodes the current address and generates the enable signal for the appropriate register. The enable values for the registers and counters change on the falling egde of LOAD. Two types of ADDRDEC logic is enabled by two pair of addresses, address 22 or 54 (vectored restart logic) and address 23 or 55 (vectored clear logic). Loading these addresses will enable the appropriate logic and put the part into either a start (all counter registers are reinitialized with preprogrammed data) or clear (all registers are cleared to zero) state. Reloading the same ADDRDEC address will not cause any change in the state of the part. The outputs during these states are frozen and the internal clock is disabled. Clocking the part during a vectored restart or vectored clear state will have no effect on the part. To resume operation in the new state, or disable the vectored restart or vectored clear state, another non-ADDRDEC address must be loaded. Operation will begin in the new state on the rising edge of the non-ADDRDEC load pulse. It is recommended that an inused address be loaded following an ADDRDEC operation to prevent data registers from accidentally being corrupted. The following addresses are used by the device.<br>Address 0: Status register, REG0<br>Address 1-18: Data registers, REG1 – REG18<br>Address 19-21: Unused<br>Address 22/54: Restart vector (restarts device)<br>Address 23/55: Clear vector (zero all registers)<br>Address 24-31: Unused<br>Address 32-50: Register scan addresses<br>Address 51-53: Counter scan addresses<br>Address 56-63: Unused<br>At any given time only one register at most is selected. It is possible to have no registers selected. |

FIGURE 5. Addressing logic.

Manual addressing mode

| Cycle number | Load falling edge | Load rising edge |
|---|---|---|
| 1 | Enable manual addressing | Load address m |
| 2 | Enable Lbyte data load | Load Lbyte m |
| 3 | Enable Hbyte data load | Load Hbyte m |
| 4 | Enable manual addressing | Load address n |
| 5 | Enable Lbyte data load | Load Lbyte n |
| 6 | Enable Hbyte data load | Load Hbyte n |




Auto addressing mode

| Cycle number | Load falling edge | Load rising edge |
|---|---|---|
| 1 | Enable auto addressing | Load start address n |
| 2 | Enable Lbyte data load | Load Lbyte n |
| 3 | Enable Hbyte data load | Load Hbyte (n); inc. counter |
| 4 | Enable Lbyte data load | Load Lbyte (n + 1) |
| 5 | Enable Hbyte data load | Load Hbyte (n + 1); inc. counter |
| 6 | Enable manual addressing | Load address |

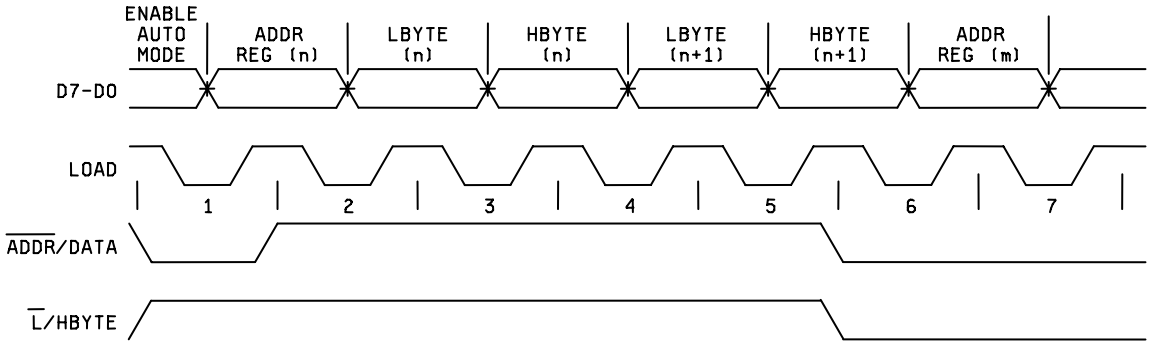



FIGURE 5. Addressing logic – Continued.

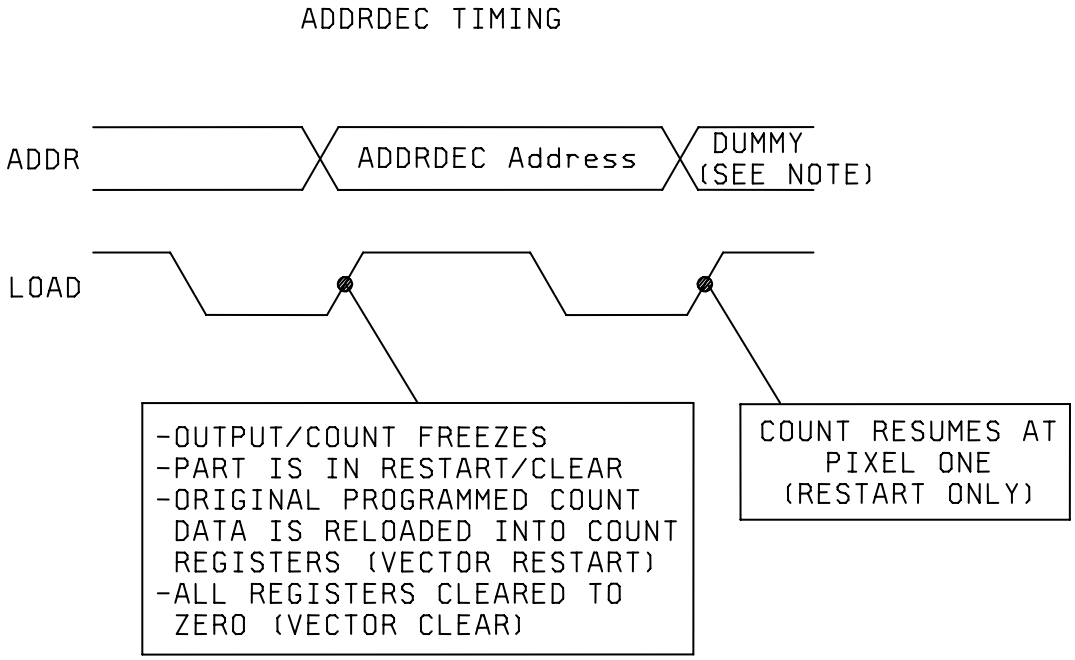
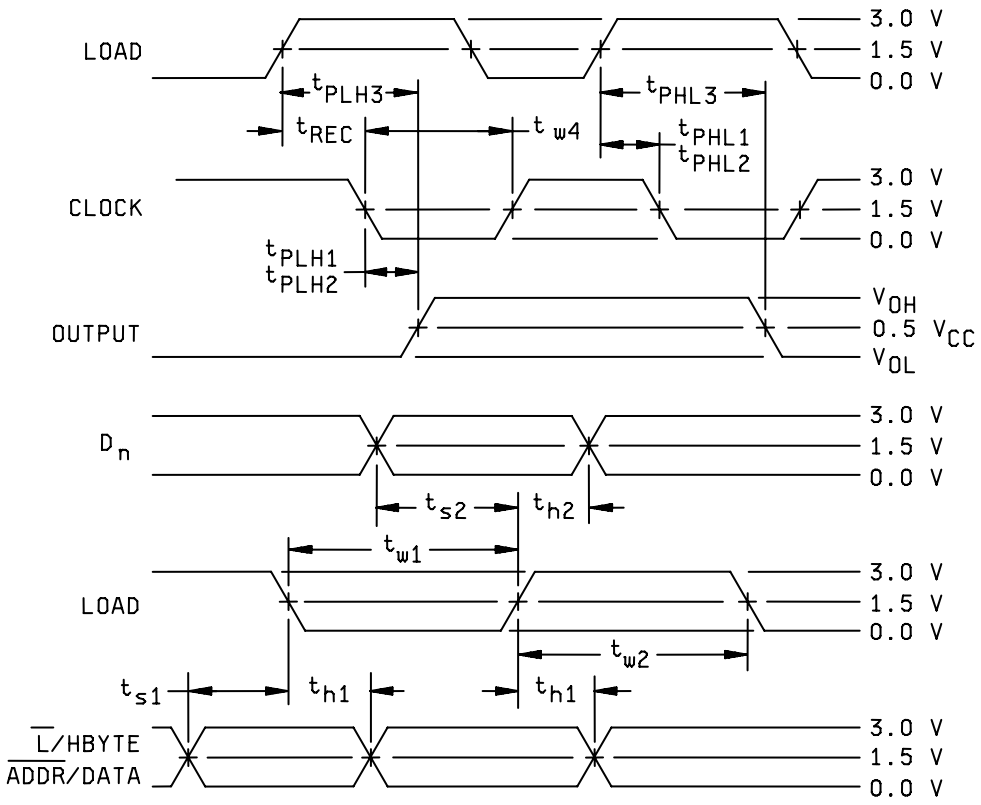
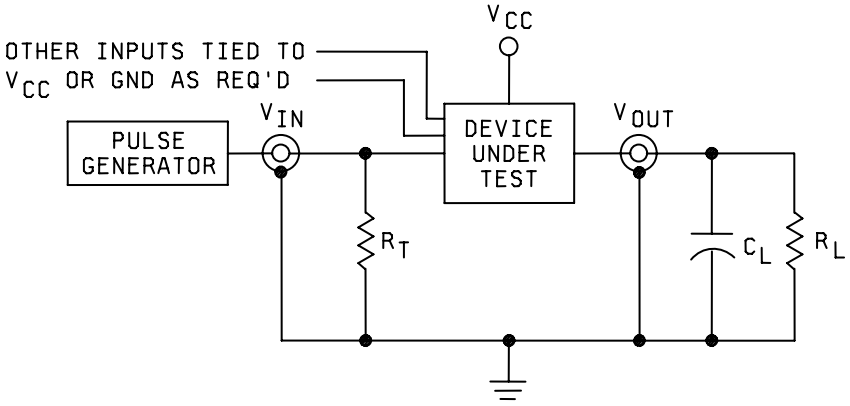



FIGURE 5. Addressing logic – Continued.




NOTES:

1. $C_L$ = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. $R_T$ = 50Ω or equivalent. $R_L$ = 500Ω or equivalent.
6. Input signal from pulse generator: $V_{IN}$ = 0.0 V to 3.0 V; PRR ≤ 10 MHz; $t_r$ ≤ 2.5 ns; $t_f$ ≤ 2.5 ns; $t_r$ and $t_f$ shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V respectively; duty cycle = 50 percent.
7. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
8. The outputs are measured one at a time with one transition per measurement.

FIGURE 6. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | - - - | 1 | 1 |
| Final electrical parameters (see 4.2) | 1/ 1, 2, 3, 7, 8, 9 | 1/ 1, 2, 3, 7, 8, 9, 10, 11 | 2/ 1, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (see 4.4) | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 1, 2, 3 |
| Group D end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 1, 2, 3 |
| Group E end-point electrical parameters (see 4.4) | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. $C_{IN}$ and $C_{PD}$ shall be measured only for initial qualification and after process or design changes which may affect capacitance. $C_{IN}$ and $C_{OUT}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. $C_{PD}$ shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For $C_{IN}$ and $C_{PD}$, test all applicable pins on five devices with zero failures.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows.

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-11-27

Approved sources of supply for SMD 5962-93097 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-9309701MRA | 27014<br>0C7V7 | 54ACT715DMQB |
| 5962-9309701M2A | 0C7V7 | 54ACT715LMQB |
| 5962-9309702MRA | 27014<br>0C7V7 | 54ACT715-RDMQB |
| 5962-9309702M2A | 27014<br>0C7V7 | 54ACT715-RLMQB |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 27014 | National Semiconductor<br>2900 Semiconductor Drive<br>P.O. Box 58090<br>Santa Clara, CA 95052-8090 |
| 0C7V7 | QP Semiconductor<br>2945 Oakmead Village Court<br>Santa Clara, CA 95051 |