

# DS90C032QML

*DS90C032QML LVDS Quad CMOS Differential Line Receiver*



Literature Number: SNLS203C

# DS90C032QML

## LVDS Quad CMOS Differential Line Receiver

### General Description

The DS90C032 is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates.

The DS90C032 accepts low voltage differential input signals and translates them to CMOS (TTL compatible) output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs. The receiver also supports OPEN Failsafe and terminated (100Ω) input Failsafe with the addition of external failsafe biasing. Receiver output will be HIGH for both Failsafe conditions.

The DS90C032 provides power-off high impedance LVDS inputs. This feature assures minimal loading effect on the LVDS bus lines when VCC is not present.

The DS90C032 and companion line driver (DS90C031) provide a new alternative to high power pseudo-ECL devices for high speed point-to-point interface applications.

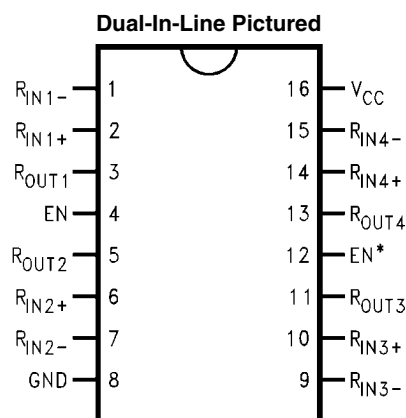
### Features

- Single Event Latchup (SEL) Immune 120 MeV-cm<sup>2</sup>/mg
- High impedance LVDS inputs with power-off.
- Accepts small swing (330 mV) differential signal levels
- Low power dissipation.
- Low differential skew.
- Low chip to chip skew.
- Pin compatible with DS26C32A
- Compatible with IEEE 1596.3 SCI LVDS standard

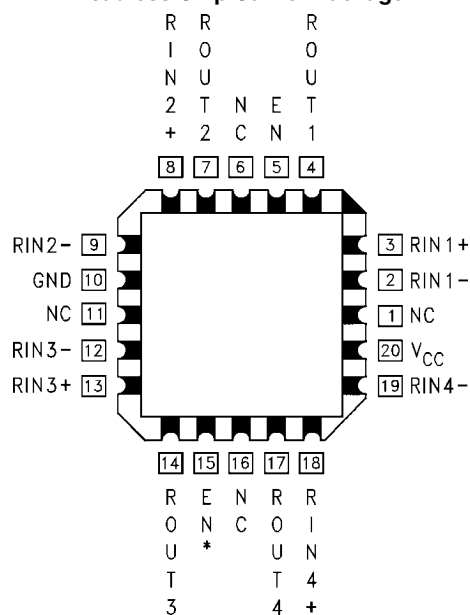
### Ordering Information

| NS Part Number  | SMD Part Number                | NS Package Number | Package Description        |
|-----------------|--------------------------------|-------------------|----------------------------|
| DS90C032E-QML   | 5962-9583401Q2A                | E20A              | 20LD Leadless Chip Carrier |
| DS90C032W-QMLV  | 5962-9583401VFA                | W16A              | 16LD Ceramic Flatpack      |
| DS90C032WLQMLV  | 5962L9583401VFA<br>50 krad(Si) | W16A              | 16LD Ceramic Flatpack      |
| DS90C032WGLQMLV | 5962L9583401VZA<br>50 krad(Si) | WG16A             | 16LD Ceramic SOIC          |

### Connection Diagrams



20163701  
See NS Package Number W16A & WG16A



See NS Package Number E20A

The diagram shows a 4-bit ripple-carry adder. It consists of four full-adder blocks (R1, R2, R3, R4) and an OR gate. The inputs are  $R_{IN1+}$ ,  $R_{IN1-}$ ,  $R_{IN2+}$ ,  $R_{IN2-}$ ,  $R_{IN3+}$ ,  $R_{IN3-}$ ,  $R_{IN4+}$ ,  $R_{IN4-}$ ,  $EN$ , and  $EN^*$ . The outputs are  $R_{OUT1}$ ,  $R_{OUT2}$ ,  $R_{OUT3}$ , and  $R_{OUT4}$ . The carry-out of each stage is the carry-in for the next stage. The final carry-out is the output of the OR gate.

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## Receiver

| ENABLES                                    |     | INPUTS              | OUTPUT |
|--------------------------------------------|-----|---------------------|--------|
| EN                                         | EN* | $R_{I+} - R_{I-}$   | $R_O$  |
| L                                          | H   | X                   | Z      |
| All other combinations<br>of ENABLE inputs |     | $V_{ID} \geq 0.1V$  | H      |
|                                            |     | $V_{ID} \leq -0.1V$ | L      |

## Absolute Maximum Ratings *(Note 1)*

|                                                           |                                            |
|-----------------------------------------------------------|--------------------------------------------|
| Supply Voltage ( $V_{CC}$ )                               | -0.3V to +6V                               |
| Input Voltage ( $R_{I+}$ , $R_{I-}$ )                     | -0.3V to +5.8V                             |
| Enable Input Voltage<br>( $EN$ , $EN^*$ )                 | -0.3V to ( $V_{CC} + 0.3V$ )               |
| Output Voltage ( $R_O$ )                                  | -0.3V to ( $V_{CC} + 0.3V$ )               |
| Storage Temperature Range ( $T_{Sig}$ )                   | $-65^{\circ}C \leq T_A \leq +150^{\circ}C$ |
| Lead Temperature Range<br>Soldering (4 sec.)              | +260°C                                     |
| Maximum Package Power Dissipation @ +25°C <i>(Note 2)</i> |                                            |
| LCC Package                                               | 1,830 mW                                   |
| Ceramic Flatpack                                          | 1,400 mW                                   |
| Ceramic SOIC                                              | 1,400 mW                                   |
| Thermal Resistance                                        |                                            |
| $\theta_{JA}$                                             |                                            |
| LCC Package                                               | 82°C/W                                     |
| Ceramic Flatpack                                          | 145°C/W                                    |
| Ceramic SOIC                                              | 145°C/W                                    |
| $\theta_{JC}$                                             |                                            |
| LCC Package                                               | 20°C/W                                     |
| Ceramic Flatpack                                          | 20°C/W                                     |
| Ceramic SOIC                                              | 20°C/W                                     |
| ESD Rating <i>(Note 3)</i>                                | 2KV                                        |

## Recommended Operating Conditions

|                                          | Min   | Typ   | Max    |
|------------------------------------------|-------|-------|--------|
| Supply Voltage ( $V_{CC}$ )              | +4.5V | +5.0V | +5.5V  |
| Receiver Input Voltage                   | Gnd   |       | 2.4V   |
| Operating Free Air Temperature ( $T_A$ ) | -55°C | +25°C | +125°C |

## Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

| Subgroup | Description         | Temp °C |
|----------|---------------------|---------|
| 1        | Static tests at     | +25     |
| 2        | Static tests at     | +125    |
| 3        | Static tests at     | -55     |
| 4        | Dynamic tests at    | +25     |
| 5        | Dynamic tests at    | +125    |
| 6        | Dynamic tests at    | -55     |
| 7        | Functional tests at | +25     |
| 8A       | Functional tests at | +125    |
| 8B       | Functional tests at | -55     |
| 9        | Switching tests at  | +25     |
| 10       | Switching tests at  | +125    |
| 11       | Switching tests at  | -55     |
| 12       | Settling time at    | +25     |
| 13       | Settling time at    | +125    |
| 14       | Settling time at    | -55     |

## DS90C032 Electrical Characteristics

### DC Parameters (Note 7)

| Symbol    | Parameter                                    | Conditions                                                   | Notes    | Min | Max      | Units   | Sub-groups |
|-----------|----------------------------------------------|--------------------------------------------------------------|----------|-----|----------|---------|------------|
| $V_{ThL}$ | Differential Input Low Threshold             | $V_{CM} = +1.2V$                                             | (Note 4) |     | -100     | mV      | 1, 2, 3    |
| $V_{ThH}$ | Differential Input High Threshold            | $V_{CM} = +1.2V$                                             | (Note 4) |     | 100      | mV      | 1, 2, 3    |
| $I_{In}$  | Input Current<br>( Input Pins)               | $V_{CC}=5.5V, V_I = 2.4V$                                    |          |     | $\pm 10$ | $\mu A$ | 1, 2, 3    |
|           |                                              | $V_{CC} = 5.5V, V_I = 0$                                     |          |     | $\pm 10$ | $\mu A$ | 1, 2, 3    |
|           |                                              | $V_{CC} = 0.0V, V_I = 2.4V$                                  |          |     | $\pm 10$ | $\mu A$ | 1, 2, 3    |
|           |                                              | $V_{CC} = 0.0V, V_I = 0.0V$                                  |          |     | $\pm 10$ | $\mu A$ | 1, 2, 3    |
| $V_{OH}$  | Output High Voltage                          | $V_{CC}= 4.5V, I_{OH} = -0.4\text{ mA},$<br>$V_{ID} = 200mV$ |          | 3.8 |          | V       | 1, 2, 3    |
| $V_{OL}$  | Output Low Voltage                           | $V_{CC} = 4.5, I_{OL} = 2\text{ mA},$<br>$V_{ID} = -200mV$   |          |     | 0.3      | V       | 1, 2, 3    |
| $I_{OS}$  | Output Short Circuit Current                 | Enabled, $V_O = 0V$                                          |          | -15 | -100     | mA      | 1, 2, 3    |
| $I_{OZ}$  | Output TRI-STATE Current                     | Disabled, $V_O = 0V$ or $V_{CC}$                             |          |     | $\pm 10$ | $\mu A$ | 1, 2, 3    |
| $V_{IH}$  | Input High Voltage                           |                                                              | (Note 4) | 2.0 |          | V       | 1, 2, 3    |
| $V_{IL}$  | Input Low Voltage                            |                                                              | (Note 4) |     | 0.8      | V       | 1, 2, 3    |
| $I_I$     | Input Current<br>(Enable Pins)               | $V_{CC} = 5.5V$                                              |          |     | $\pm 10$ | $\mu A$ | 1, 2, 3    |
| $V_{CL}$  | Input Clamp Voltage                          | $I_{CI} = -18mA$                                             |          |     | -1.5     | V       | 1, 2, 3    |
| $I_{CC}$  | No Load Supply Current                       | EN, EN* = $V_{CC}$ or Gnd,<br>Inputs Open                    |          |     | 11       | mA      | 1, 2, 3    |
|           |                                              | EN, EN* = 2.4 or 0.5,<br>Inputs Open                         |          |     | 11       | mA      | 1, 2, 3    |
| $I_{CCZ}$ | No Load Supply Current<br>Receivers Disabled | EN = Gnd, EN* = $V_{CC}$ ,<br>Inputs Open                    |          |     | 11       | mA      | 1, 2, 3    |

### AC Parameters (Note 7)

The following conditions apply, unless otherwise specified.

AC:  $V_{CC} = 4.5V / 5.0V / 5.5V, C_L = 20pF$

| Symbol     | Parameter                                     | Conditions                                                                                                    | Notes    | Min | Max | Units | Sub-groups |
|------------|-----------------------------------------------|---------------------------------------------------------------------------------------------------------------|----------|-----|-----|-------|------------|
| $t_{PHLD}$ | Differential Propagation Delay<br>High to Low | $V_{ID} = 200mV,$<br>Input pulse = 1.1V to 1.3V,<br>$V_I = 1.2V$ (0V differential) to $V_O =$<br>$1/2 V_{CC}$ |          | 1.0 | 8.0 | ns    | 9, 10, 11  |
| $t_{PLHD}$ | Differential Propagation Delay<br>Low to High | $V_{ID} = 200mV,$<br>Input pulse = 1.1V to 1.3V,<br>$V_I = 1.2V$ (0V differential) to $V_O =$<br>$1/2 V_{CC}$ |          | 1.0 | 8.0 | ns    | 9, 10, 11  |
| $t_{SkD}$  | Differential Skew $ t_{PHLD} - t_{PLHD} $     | $C_L = 20pF, V_{ID} = 200mV$                                                                                  |          |     | 3.0 | ns    | 9, 10, 11  |
| $t_{Sk1}$  | Channel to Channel Skew                       | $C_L = 20pF, V_{ID} = 200mV$                                                                                  | (Note 5) |     | 3.0 | ns    | 9, 10, 11  |
| $t_{Sk2}$  | Chip to Chip Skew                             | $C_L = 20pF, V_{ID} = 200mV$                                                                                  | (Note 6) |     | 7.0 | ns    | 9, 10, 11  |
| $t_{PLZ}$  | Disable Time Low to Z                         | Input pulse = 0V to 3.0V,<br>$V_O = V_{OL} + 0.5V,$<br>$R_L = 1K\Omega$ to $V_{CC}, V_I = 1.5V$               |          |     | 20  | ns    | 9, 10, 11  |
| $t_{PHZ}$  | Disable Time High to Z                        | Input pulse = 0V to 3.0V,<br>$V_I = 1.5V, V_O = V_{OH} - 0.5V,$<br>$R_L = 1K\Omega$ to Gnd                    |          |     | 20  | ns    | 9, 10, 11  |

| Symbol    | Parameter             | Conditions                                                                                 | Notes | Min | Max | Units | Sub-groups |
|-----------|-----------------------|--------------------------------------------------------------------------------------------|-------|-----|-----|-------|------------|
| $t_{PZH}$ | Enable Time Z to High | Input pulse = 0V to 3.0V,<br>$V_I = 1.5V$ , $V_O = 50\%$ ,<br>$R_L = 1K\Omega$ to Gnd      |       |     | 20  | ns    | 9, 10, 11  |
| $t_{PZL}$ | Enable Time Z to Low  | Input pulse = 0V to 3.0V,<br>$V_I = 1.5V$ , $V_O = 50\%$ ,<br>$R_L = 1K\Omega$ to $V_{CC}$ |       |     | 20  | ns    | 9, 10, 11  |

## AC/DC Post Radiation Limits *(Note 7)*

| Symbol    | Parameter                                    | Conditions                                | Notes | Min | Max | Units | Sub-groups |
|-----------|----------------------------------------------|-------------------------------------------|-------|-----|-----|-------|------------|
| $I_{CC}$  | No Load Supply Current                       | EN, EN* = $V_{CC}$ or Gnd,<br>Inputs Open |       |     | 20  | mA    | 1          |
|           |                                              | EN, EN* = 2.4 or 0.5,<br>Inputs Open      |       |     | 20  | mA    | 1          |
| $I_{CCZ}$ | No Load Supply Current<br>Receivers Disabled | EN = Gnd, EN* = $V_{CC}$ ,<br>Inputs Open |       |     | 20  | mA    | 1          |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Note 2:** Derate LCC @ 12.2mW/°C above +25°C. Derate ceramic flatpack @ 6.8mW/°C above +25°C

**Note 3:** Human body model, 1.5 k $\Omega$  in series with 100 pF.

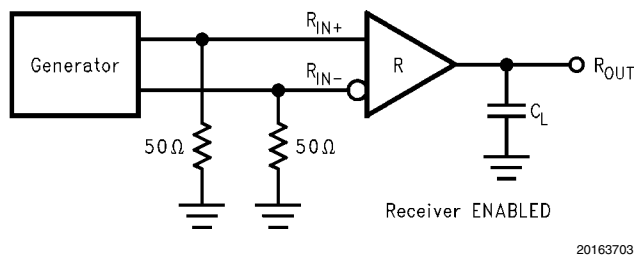
**Note 4:** Tested during  $V_{OH}$  /  $V_{OL}$  tests.

**Note 5:** Channel-to-Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with an event on the inputs.

**Note 6:** Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

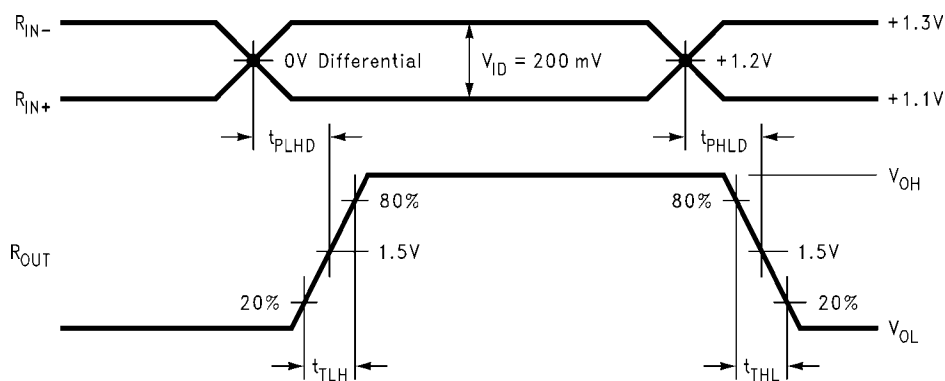
**Note 7:** Pre and post irradiation limits are identical to those listed under AC & DC electrical characteristics except as listed in the "Post Radiation Limits" table. Radiation end point limits for the noted parameters are guaranteed only for the conditions, as specified.

## Parameter Measurement Information



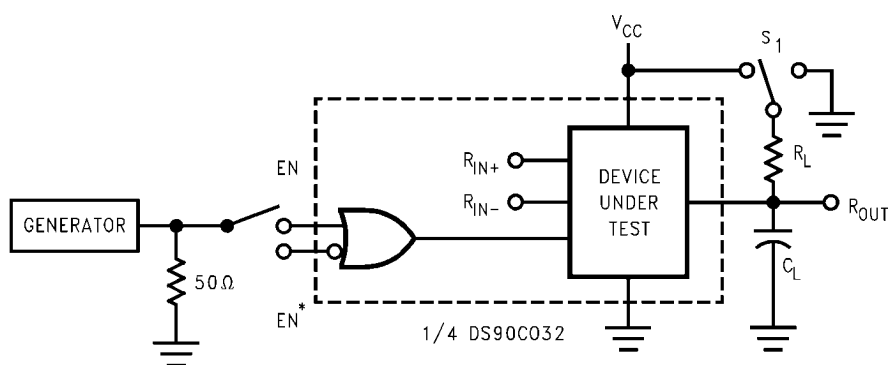
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**FIGURE 1. Receiver Propagation Delay and Transition Time Test Circuit**



20163704

**FIGURE 2. Receiver Propagation Delay and Transition Time Waveforms**



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$C_L$  includes load and test jig capacitance.

$S_1 = V_{CC}$  for  $t_{PZL}$  and  $t_{PLZ}$  measurements.

$S_1 = \text{Gnd}$  for  $t_{PZH}$  and  $t_{PHZ}$  measurements.

**FIGURE 3. Receiver TRI-STATE Delay Test Circuit**



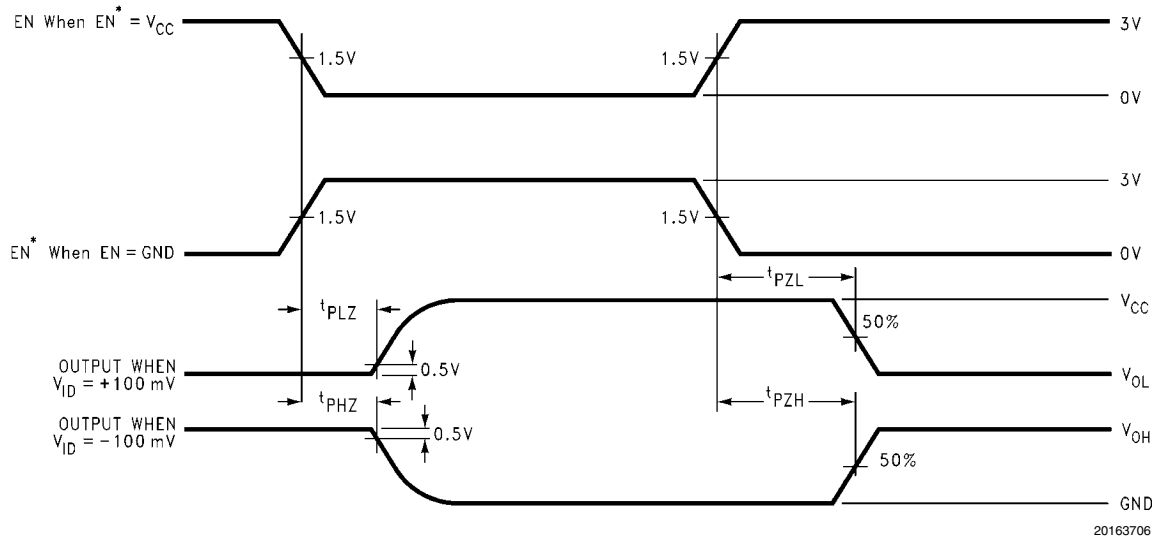
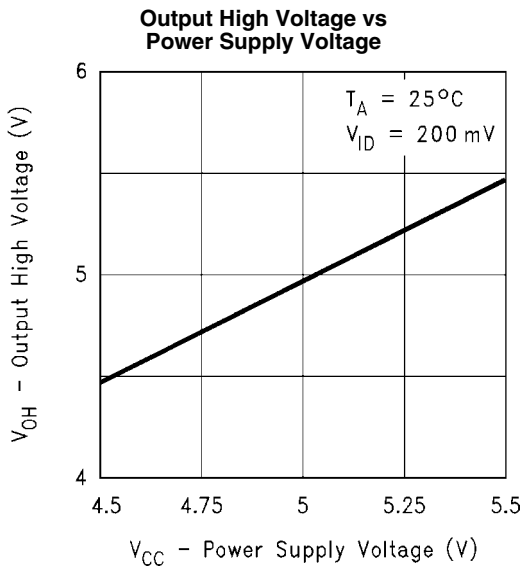
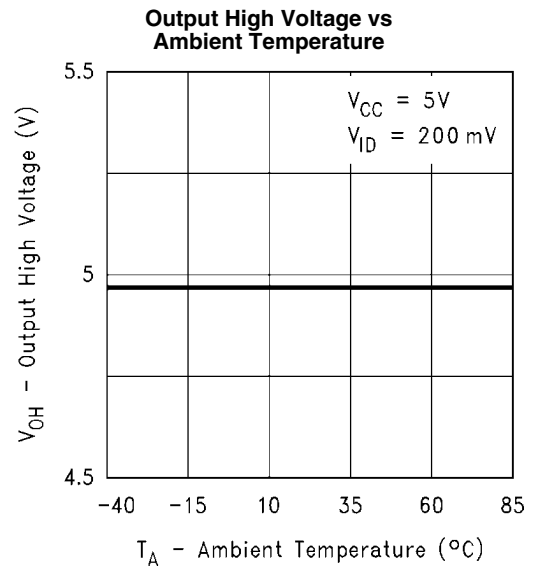


FIGURE 4. Receiver TRI-STATE Delay Waveforms

## Typical Performance Characteristics

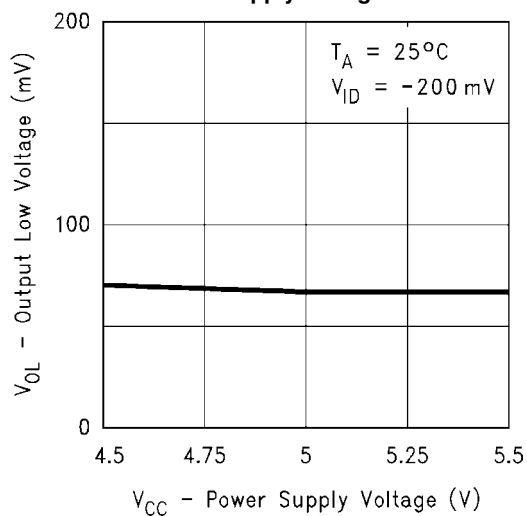


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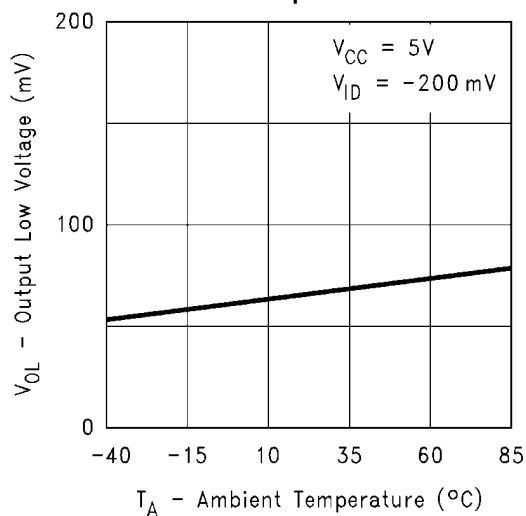
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**Output Low Voltage vs  
Power Supply Voltage**



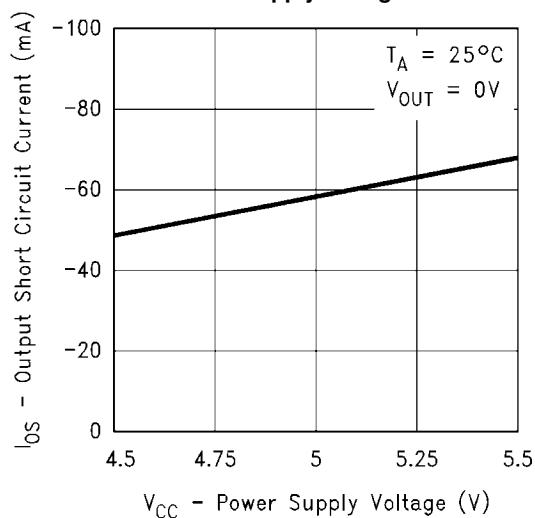
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**Output Low Voltage vs  
Ambient Temperature**



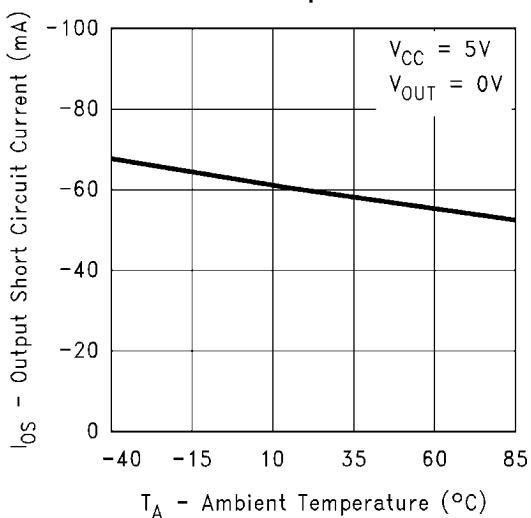
20163711

**Output Short Circuit Current  
vs Power Supply Voltage**



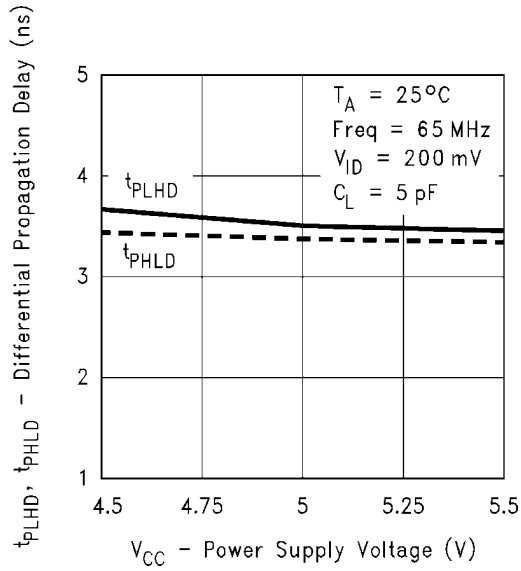
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**Output Short Circuit Current  
vs Ambient Temperature**



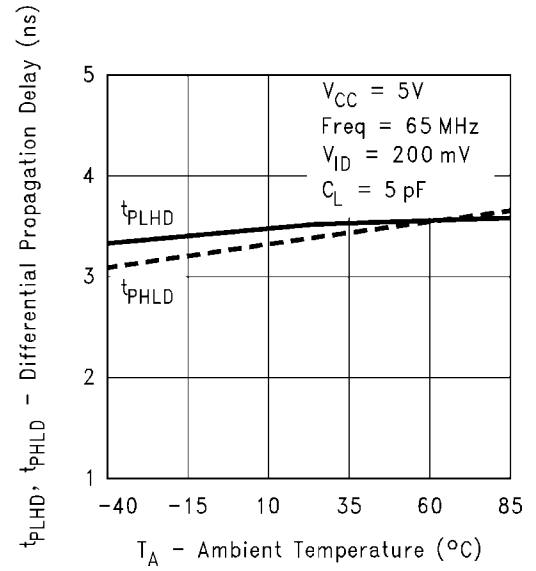
20163713

**Differential Propagation Delay  
vs Power Supply Voltage**



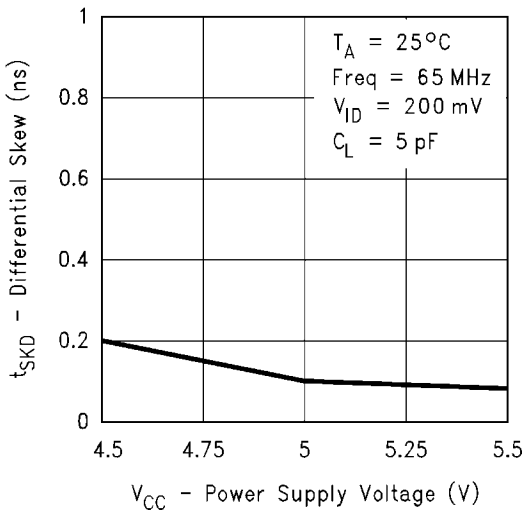
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**Differential Propagation Delay  
vs Ambient Temperature**



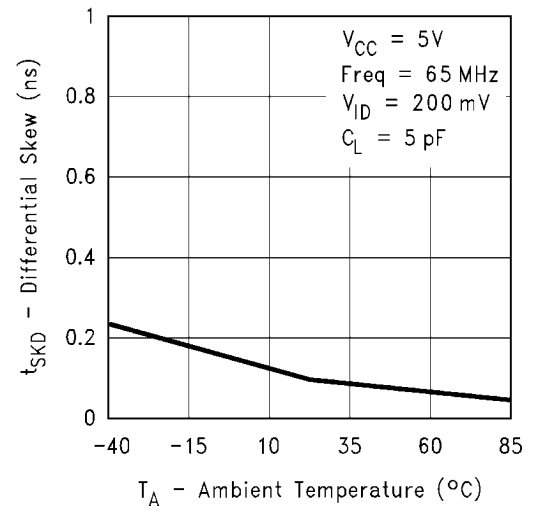
20163715

**Differential Skew vs  
Power Supply Voltage**

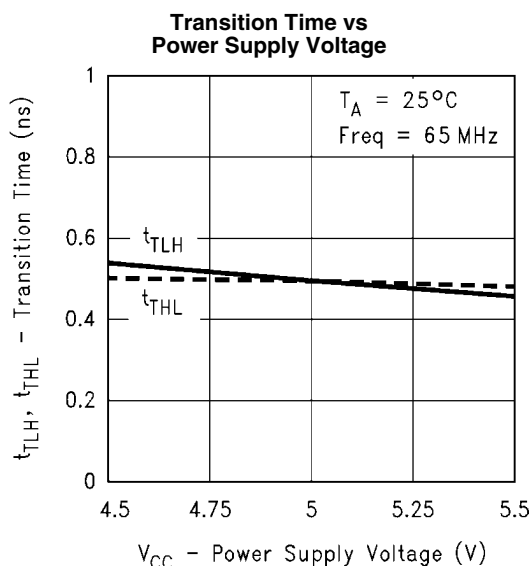


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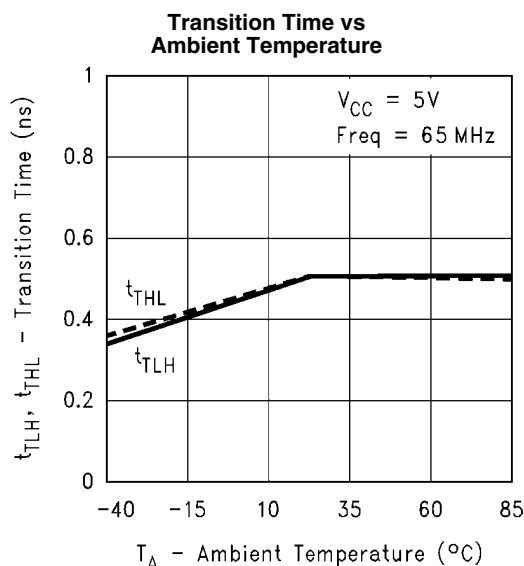
**Differential Skew vs  
Ambient Temperature**



20163717

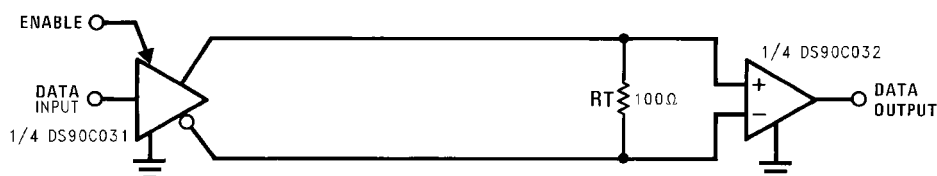


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## Typical Application



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FIGURE 5. Point-to-Point Application

## Applications Information

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 5. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90C032 differential line receiver is capable of detecting signals as low as 100 mV, over a  $\pm 1\text{V}$  common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift  $\pm 1\text{V}$  around this center point. The  $\pm 1\text{V}$  shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. Both receiver input pins should honor their specified operating input voltage range of 0V to +2.4V (measured from each pin to

ground), exceeding these limits may turn on the ESD protection circuitry which will clamp the bus voltages.

## Receiver Failsafe

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal failsafe circuitry is designed to source/sink a small amount of current, providing failsafe protection (a stable known state of HIGH output voltage) for floating and terminated (100Ω) receiver inputs in low noise environment (differential noise < 10mV).

### 1. Open Input Pins

The DS90C032 is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

### 2. Terminated Input

The DS90C032 requires external failsafe biasing for terminated input failsafe.

Terminated input failsafe is the case of a receiver that has a 100Ω termination across its inputs and the driver is in the following situations. Unplugged from the bus, or the driver output

is in TRI-STATE or in power-off condition. The use of external biasing resistors provide a small bias to set the differential input voltage while the line is un-driven, and therefore the receiver output will be in HIGH state. If the driver is removed from the bus but the cable is still present and floating, the unplugged cable can become a floating antenna that can pick up noise. The LVDS receiver is designed to detect very small amplitude and width signals and recover them to standard logic levels. Thus, if the cable picks up more than 10mV of differential noise, the receiver may respond. To insure that any noise is seen as commonmode and not differential, a balanced interconnect and twisted pair cables is recommended, as they help to ensure that noise is coupled common to both lines and rejected by the receivers.

### 3. Operation in environment with greater than 10mV differential noise

National recommends external failsafe biasing on its LVDS receivers for a number of system level and signal quality rea-

sons. First, only an application that requires failsafe biasing needs to employ it. Second, the amount of failsafe biasing is now an application design parameter and can be custom tailored for the specific application. In applications in low noise environments, they may choose to use a very small bias if any. For applications with less balanced interconnects and/or in high noise environments they may choose to boost failsafe further. Nationals "LVDS Owner's Manual provides detailed calculations for selecting the proper failsafe biasing resistors. Third, the common-mode voltage is biased by the resistors during the un-driven state. This is selected to be close to the nominal driver offset voltage (VOS). Thus when switching between driven and un-driven states, the common-mode modulation on the bus is held to a minimum.

For additional Failsafe Biasing information, please refer to Application Note AN-1194 for more detail.

## Pin Descriptions

| Pin No. (SOIC) | Name            | Description                            |
|----------------|-----------------|----------------------------------------|
| 2, 6, 10, 14   | R <sub>I+</sub> | Non-inverting receiver input pin       |
| 1, 7, 9, 15    | R <sub>I-</sub> | Inverting receiver input pin           |
| 3, 5, 11, 13   | R <sub>O</sub>  | Receiver output pin                    |
| 4              | EN              | Active high enable pin, OR-ed with EN* |
| 12             | EN*             | Active low enable pin, OR-ed with EN   |
| 16             | V <sub>CC</sub> | Power supply pin, +5V ± 10%            |
| 8              | Gnd             | Ground pin                             |

## Radiation Environments

Careful consideration should be given to environmental conditions when using a product in a radiation environment.

## Total Ionizing Dose

Radiation hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the Ordering Information table on the front page. Testing and qualification of these products is done on a wafer level according to MIL-STD-883G, Test Method 1019.7, Condition A and the "Extended room temperature anneal test" described in section 3.11 for application environment dose rates less than 0.19 rad(Si)/s. Wafer level TID data is available with lot shipments.

## Single Event Latch-Up and Functional Interrupt

One time single event latch-up (SEL) and single event functional interrupt (SEFI) testing was preformed according to EIA/JEDEC Standard, EIA/JEDEC57. The linear energy transfer threshold (LET<sub>th</sub>) shown in the Features on the front page is the maximum LET tested. A test report is available upon request.

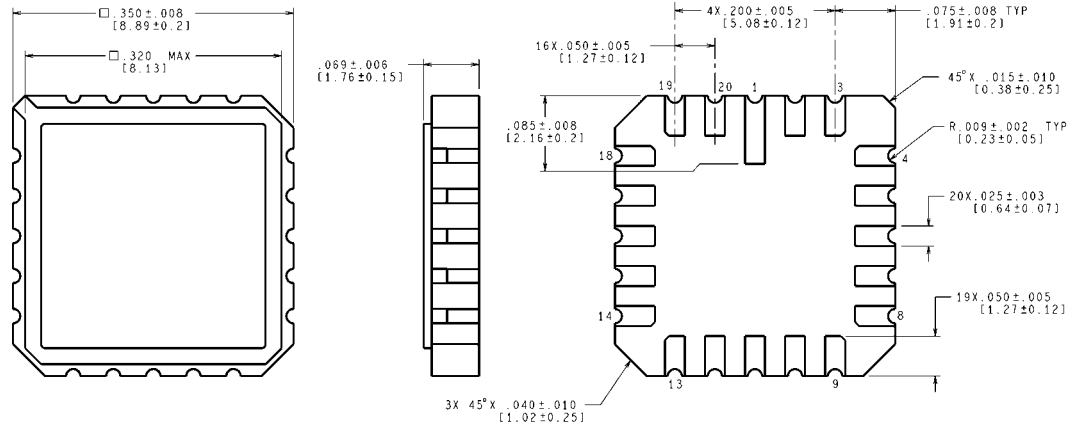
## Single Event Upset

A report on single event upset (SEU) is available upon request.

## Revision History

| Released  | Revision | Section                                                                        | Changes                                                                                                                                                                                                      |
|-----------|----------|--------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 03/01/06  | A        | New Release, Corporate format                                                  | 1 MDS data sheet converted into Corp. data sheet format. MNDS90C032-X-RH Rev 1B1 will be archived.                                                                                                           |
| 10/10/06  | B        | Applications Information - Pg. 10, Physical Dimensions - Pg. 12                | Deleted Shorted Inputs paragraph - page 10. Updated Physical Dimensions package drawings E20A, W16A to current revision - page 12. Revision A will be Archived.                                              |
| 05/07/07  | C        | Receiver Table - Pg. 2, Application Information - Pg. 9 & 10                   | Deleted Full Fail-safe OPEN/SHORT or terminated - Page 2. & Paragraph RECEIVER FAIL-SAFE and 1, 2, 3 - Page 9 & 10. Revision B will be Archived.                                                             |
| 9/28/2010 | D        | Order Information Table, General Description, Applications Information section | Copied general description and Receiver Failsafe from commercial d/s DS90C032B, dated Sept. 2003. Removed Code K devices. Added Radiation Environments paragraph to data sheet. Revision C will be Archived. |
|           |          |                                                                                |                                                                                                                                                                                                              |

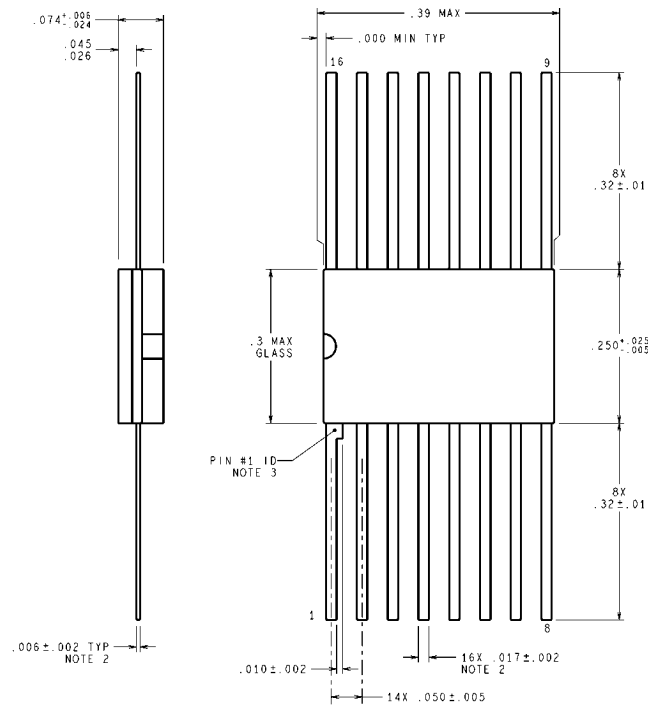
# Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS

E20A (Rev F)

## 20-Lead Ceramic Leadless Chip Carrier NS Package Number E20A



DIMENSIONS ARE IN INCHES

## 16-Lead Ceramic Flatpack NS Package Number W16A

W16A (Rev T)





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