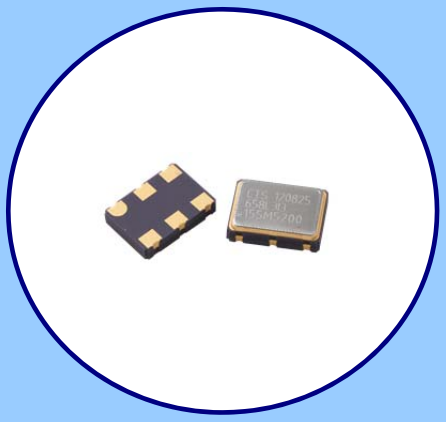
Model 656P/L

Advanced PLL Clock

FEATURES

- **Advanced PLL Design**
- **Differential LVPECL or LVDS Output**
- **Standard 7.0mm x 5.0mm 6-Pad Surface Mount Package**
- **Integrated Phase Jitter 600fs Typical [12kHz – 20MHz]**
- **Frequency Range 10MHz – 1.0GHz**
- **Frequency Stability; ±50ppm Standard, ±25ppm Available**
- **Operating Temperature to -40°C to +85°C**
- **Output Enable Standard**
- **Tape & Reel Packaging Available**
- **RoHS/Green Compliant [6/6]**



APPLICATIONS

Model 656P/L is ideal for applications such as networking equipment, broadcast video systems, Ethernet, Fiber Channel, storage area networks, PCI Express, test and measurement equipment.

ORDERING INFORMATION

656 □ □ □ □ □ □ □ □ □

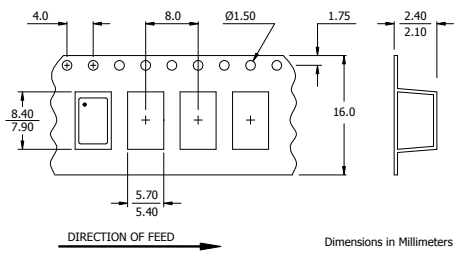
OUTPUT TYPE	FREQUENCY	FREQUENCY STABILITY	PACKAGING	SUPPLY VOLTAGE	TEMPERATURE RANGE
P = LVPECL - Pin 1 Enable L = LVDS - Pin 1 Enable	Product Frequency Code [1]	6 = ±20ppm [2] 5 = ±25ppm 3 = ±50ppm	T = 1k pcs./reel	2 = +2.5Vdc 3 = +3.3Vdc	C = -20°C to +70°C I = -40°C to +85°C [2]

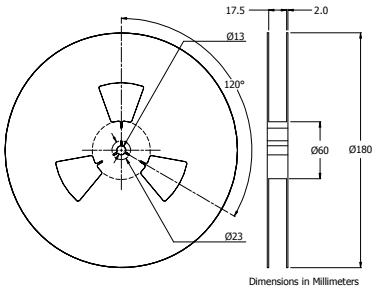
1. Refer to document 016-1454-0, Frequency Code Tables.
   3-digits required for frequencies below 100MHz and 4-digits for frequencies 100MHz or greater.
2. Consult factory for availability of 6I Stability/Temperature combination.

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

PACKAGING INFORMATION [Reference]

Device quantity is 1,000 pieces maximum per 180mm reel.





ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Electrical and Waveform Parameters	Maximum Supply Voltage	V_{CC}	-	-0.5	-	5.0	V
	Storage Temperature	T_{STG}	-	-55	-	+125	°C
	Frequency Range	f_O	-	10	-	1000	MHz
	Frequency Stability	$\Delta f/f_O$	All Inclusive, see Note 1.	-	-	20, 25, 50	± ppm
			1st year aging	-	-	3	
	Operating Temperature	T_A	-		+25		°C
	Commerical			-20		+70	
	Industrial			-40		+85	
	Supply Voltage	V_{CC}	±5%	2.38	2.5	2.63	V
				3.14	3.3	3.47	
	Supply Current	I_{CC}	Maximum Load				mA
	LVPECL			-	54	-	
	LVDS			-	23	-	
	Start Up Time	T_S	Application of V_{CC}	-	3	5	ms
	Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	-	0.7	<1	ps
	Period Jitter, RMS	pjrms	-	-	2.5	-	
	Period Jitter, Pk-Pk	pjpk-pk	-	-	25	-	
	Enable Function		Standby				V
	Enable Input Voltage	V_{IH}	Pin 1 Logic '1', Output Enabled	0.7*V_{CC}	-	-	
	Disable Input Voltage	V_{IL}	Pin 1 Logic '0', Output Disabled	-	-	0.3*V_{CC}	
	Disable Current	I_{IL}	Pin 1 Logic '1' , Output Disabled	-	-	20	uA
	Enable Time	T_{PLZ}	Pin 1 Logic '1'	-	-	5	ns
	LVPECL WAVEFORM						
	Output Load	R_L	Connected between each output and V_{CC} - 2V	-	50	-	Ohms
	Output Duty Cycle	SYM	@ V_{CC} - 1.3V	45	-	55	%
	Output Voltage Levels						V
	Logic '1' Level	V_{OH}	LVPECL Load	V_{CC} - 1.03V	-	V_{CC} - 0.60V	
	Logic '0' Level	V_{OL}	LVPECL Load	V_{CC} - 1.85V	-	V_{CC} - 1.60V	
	Rise and Fall Time	T_R, T_F	@ 20% - 80% Levels	-	0.25	0.6	ns
	LVDS WAVEFORM						
	Output Load	R_L	Between Outputs	-	100	-	Ohms
	Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
	Differential Output Voltage	V_{OD}	RL = 100 Ohms	175	350	454	mV
	Offset Voltage	V_{OS}	LVDS Load	1.20	1.25	1.30	V
	Output Voltage Levels						V
	Logic '1' Level	V_{OH}	LVDS Load	-	1.43	1.60	
	Logic '0' Level	V_{OL}	LVDS Load	0.90	1.10	-	
	Rise and Fall Time	T_R, T_F	@ 20% - 80% Levels	-	-	0.4	ns

Notes:

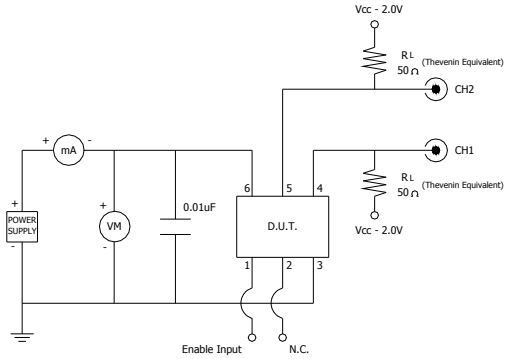
1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and aging.

ENABLE TRUTH TABLE

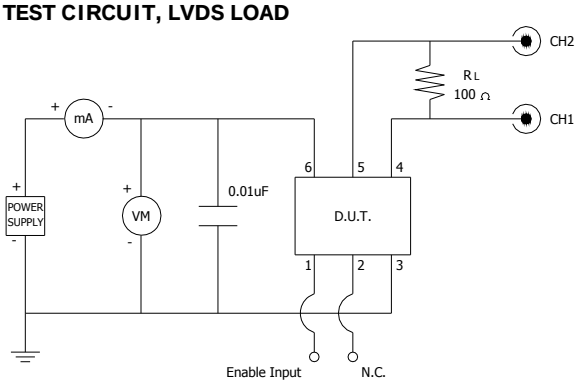
PIN 1	PIN 4 / 5
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

ELECTRICAL CHARACTERISTICS

TEST CIRCUIT, LVPECL LOAD



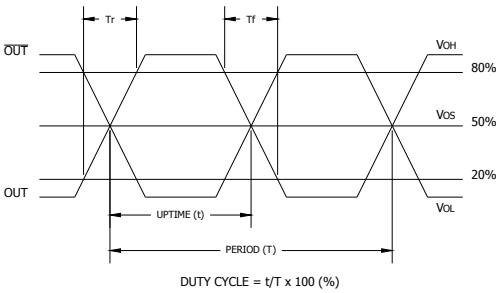
TEST CIRCUIT, LVDS LOAD



D.U.T. PIN ASSIGNMENTS

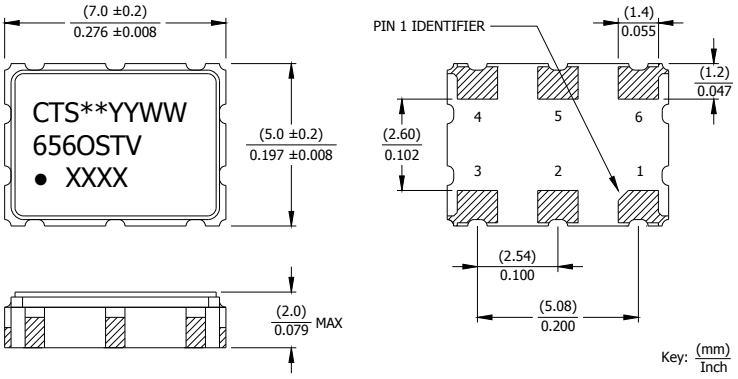
PIN	SYMBOL	DESCRIPTION
1	EOH	Enable
2	N.C.	No Connect
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V_{CC}	Supply Voltage

LVPECL/LVDS OUTPUT WAVEFORM

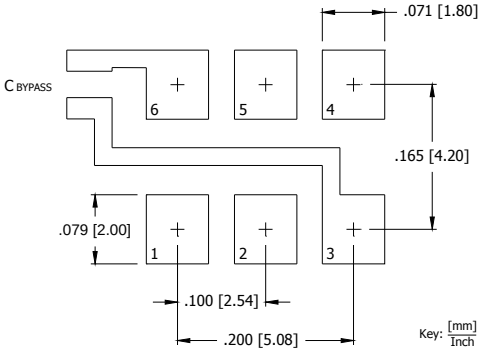


MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



SUGGESTED SOLDER PAD GEOMETRY



MARKING INFORMATION

1. ** - Manufacturing Site Code.
2. YYWW – Date code, YY – year, WW – week.
3. O – Output Type. P = LVPECL, L = LVDS.
4. ST – Frequency stability/temperature code. [Refer to Ordering Information.]
5. V – Voltage code. 3 = 3.3V, 2 = 2.5V
6. xxxx – Frequency Code.
   3-digits, frequencies below 100MHz
   4-digits, frequencies 100MHz or greater.

Refer to document 016-1454-0, Frequency Code Tables.

NOTES

1. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.
2. Termination pads (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
3. Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
4. MSL = 1.

ELECTRICAL CHARACTERISTICS [Addendum]

PHASE NOISE

PARAMETER	SYMBOL	CONDITIONS	TYPICAL	UNIT
LVPECL @ 100MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-70	
		@ 100Hz	-93	
		@ 1kHz	-116	
	-	@ 10kHz	-127	dBc/Hz
		@ 100kHz	-130	
		@ 1MHz	-144	
		@ 10MHz	-155	
		@ 40MHz	-155	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	714	fs
LVPECL @ 312.5MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-81	
		@ 100Hz	-92	
		@ 1kHz	-105	
	-	@ 10kHz	-116	dBc/Hz
		@ 100kHz	-121	
		@ 1MHz	-136	
		@ 10MHz	-153	
		@ 40MHz	-153	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	496	fs
LVPECL @ 800MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-85	
		@ 100Hz	-91	
		@ 1kHz	-97	
	-	@ 10kHz	-107	dBc/Hz
		@ 100kHz	-108	
		@ 1MHz	-126	
		@ 10MHz	-145	
		@ 40MHz	-150	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	782	fs