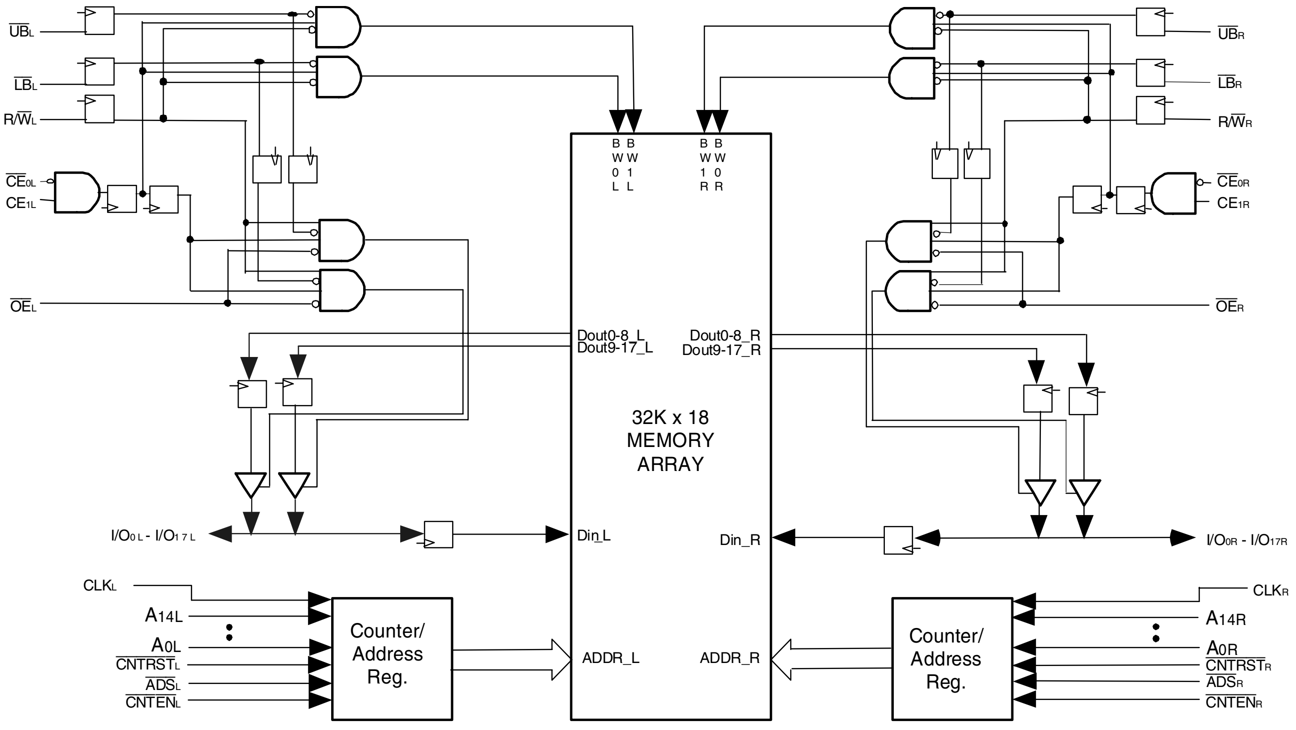
HIGH-SPEED 3.3V 32K x 18 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

IDT70V3379S

Features:

- **True Dual-Port memory cells which allow simultaneous access of the same memory location**
- **High-speed clock to data access**
  - *Commercial: 4.2/5/6ns (max.)*
  - *Industrial: 5ns (max)*
- **Pipelined output mode**
- **Counter enable and reset features**
- **Dual chip enables allow for depth expansion without additional logic**
- **Full synchronous operation on both ports**
  - *7.5ns cycle time, 133MHz operation (9.6 Gbps bandwidth)*
  - *Fast 4.2ns clock to data out*
  - *1.8ns setup to clock and 0.7ns hold on all control, data, and address inputs @ 133MHz*
  - *Data input, address, byte enable and control registers*
  - *Self-timed write allows fast cycle time*
- **Separate byte controls for multiplexed bus and bus matching compatibility**
- **LVTTL- compatible, single 3.3V (±150mV) power supply for core**
- **LVTTL- compatible, selectable 3.3V (±150mV)/2.5V (±125mV) power supply for I/Os and control signals on each port**
- **Industrial temperature range (-40°C to +85°C) is available for selected speeds**
- **Available in a 128-pin Thin Quad Plastic Flatpack (TQFP) and 208-pin fine pitch Ball Grid Array, and 256-pin Ball Grid Array**
- **Green parts available, see ordering information**

Functional Block Diagram



4833 tbl 01

FEBRUARY 2006

Description:

The IDT70V3379 is a high-speed 32K x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3379 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE$_1$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3379 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (V$_{DD}$) remains at 3.3V.

Pin Configuration(1,2,3,4)

12/05/01

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	I/O$_{9L}$	NC	V$_{SS}$	NC	NC	NC	A$_{12L}$	A$_{8L}$	NC	V$_{DD}$	CLK$_L$	$\overline{CNTEN}_L$	A$_{4L}$	A$_{0L}$	OPT$_L$	NC	V$_{SS}$
B	NC	V$_{SS}$	NC	V$_{SS}$	NC	A$_{13L}$	A$_{9L}$	NC	$\overline{CE}_{0L}$	V$_{SS}$	$\overline{ADS}_L$	A$_{5L}$	A$_{1L}$	V$_{SS}$	V$_{DDQR}$	I/O$_{8L}$	NC
C	V$_{DDQL}$	I/O$_{9R}$	V$_{DDQR}$	V$_{DD}$	NC	A$_{14L}$	A$_{10L}$	$\overline{UB}_L$	CE$_{1L}$	V$_{SS}$	R/$\overline{W}_L$	A$_{6L}$	A$_{2L}$	V$_{DD}$	I/O$_{8R}$	NC	V$_{SS}$
D	NC	V$_{SS}$	I/O$_{10L}$	NC	NC	A$_{11L}$	A$_{7L}$	$\overline{LB}_L$	V$_{DD}$	$\overline{OE}_L$	$\overline{CNTRST}_L$	A$_{3L}$	V$_{DD}$	NC	V$_{DDQL}$	I/O$_{7L}$	I/O$_{7R}$
E	I/O$_{11L}$	NC	V$_{DDQR}$	I/O$_{10R}$										I/O$_{6L}$	NC	V$_{SS}$	NC
F	V$_{DDQL}$	I/O$_{11R}$	NC	V$_{SS}$										V$_{SS}$	I/O$_{6R}$	NC	V$_{DDQR}$
G	NC	V$_{SS}$	I/O$_{12L}$	NC										NC	V$_{DDQL}$	I/O$_{5L}$	NC
H	V$_{DD}$	NC	V$_{DDQR}$	I/O$_{12R}$										V$_{DD}$	NC	V$_{SS}$	I/O$_{5R}$
J	V$_{DDQL}$	V$_{DD}$	V$_{SS}$	V$_{SS}$										V$_{SS}$	V$_{DD}$	V$_{SS}$	V$_{DDQR}$
K	I/O$_{14R}$	V$_{SS}$	I/O$_{13R}$	V$_{SS}$										I/O$_{3R}$	V$_{DDQL}$	I/O$_{4R}$	V$_{SS}$
L	NC	I/O$_{14L}$	V$_{DDQR}$	I/O$_{13L}$										NC	I/O$_{3L}$	V$_{SS}$	I/O$_{4L}$
M	V$_{DDQL}$	NC	I/O$_{15R}$	V$_{SS}$										V$_{SS}$	NC	I/O$_{2R}$	V$_{DDQR}$
N	NC	V$_{SS}$	NC	I/O$_{15L}$										I/O$_{1R}$	V$_{DDQL}$	NC	I/O$_{2L}$
P	I/O$_{16R}$	I/O$_{16L}$	V$_{DDQR}$	NC	NC	NC	A$_{12R}$	A$_{8R}$	NC	V$_{DD}$	CLK$_R$	$\overline{CNTEN}_R$	A$_{4R}$	NC	I/O$_{1L}$	V$_{SS}$	NC
R	V$_{SS}$	NC	I/O$_{17R}$	NC	NC	A$_{13R}$	A$_{9R}$	NC	$\overline{CE}_{0R}$	V$_{SS}$	$\overline{ADS}_R$	A$_{5R}$	A$_{1R}$	V$_{SS}$	V$_{DDQL}$	I/O$_{0R}$	V$_{DDQR}$
T	NC	I/O$_{17L}$	V$_{DDQL}$	V$_{SS}$	NC	A$_{14R}$	A$_{10R}$	$\overline{UB}_R$	CE$_{1R}$	V$_{SS}$	R/$\overline{W}_R$	A$_{6R}$	A$_{2R}$	V$_{SS}$	NC	V$_{SS}$	NC
U	V$_{SS}$	NC	V$_{DD}$	NC	NC	A$_{11R}$	A$_{7R}$	$\overline{LB}_R$	V$_{DD}$	$\overline{OE}_R$	$\overline{CNTRST}_R$	A$_{3R}$	A$_{0R}$	V$_{DD}$	OPT$_R$	NC	I/O$_{0L}$

70V3379BF
BF-208(5)

208-Pin fpBGA
Top View(6)

4833 tbl 02

NOTES:

1. All V$_{DD}$ pins must be connected to 3.3V power supply.
2. All V$_{DDQ}$ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V$_{IH}$ (3.3V), and 2.5V if OPT pin for that port is set to V$_{IL}$ (0V).
3. All V$_{SS}$ pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm, with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration[1,2,3,4] (con't.)

70V3379BC
BC-256[5]

256-Pin BGA
Top View[6]

12/05/01

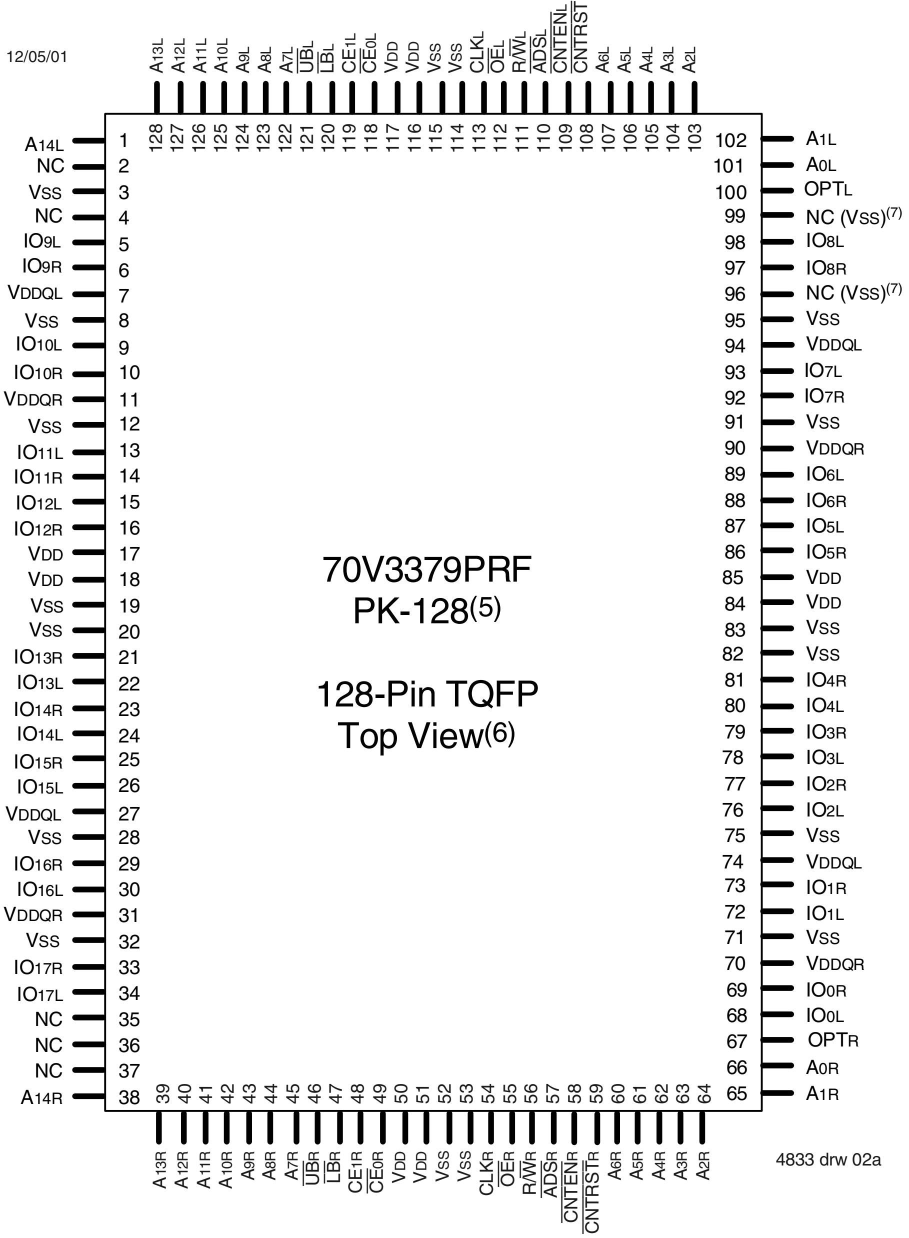
A1 NC	A2 NC	A3 NC	A4 NC	A5 A_{14L}	A6 A_{11L}	A7 A_{8L}	A8 NC	A9 CE_{1L}	A10 $\overline{OE}_L$	A11 $\overline{CNTEN}_L$	A12 A_{5L}	A13 A_{2L}	A14 A_{0L}	A15 NC	A16 NC
B1 NC	B2 NC	B3 NC	B4 NC	B5 NC	B6 A_{12L}	B7 A_{9L}	B8 $\overline{UB}_L$	B9 $\overline{CE}_{0L}$	B10 $R/\overline{W}_L$	B11 $\overline{CNTRST}_L$	B12 A_{4L}	B13 A_{1L}	B14 V_{DD}	B15 NC	B16 NC
C1 NC	C2 I/O$_{9L}$	C3 V_{SS}	C4 NC	C5 A_{13L}	C6 A_{10L}	C7 A_{7L}	C8 NC	C9 $\overline{LB}_L$	C10 CLK_L	C11 $\overline{ADS}_L$	C12 A_{6L}	C13 A_{3L}	C14 OPT_L	C15 NC	C16 I/O$_{8L}$
D1 NC	D2 I/O$_{9R}$	D3 NC	D4 V_{DD}	D5 V_{DDQL}	D6 V_{DDQL}	D7 V_{DDQR}	D8 V_{DDQR}	D9 V_{DDQL}	D10 V_{DDQL}	D11 V_{DDQR}	D12 V_{DDQR}	D13 V_{DD}	D14 NC	D15 NC	D16 I/O$_{8R}$
E1 I/O$_{10R}$	E2 I/O$_{10L}$	E3 NC	E4 V_{DDQL}	E5 V_{DD}	E6 V_{DD}	E7 V_{SS}	E8 V_{SS}	E9 V_{SS}	E10 V_{SS}	E11 V_{DD}	E12 V_{DD}	E13 V_{DDQR}	E14 NC	E15 I/O$_{7L}$	E16 I/O$_{7R}$
F1 I/O$_{11L}$	F2 NC	F3 I/O$_{11R}$	F4 V_{DDQL}	F5 V_{DD}	F6 V_{SS}	F7 V_{SS}	F8 V_{SS}	F9 V_{SS}	F10 V_{SS}	F11 V_{SS}	F12 V_{DD}	F13 V_{DDQR}	F14 I/O$_{6R}$	F15 NC	F16 I/O$_{6L}$
G1 NC	G2 NC	G3 I/O$_{12L}$	G4 V_{DDQR}	G5 V_{SS}	G6 V_{SS}	G7 V_{SS}	G8 V_{SS}	G9 V_{SS}	G10 V_{SS}	G11 V_{SS}	G12 V_{SS}	G13 V_{DDQL}	G14 I/O$_{5L}$	G15 NC	G16 NC
H1 NC	H2 I/O$_{12R}$	H3 NC	H4 V_{DDQR}	H5 V_{SS}	H6 V_{SS}	H7 V_{SS}	H8 V_{SS}	H9 V_{SS}	H10 V_{SS}	H11 V_{SS}	H12 V_{SS}	H13 V_{DDQL}	H14 NC	H15 NC	H16 I/O$_{5R}$
J1 I/O$_{13L}$	J2 I/O$_{14R}$	J3 I/O$_{13R}$	J4 V_{DDQL}	J5 V_{SS}	J6 V_{SS}	J7 V_{SS}	J8 V_{SS}	J9 V_{SS}	J10 V_{SS}	J11 V_{SS}	J12 V_{SS}	J13 V_{DDQR}	J14 I/O$_{4R}$	J15 I/O$_{3R}$	J16 I/O$_{4L}$
K1 NC	K2 NC	K3 I/O$_{14L}$	K4 V_{DDQL}	K5 V_{SS}	K6 V_{SS}	K7 V_{SS}	K8 V_{SS}	K9 V_{SS}	K10 V_{SS}	K11 V_{SS}	K12 V_{SS}	K13 V_{DDQR}	K14 NC	K15 NC	K16 I/O$_{3L}$
L1 I/O$_{15L}$	L2 NC	L3 I/O$_{15R}$	L4 V_{DDQR}	L5 V_{DD}	L6 V_{SS}	L7 V_{SS}	L8 V_{SS}	L9 V_{SS}	L10 V_{SS}	L11 V_{SS}	L12 V_{DD}	L13 V_{DDQL}	L14 I/O$_{2L}$	L15 NC	L16 I/O$_{2R}$
M1 I/O$_{16R}$	M2 I/O$_{16L}$	M3 NC	M4 V_{DDQR}	M5 V_{DD}	M6 V_{DD}	M7 V_{SS}	M8 V_{SS}	M9 V_{SS}	M10 V_{SS}	M11 V_{DD}	M12 V_{DD}	M13 V_{DDQL}	M14 I/O$_{1R}$	M15 I/O$_{1L}$	M16 NC
N1 NC	N2 I/O$_{17R}$	N3 NC	N4 V_{DD}	N5 V_{DDQR}	N6 V_{DDQR}	N7 V_{DDQL}	N8 V_{DDQL}	N9 V_{DDQR}	N10 V_{DDQR}	N11 V_{DDQL}	N12 V_{DDQL}	N13 V_{DD}	N14 NC	N15 I/O$_{0R}$	N16 NC
P1 NC	P2 I/O$_{17L}$	P3 NC	P4 NC	P5 A_{13R}	P6 A_{10R}	P7 A_{7R}	P8 NC	P9 $\overline{LB}_R$	P10 CLK_R	P11 $\overline{ADS}_R$	P12 A_{6R}	P13 A_{3R}	P14 NC	P15 NC	P16 I/O$_{0L}$
R1 NC	R2 NC	R3 NC	R4 NC	R5 NC	R6 A_{12R}	R7 A_{9R}	R8 $\overline{UB}_R$	R9 $\overline{CE}_{0R}$	R10 $R/\overline{W}_R$	R11 $\overline{CNTRST}_R$	R12 A_{4R}	R13 A_{1R}	R14 OPT_R	R15 NC	R16 NC
T1 NC	T2 NC	T3 NC	T4 NC	T5 A_{14R}	T6 A_{11R}	T7 A_{8R}	T8 NC	T9 CE_{1R}	T10 $\overline{OE}_R$	T11 $\overline{CNTEN}_R$	T12 A_{5R}	T13 A_{2R}	T14 A_{0R}	T15 NC	T16 NC

4833 drw 02c

NOTES:

1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration(1,2,3,4) (con't.)



NOTES:

1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 14mm x 20mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.
7. In the 70V3379 (32K x 18) and 70V3389 (64K x 18), pins 96 and 99 are NC. The upgrade devices 70V3399 (128K x 18) and 70V3319 (256K x 18) assign these pins as Vss. Customers who plan to take advantage of the upgrade path should treat these pins as VSS on the 70V3379 and 70V3389. If no upgrade is needed, the pins can be treated as NC.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{14L}	A_{0R} - A_{14R}	Address
I/O_{0L} - I/O_{17L}	I/O_{0R} - I/O_{17R}	Data Input/Output
CLK_L	CLK_R	Clock
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset
UB_L - LB_L	UB_R - LB_R	Byte Enables (9-bit bytes)
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V or 2.5V)[1]
OPT_L	OPT_R	Option for selecting V_{DDQX}[1,2]
V_{DD}		Power (3.3V)[1]
V_{SS}		Ground (0V)

4833 tbl 01

NOTES:
1. V_{DD}, OPT_X, and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
2. OPT_X selects the operating voltage levels for the I/Os and controls on that port. If OPT_X is set to VIH (3.3V), then that port's I/Os and controls will operate at 3.3V levels and V_{DDQX} must be supplied at 3.3V. If OPT_X is set to VIL (0V), then that port's I/Os and controls will operate at 2.5V levels and V_{DDQX} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.

Truth Table I—Read/Write and Enable Control[1,2,3]

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$\overline{UB}$	$\overline{LB}$	$R/\overline{W}$	Upper Byte I/O_{9-18}	Lower Byte I/O_{0-8}	MODE
X	↑	L	H	H	H	X	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	L	L	High-Z	D_{IN}	Write to Lower Byte Only
X	↑	L	H	L	H	L	D_{IN}	High-Z	Write to Upper Byte Only
X	↑	L	H	L	L	L	D_{IN}	D_{IN}	Write to Both Bytes
L	↑	L	H	H	L	H	High-Z	D_{OUT}	Read Lower Byte Only
L	↑	L	H	L	H	H	D_{OUT}	High-Z	Read Upper Byte Only
L	↑	L	H	L	L	H	D_{OUT}	D_{OUT}	Read Both Bytes
H	↑	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

4833 tbl 02

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = X.
3. $\overline{OE}$ is an asynchronous input signal.

Truth Table II—Address Counter Control[1,2]

Address	Previous Address	Addr Used	CLK[6]	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNTRST}$	I/O[3]	MODE
X	X	0	↑	X	X	L[4]	$D_{I/O}(0)$	Counter Reset to Address 0
An	X	An	↑	L[4]	X	H	$D_{I/O}$ (n)	External Address Used
An	Ap	Ap	↑	H	H	H	$D_{I/O}(p)$	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	↑	H	L[5]	H	$D_{I/O}(p+1)$	Counter Enabled—Internal Address generation

4833 tbl 03

NOTES:

1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. Read and write operations are controlled by the appropriate setting of R/$\overline{W}$, $\overline{CE}_0$, CE_1, $\overline{BE}$n and $\overline{OE}$.
3. Outputs are in Pipelined mode: the data out will be delayed by one cycle.
4. $\overline{ADS}$ and $\overline{CNTRST}$ are independent of all other memory control signals including $\overline{CE}_0$, CE_1 and $\overline{BE}$n
5. The address counter advances if $\overline{CNTEN}$ = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE}_0$, CE_1, $\overline{BE}$n.

Recommended Operating Temperature and Supply Voltage[1]

Grade	Ambient Temperature	GND	V_{DD}
Commercial	0^{o}C to $+70^{o}$C	0V	3.3V ± 150mV
Industrial	-40^{o}C to $+85^{o}$C	0V	3.3V ± 150mV

4833 tbl 04

NOTES:

1. This is the parameter T_A. This is the "instant on" case tempereature.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

4833 tbl 06

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \geq V_{DD}$ + 150mV.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V_{DDQ}	I/O Supply Voltage[3]	2.375	2.5	2.625	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage[3] (Address & Control Inputs)	1.7	—	V_{DDQ} + 125mV[2]	V
V_{IH}	Input High Voltage - I/O[3]	1.7	—	V_{DDQ} + 125mV[2]	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.7	V

4833 tbl 05a

NOTES:

1. $V_{IL} \geq$ -1.5V for pulse width less than 10 ns.
2. V_{TERM} must not exceed V_{DDQ} + 125mV.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IL} (0V), and V_{DDQX} for that port must be supplied as indicated above.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V_{DDQ}	I/O Supply Voltage[3]	3.15	3.3	3.45	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage (Address & Control Inputs)[3]	2.0	—	V_{DDQ} + 150mV[2]	V
V_{IH}	Input High Voltage - I/O[3]	2.0	—	V_{DDQ} + 150mV[2]	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.8	V

4833 tbl 05b

NOTES:

1. $V_{IL} \geq$ -1.5V for pulse width less than 10 ns.
2. V_{TERM} must not exceed V_{DDQ} + 150mV.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IH} (3.3V), and V_{DDQX} for that port must be supplied as indicated above.

Capacitance[1]

(T_A = +25°C, F = 1.0MHz) TQFP ONLY

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
C_{OUT}[3]	Output Capacitance	V_{OUT} = 3dV	10.5	pF

4833 tbl 07

NOTES:

1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C_{OUT} also references $C_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V3379S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{DDQ} = Max., V_{IN} = 0V to V_{DDQ}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{DDQ}	—	10	µA
V_{OL} (3.3V)	Output Low Voltage[2]	I_{OL} = +4mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage[2]	I_{OH} = -4mA, V_{DDQ} = Min.	2.4	—	V
V_{OL} (2.5V)	Output Low Voltage[2]	I_{OL} = +2mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (2.5V)	Output High Voltage[2]	I_{OH} = -2mA, V_{DDQ} = Min.	2.0	—	V

4833 tbl 08

NOTE:

1. At $V_{DD} \leq$ - 2.0V input leakages are undefined.
2. V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.4 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range$^{(3)}$ (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Condition	Version	70V3379S4 Com'l Only		70V3379S5 Com'l & Ind		70V3379S6 Com'l Only		Unit
				Typ.$^{(4)}$	Max.	Typ.$^{(4)}$	Max.	Typ.$^{(4)}$	Max.	
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, Outputs Disabled, f = $f_{MAX}$$^{(1)}$	COM'L S	375	460	285	360	245	310	mA
			IND S	—	—	285	415	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = $f_{MAX}$$^{(1)}$	COM'L S	145	190	105	145	95	125	mA
			IND S	—	—	105	175	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = $V_{IH}$$^{(5)}$ Active Port Outputs Disabled, f=$f_{MAX}$$^{(1)}$	COM'L S	265	325	190	260	175	225	mA
			IND S	—	—	190	300	—	—	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ $\geq$ V_{DD} - 0.2V, V_{IN} $\geq$ V_{DD} - 0.2V or V_{IN} $\leq$ 0.2V, f = 0$^{(2)}$	COM'L S	6	15	6	15	6	15	mA
			IND S	—	—	6	30	—	—	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"}$ $\leq$ 0.2V and $\overline{CE}_{"B"}$ $\geq$ V_{DD} - 0.2V$^{(5)}$ V_{IN} $\geq$ V_{DD} - 0.2V or V_{IN} $\leq$ 0.2V, Active Port, Outputs Disabled, f = $f_{MAX}$$^{(1)}$	COM'L S	265	325	180	260	170	225	mA
			IND S	—	—	180	300	—	—	

4833 tbl 09

NOTES:

1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{DD} = 3.3V, T_A = 25°C for Typ, and are not production tested. $I_{DD\ DC}$(f=0) = 120mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X$ $\leq$ 0.2V means $\overline{CE}_{0X}$ $\leq$ 0.2V and CE_{1X} $\geq$ V_{CC} - 0.2V
   $\overline{CE}_X$ $\geq$ V_{CC} - 0.2V means $\overline{CE}_{0X}$ $\geq$ V_{CC} - 0.2V or CE_{1X} - 0.2V
   "X" represents "L" for left port or "R" for right port.

AC Test Conditions

Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.35V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.35V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1, 2, and 3

4833 tbl 10

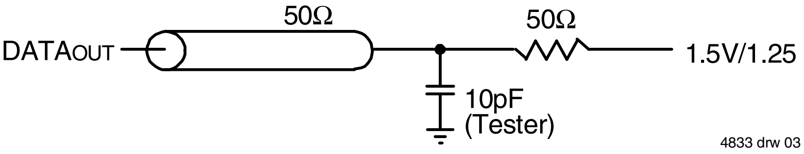


Figure 1. AC Output Test load.

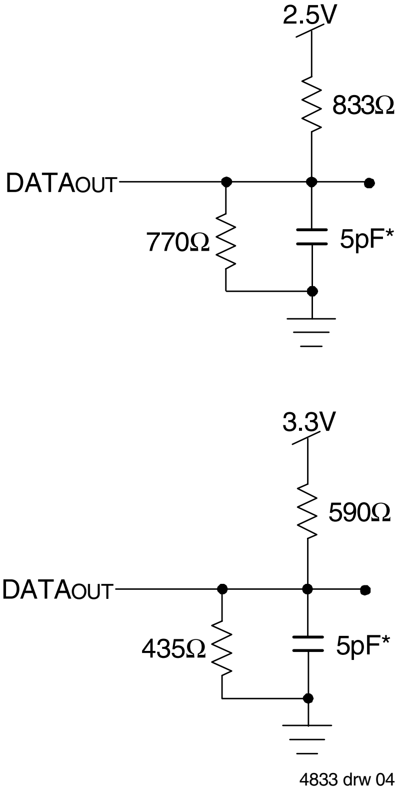


Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.

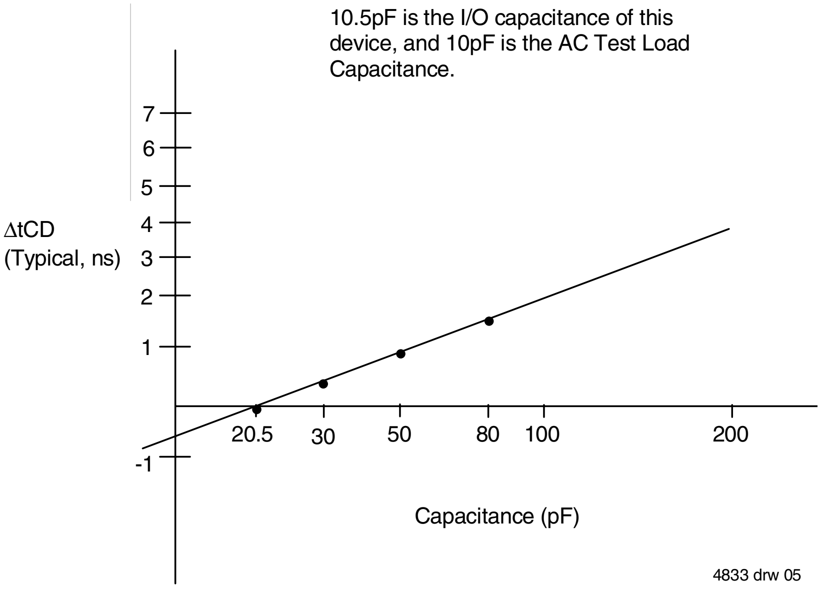


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)(1,2)

(V_{DD} = 3.3V ± 150mV, T_A = 0°C to +70°C)

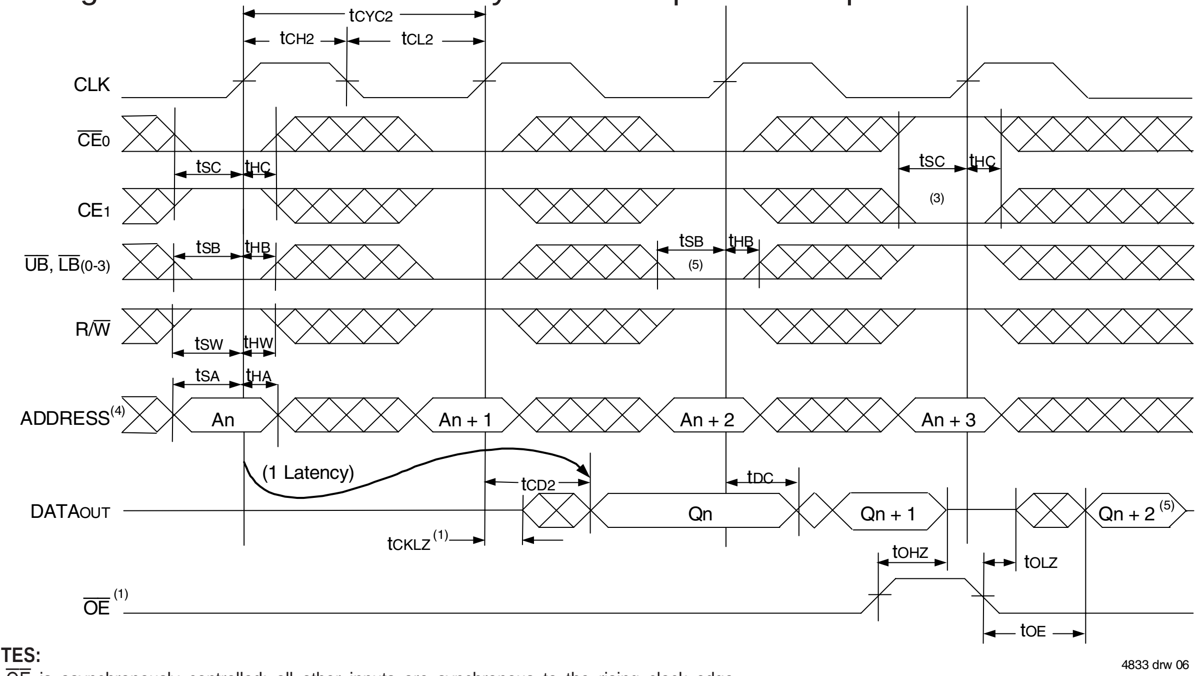
		70V3379S4 Com'l Only		70V3379S5 Com'l & Ind		70V3379S6 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{CYC2}	Clock Cycle Time (Pipelined)	7.5	—	10	—	12	—	ns
t_{CH2}	Clock High Time (Pipelined)	3	—	4	—	5	—	ns
t_{CL2}	Clock Low Time (Pipelined)	3	—	4	—	5	—	ns
t_R	Clock Rise Time	—	3	—	3	—	3	ns
t_F	Clock Fall Time	—	3	—	3	—	3	ns
t_{SA}	Address Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HA}	Address Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SC}	Chip Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HC}	Chip Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SB}	Byte Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HB}	Byte Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SW}	R/$\overline{W}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HW}	R/$\overline{W}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SD}	Input Data Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HD}	Input Data Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SRST}	$\overline{CNTRST}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{OE}(1)	Output Enable to Data Valid	—	4	—	5	—	6	ns
t_{OLZ}	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t_{OHZ}	Output Enable to Output High-Z	1	4	1	4.5	1	5	ns
t_{CD2}	Clock to Data Valid (Pipelined)	—	4.2	—	5	—	6	ns
t_{DC}	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t_{CKHZ}	Clock High to Output High-Z	1	3	1	4.5	1.5	6	ns
t_{CKLZ}	Clock High to Output Low-Z	1	—	1	—	1	—	ns
Port-to-Port Delay								
t_{CO}	Clock-to-Clock Offset	6	—	8	—	10	—	ns

4833 tbl 11

NOTES:

1. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$).
2. These values are valid for either level of V_{DDQ} (3.3V/2.5V). See page 4 for details on selecting the desired I/O voltage levels for each port.

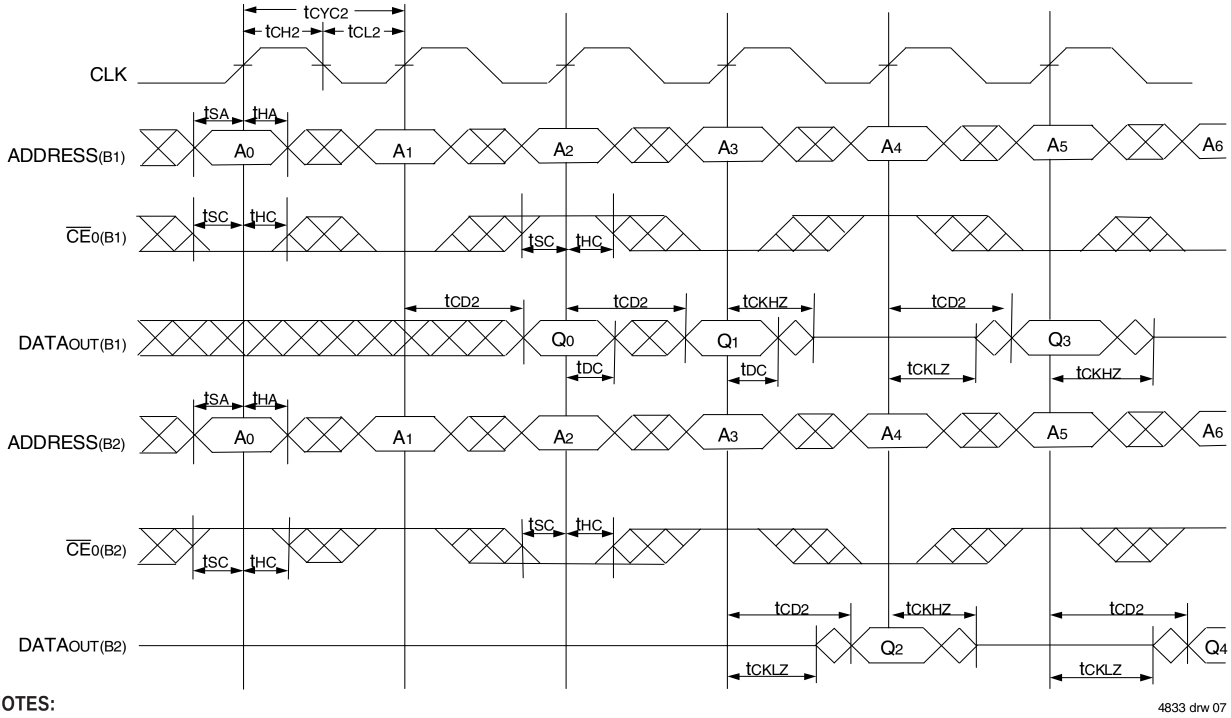
Timing Waveform of Read Cycle for Pipelined Operation(2)



NOTES:

1. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = V_{IH}, CE_1 = V_{IL}, $\overline{UB}$, $\overline{LB}$ = V_{IH} following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{UB}$ or $\overline{LB}$ was HIGH, then the appropriate Byte of $DATA_{OUT}$ for Qn + 2 would be disabled (High-Impedance state).

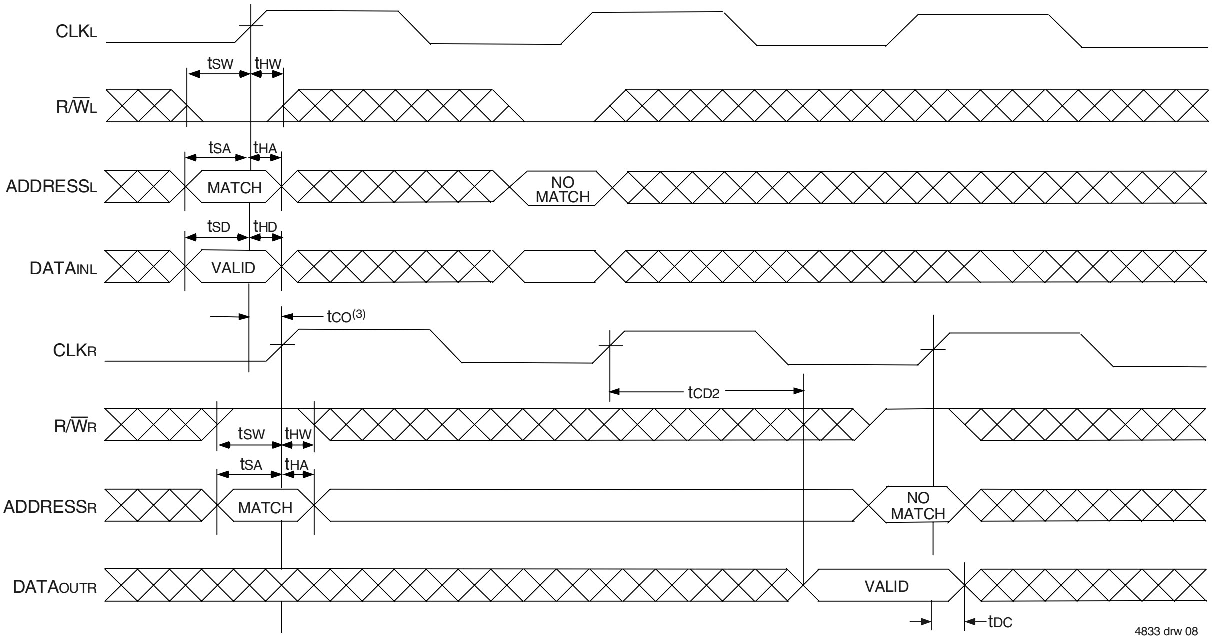
Timing Waveform of a Multi-Device Pipelined Read(1,2)



NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3379 for this waveform, and are setup for depth expansion in this example. $ADDRESS_{(B1)}$ = $ADDRESS_{(B2)}$ in this situation.
2. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$, and $\overline{ADS}$ = V_{IL}; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.

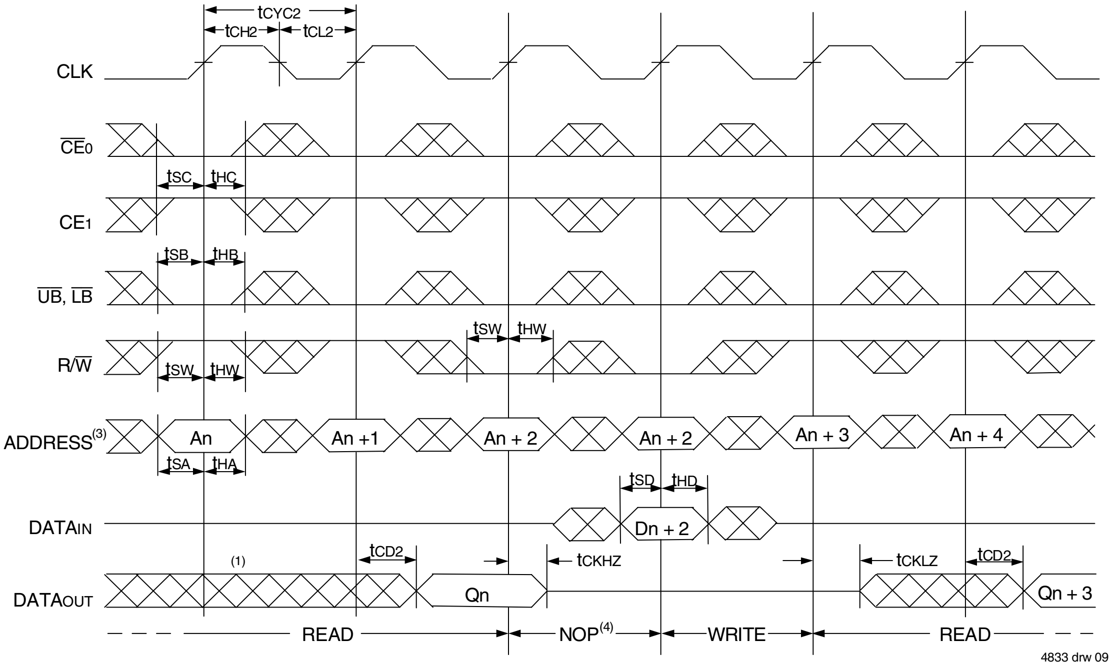
Timing Waveform of Left Port Write to Pipelined Right Port Read(1,2)



NOTES:

1. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from right port read is not valid until following right port clock cycle (ie, time from write to valid read on opposite port will be t_{CO} + 2 t_{CYC2} + t_{CD2}). If t_{CO} > minimum, then data from right port read is available on first right port clock cycle (ie, time from write to valid read on opposite port will be t_{CO} + t_{CYC} + t_{CD2}).

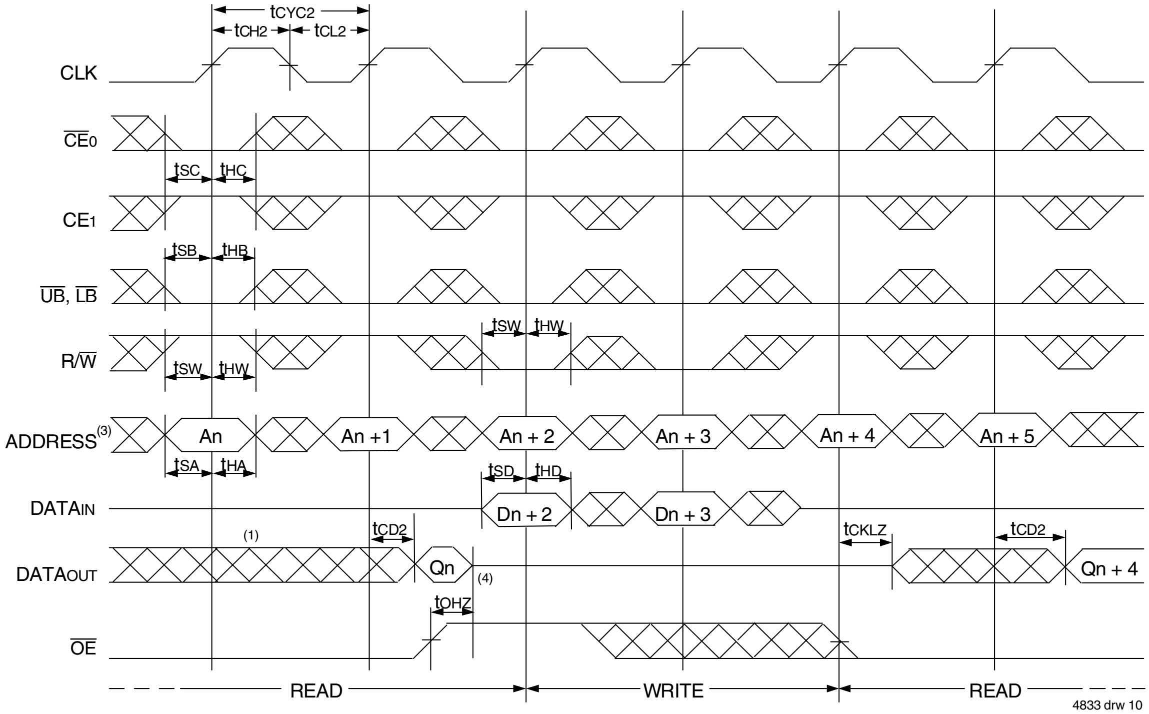
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = V_{IL})(2)



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

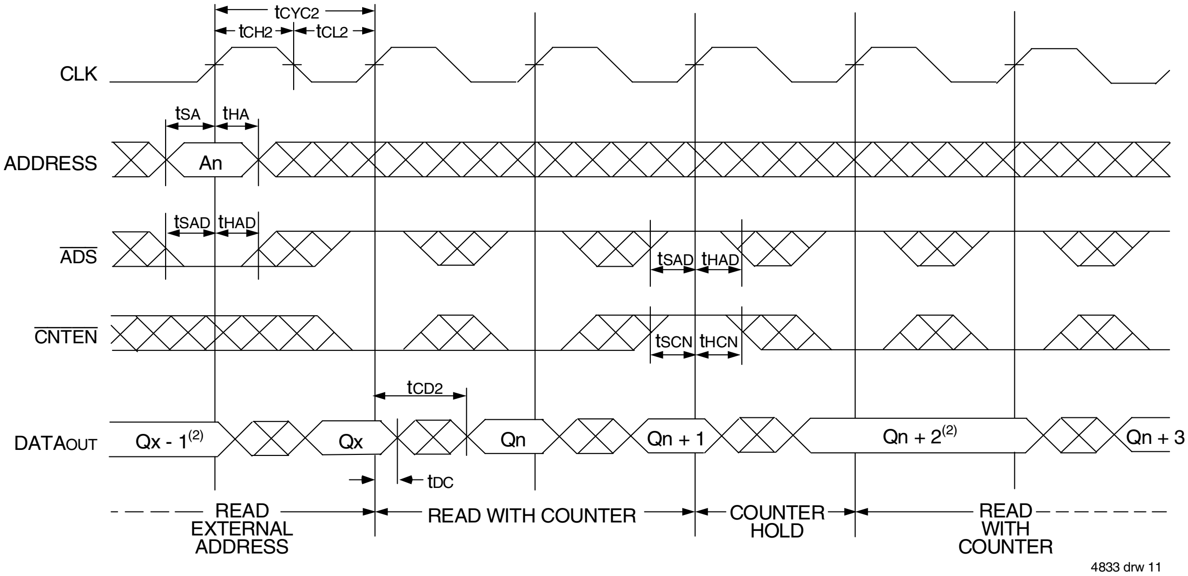
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{\text{OE}}$ Controlled)(2)



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{\text{CE}}_0$, $\overline{\text{UB}}$, $\overline{\text{LB}}$, and $\overline{\text{ADS}}$ = V_{IL}; CE_1, $\overline{\text{CNTEN}}$, and $\overline{\text{CNTRST}}$ = V_{IH}.
3. Addresses do not have to be accessed sequentially since $\overline{\text{ADS}}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

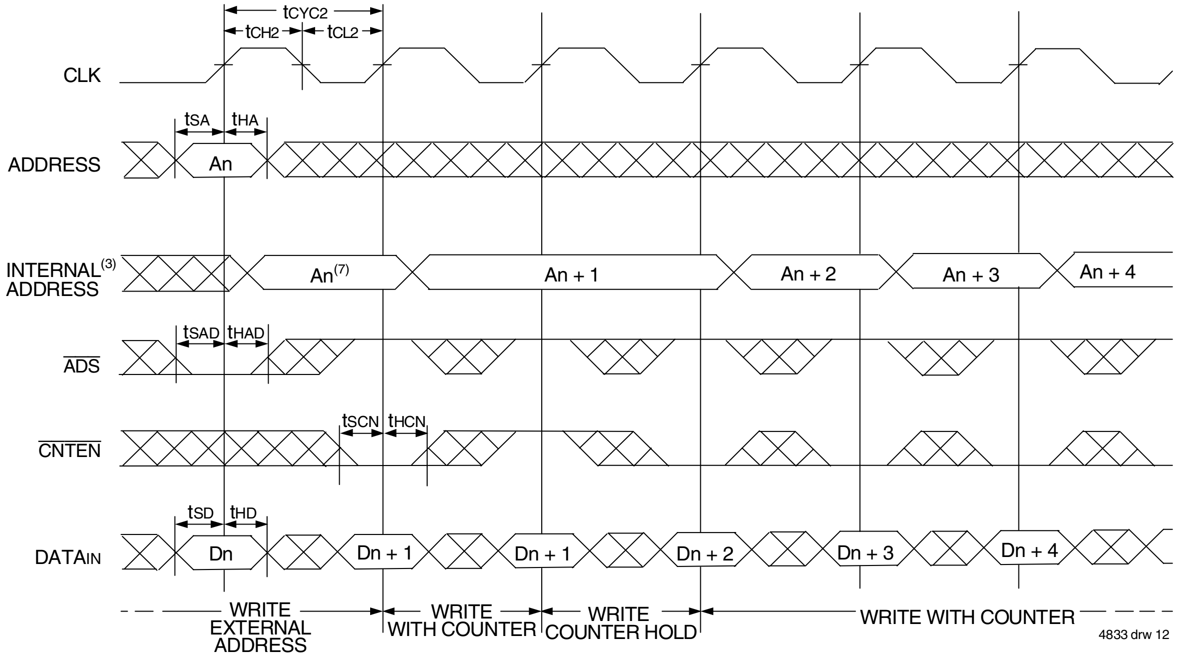
Timing Waveform of Pipelined Read with Address Counter Advance(1)



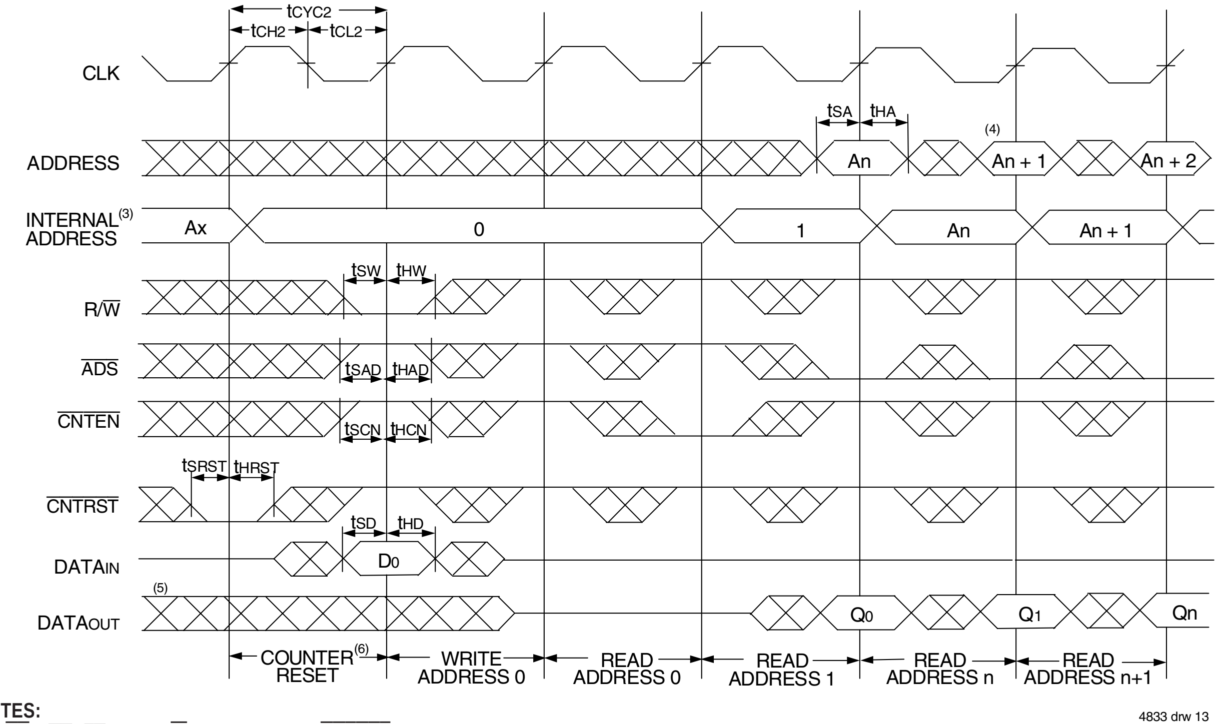
NOTES:

1. $\overline{\text{CE}}_0$, $\overline{\text{OE}}$, $\overline{\text{UB}}$, $\overline{\text{LB}}$ = V_{IL}; CE_1, R/$\overline{\text{W}}$, and $\overline{\text{CNTRST}}$ = V_{IH}.
2. If there is no address change via $\overline{\text{ADS}}$ = V_{IL} (loading a new address) or $\overline{\text{CNTEN}}$ = V_{IL} (advancing the address), i.e. $\overline{\text{ADS}}$ = V_{IH} and $\overline{\text{CNTEN}}$ = V_{IH}, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance(1)



Timing Waveform of Counter Reset(2)



NOTES:

1. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{CNTRST}$ = V_{IH}.
2. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$ = V_{IL}; CE_1 = V_{IH}.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle: ADDR 0 will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN}$ = V_{IL} advances Internal Address from ‘An’ to ‘An +1’. The transition shown indicates the time required for the counter to advance. The ‘An +1’Address is written to during this cycle.

Functional Description

The IDT70V3379 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3379s for depth expansion configurations. Two cycles are required with $\overline{CE}_0$ LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT70V3379 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3379 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 36-bits or wider.

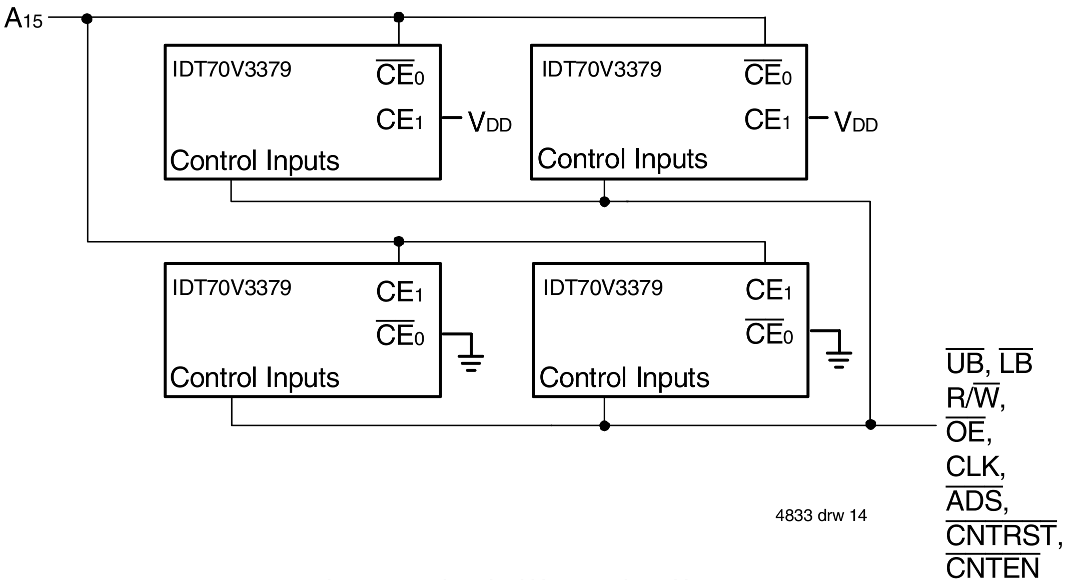
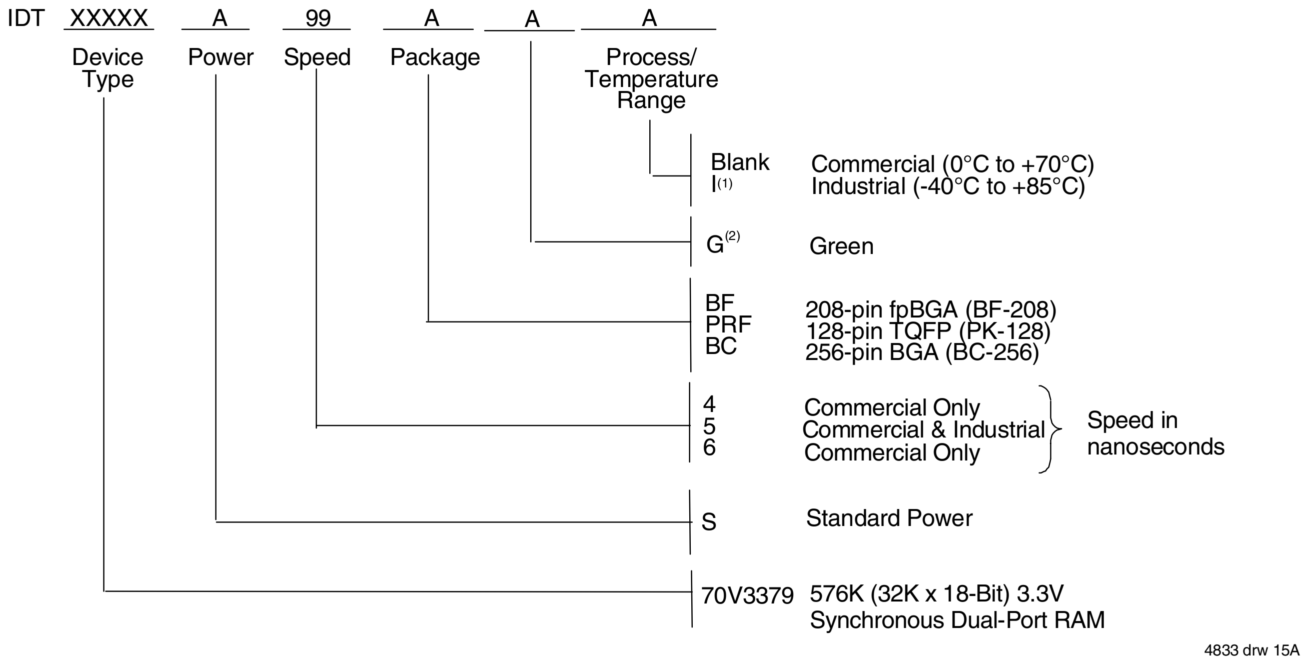


Figure 4. Depth and Width Expansion with IDT70V3379

Ordering Information



NOTES:

1. Contact your local sales office for Industrial temp range in other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

Datasheet Document History

1/18/98:	Initial Public Release	
3/15/99:	Page 10	Additional Notes
4/28/99:	Added fpBGA package	
6/8/99:	Page 2	Changed package body height from 1.5mm to 1.4mm
6/11/99:	Page 5	Deleted note 6 for Table II
7/14/99:	Page 2	Corrected pin to T3 to VDDQL
8/4/99:	Page 6 Improved power numbers	
10/4/99:	Upgraded speed to 133MHz, added 2.5V I/O capability	
11/12/99:	Replaced IDT logo	
2/28/00:	Added new BGA package, added full 2.5V interface capability	
5/1/00:	Page 2	Added ball pitch
	Page 3	Renamed pins
	Page 6	Made corrections to Truth Table
	Page 9	Changed Ω numbers in figure 2
6/7/00:	Page 4	Added information to pin and pin notes
	Page 6	Increased storage temperature parameter Clarified TA Parameter
	Page 8	DC Electrical parameters–changed wording from "open" to "disabled" Removed note 7 on DC Electrical Characteristics table

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	Page 3	Renamed pins
	Page 6	Made corrections to Truth Table
	Page 9	Changed Ω numbers in figure 2
06/07/00:	Page 4	Added information to pin and pin notes
	Page 6	Increased storage temperature parameter
		Clarified T_A Parameter
	Page 8	DC Electrical parameters–changed wording from "open" to "disabled"
		Removed note 7 on DC Electrical Characteristics table
01/10/01:	Page 1	Changed 64K to 32K in block drawing
		Removed Preliminary status
04/10/01:		Added Industrial Temperature Ranges and removed related notes
12/12/01:	Page 2, 3& 4	Added date revision to pin configurations
	Page 6	Removed industrial temp footnote from table 04
	Page 8 & 10	Removed industrial temp for 6ns from DC & AC Electrical Characteristics
	Page 16	Removed industrial temp from 6ns in ordering information
		Added industrial temp footnote
	Page 1 & 17	Replaced TM logo with ® logo
01/05/06:	Page 1	Added green availability to features
	Page 16	Added green indicator to ordering information
02/08/06:	Page 5	Changed footnote 2 for Truth Table I from $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = V_{IH} to $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = X

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