

DATA SHEET

74ABT377A

Octal D-type flip-flop with enable

Product specification
Replaces data sheet 74ABT377 of 1995 Sep 06
IC23 Data Handbook

1997 Feb 26

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FEATURES

- Ideal for addressable register applications
- 8-bit positive edge-triggered register
- Enable for address and data synchronization applications
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up reset

DESCRIPTION

The 74ABT377A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT377A has 8 edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Enable (\bar{E}) input is Low.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The \bar{E} input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

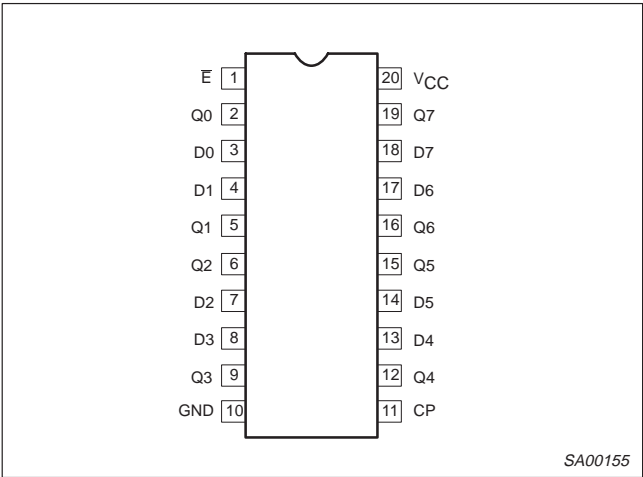
QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb} = 25^{\circ}\text{C}; GND = 0V$ | TYPICAL | UNIT |
|------------------------|-------------------------------|--|------------|------|
| t_{PLH} t_{PHL} | Propagation delay CP to Qn | $C_L = 50\text{pF}; V_{CC} = 5V$ | 3.1 3.6 | ns |
| C_{IN} | Input capacitance | $V_I = 0V \text{ or } V_{CC}$ | 4 | pF |
| I_{CCH} | Total current supply | Outputs High; $V_{CC} = 5.5V$ | 500 | nA |

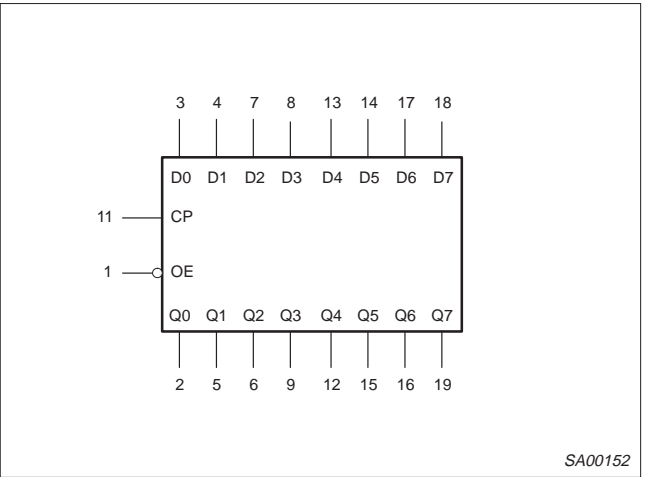
ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|-----------------------------|--|-----------------------|----------------|------------|
| 20-Pin Plastic DIP | -40°C to $+85^{\circ}\text{C}$ | 74ABT377A N | 74ABT377A N | SOT146-1 |
| 20-Pin plastic SO | -40°C to $+85^{\circ}\text{C}$ | 74ABT377A D | 74ABT377A D | SOT163-1 |
| 20-Pin Plastic SSOP Type II | -40°C to $+85^{\circ}\text{C}$ | 74ABT377A DB | 74ABT377A DB | SOT339-1 |
| 20-Pin Plastic TSSOP Type I | -40°C to $+85^{\circ}\text{C}$ | 74ABT377A PW | 74ABT377PWA DH | SOT360-1 |

PIN CONFIGURATION



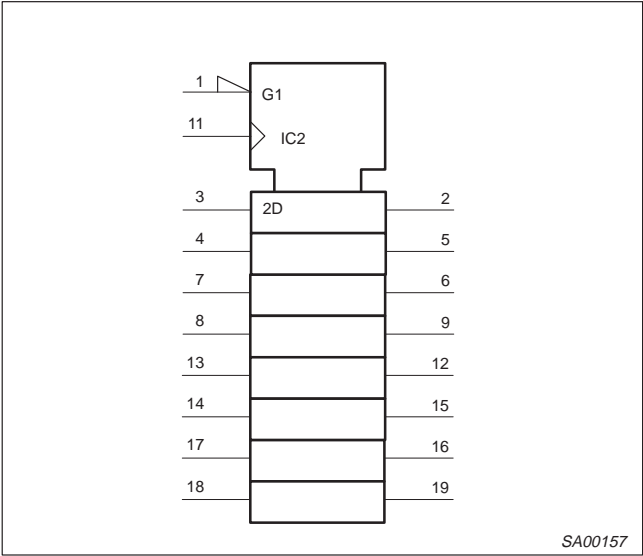
LOGIC SYMBOL



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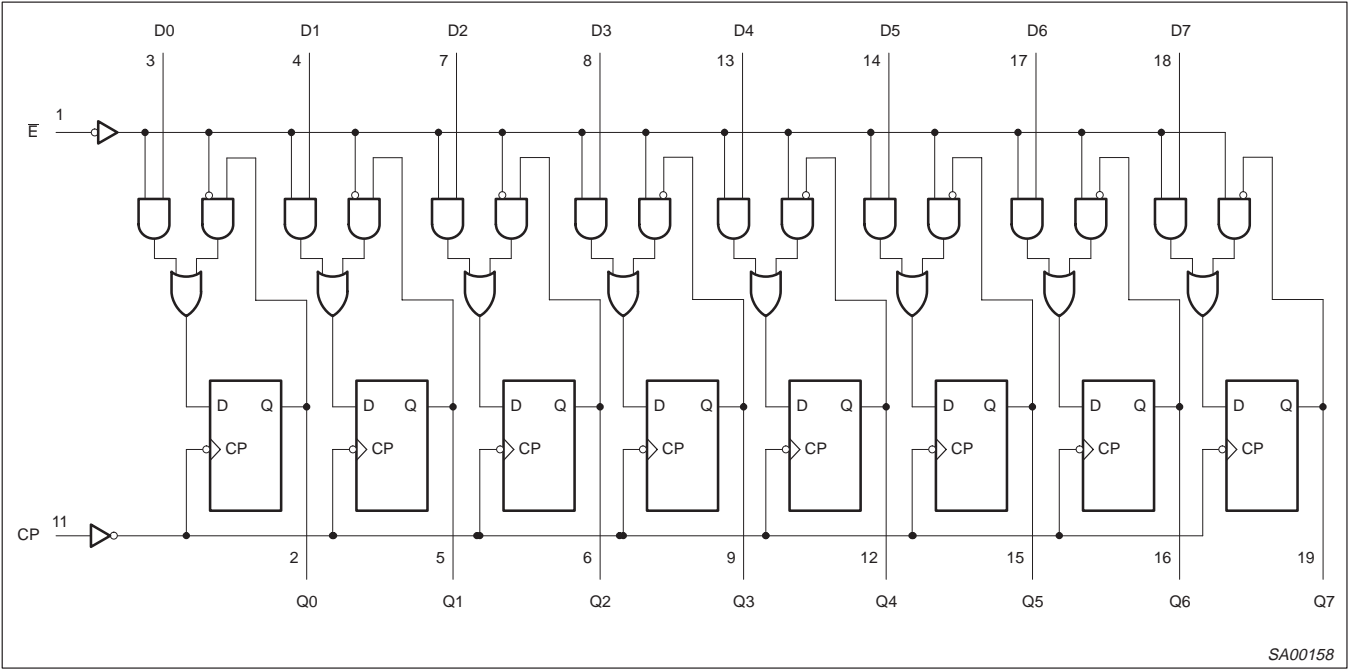
LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|----------------------------|-----------------|--|
| 1 | \bar{E} | Enable input (active-Low) |
| 3, 4, 7, 8, 13, 14, 17, 18 | D0-D7 | Data inputs |
| 2, 5, 6, 9, 12, 15, 16, 19 | Q0-Q7 | Data outputs |
| 11 | CP | Clock Pulse input (active rising edge) |
| 10 | GND | Ground (0V) |
| 20 | V _{CC} | Positive supply voltage |

LOGIC DIAGRAM



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FUNCTION TABLE

| INPUTS | | | OUTPUTS | OPERATING MODE |
|--------|--------|--------|------------------------|-------------------|
| E | CP | Dn | Qn | |
| l | ↑ | h | H | Load "1" |
| l | ↑ | l | L | Load "0" |
| h H | ↑ X | X X | no change no change | Hold (do nothing) |

H = High voltage level

h = High voltage level one set-up time prior to the Low-to-High clock transition

L = Low voltage level

l = Low voltage level one set-up time prior to the Low-to-High clock transition

X = Don't care

↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS^{1, 2}

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|------------------|--------------------------------|-----------------------------|--------------|------|
| V _{CC} | DC supply voltage | | −0.5 to +7.0 | V |
| I _{IK} | DC input diode current | V _I < 0 | −18 | mA |
| V _I | DC input voltage ³ | | −1.2 to +7.0 | V |
| I _{OK} | DC output diode current | V _O < 0 | −50 | mA |
| V _{OUT} | DC output voltage ³ | output in Off or High state | −0.5 to +5.5 | V |
| I _{OUT} | DC output current | output in Low state | 128 | mA |
| T _{stg} | Storage temperature range | | −65 to 150 | °C |

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|------------------|--------------------------------------|--------|-----------------|------|
| | | MIN | MAX | |
| V _{CC} | DC supply voltage | 4.5 | 5.5 | V |
| V _I | Input voltage | 0 | V _{CC} | V |
| V _{IH} | High-level input voltage | 2.0 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | V |
| I _{OH} | High-level output current | | −32 | mA |
| I _{OL} | Low-level output current | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | 0 | 5 | ns/V |
| T _{amb} | Operating free-air temperature range | −40 | +85 | °C |

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DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|------------------|--|--|--------------------------|-------|------|-----------------------------------|------|------|
| | | | T _{amb} = +25°C | | | T _{amb} = −40°C to +85°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| V _{IK} | Input clamp voltage | V _{CC} = 4.5V; I _{IK} = −18mA | | −0.9 | −1.2 | | −1.2 | V |
| V _{OH} | High-level output voltage | V _{CC} = 4.5V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH} | 2.5 | 2.9 | | 2.5 | | V |
| | | V _{CC} = 5.0V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH} | 3.0 | 3.4 | | 3.0 | | V |
| | | V _{CC} = 4.5V; I _{OH} = −32mA; V _I = V _{IL} or V _{IH} | 2.0 | 2.4 | | 2.0 | | V |
| V _{OL} | Low-level output voltage | V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH} | | 0.42 | 0.55 | | 0.55 | V |
| V _{RST} | Power-up output low voltage ³ | V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC} | | 0.13 | 0.55 | | 0.55 | V |
| I _I | Input leakage current | V _{CC} = 5.5V; V _I = GND or 5.5V | | ±0.01 | ±1.0 | | ±1.0 | μA |
| I _{OFF} | Power-off leakage current | V _{CC} = 0.0V; V _O or V _I ≤ 4.5V | | ±5.0 | ±100 | | ±100 | μA |
| I _{CEX} | Output High leakage current | V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC} | | 5.0 | 50 | | 50 | μA |
| I _O | Output current ¹ | V _{CC} = 5.5V; V _O = 2.5V | −50 | −100 | −180 | −50 | −180 | mA |
| I _{CCH} | Quiescent supply current | V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC} | | 0.5 | 250 | | 250 | μA |
| I _{CCL} | | V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC} | | 24 | 30 | | 30 | mA |
| ΔI _{CC} | Additional supply current per input pin ² | V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND | | 0.5 | 1.5 | | 1.5 | mA |

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

| SYMBOL | PARAMETER | WAVEFORM | LIMITS ¹ | | | | | UNIT |
|--------------------------------------|-------------------------------|----------|---|------------|------------|--|------------|------|
| | | | T _{amb} = +25°C V _{CC} = +5.0V | | | T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| f _{MAX} | Maximum clock frequency | 1 | 150 | 250 | | 150 | | MHz |
| t _{PLH} t _{PHL} | Propagation delay CP to Qn | 1 | 1.8 2.2 | 3.1 3.6 | 4.0 4.7 | 1.8 2.2 | 4.8 4.9 | ns |

NOTE:

- Limits may vary among suppliers.

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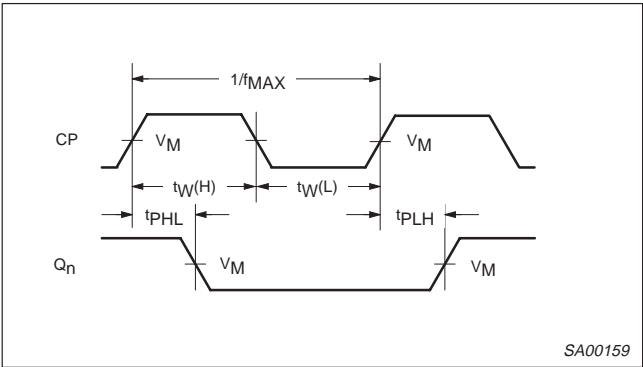
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

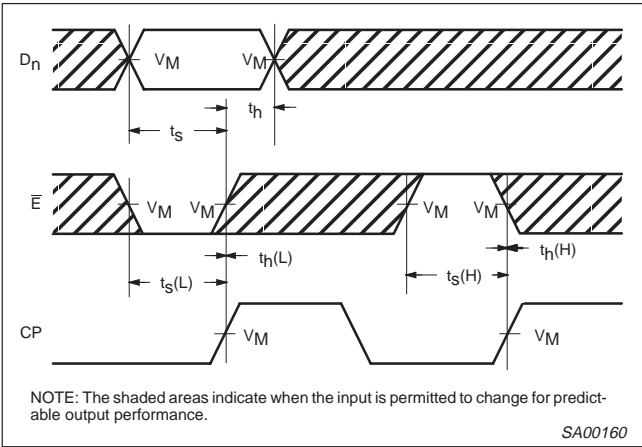
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | UNIT |
|--|---|----------|--|--------------|--|------|
| | | | $T_{\text{amb}} = +25^{\circ}\text{C}$ $V_{\text{CC}} = +5.0\text{V}$ | | $T_{\text{amb}} = -40 \text{ to } +85^{\circ}\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$ | |
| | | | MIN | TYP | MIN | |
| $t_{\text{s}}(\text{H})$ $t_{\text{s}}(\text{L})$ | Setup time, High or Low Dn to CP | 2 | 1.5 1.5 | 0.7 0.5 | 1.5 1.5 | ns |
| $t_{\text{h}}(\text{H})$ $t_{\text{h}}(\text{L})$ | Hold time, High or Low Dn to CP | 2 | 1.0 1.0 | -0.4 -0.6 | 1.0 1.0 | ns |
| $t_{\text{s}}(\text{H})$ $t_{\text{s}}(\text{L})$ | Setup time, High or Low $\bar{\text{E}}$ to CP | 2 | 2.0 2.0 | 1.1 1.0 | 2.0 2.0 | ns |
| $t_{\text{h}}(\text{H})$ $t_{\text{h}}(\text{L})$ | Hold time, High or Low $\bar{\text{E}}$ to CP | 2 | 1.0 1.0 | -0.9 -0.1 | 1.0 1.0 | ns |
| $t_{\text{w}}(\text{H})$ $t_{\text{w}}(\text{L})$ | Clock Pulse width High or Low | 1 | 1.5 2.0 | 0.7 1.0 | 1.5 2.0 | ns |

AC WAVEFORMS

$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency

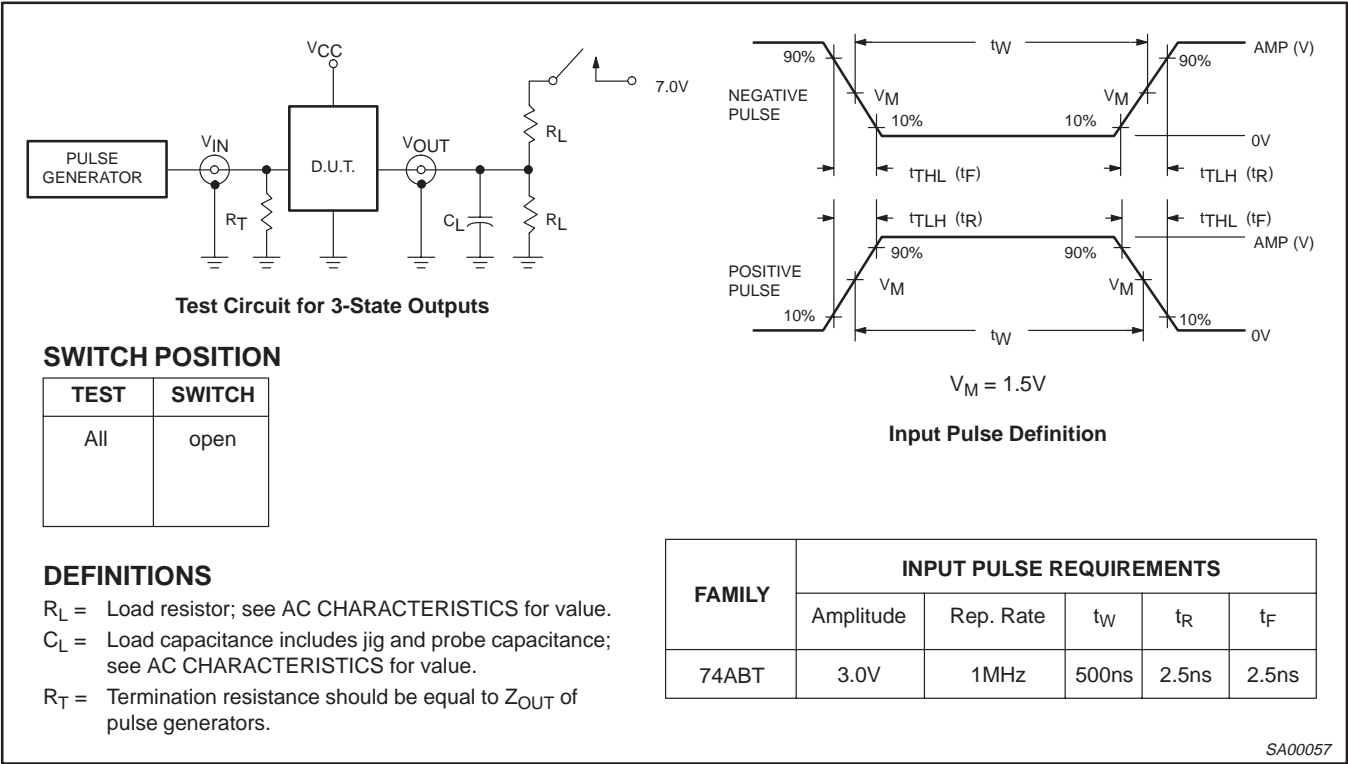


Waveform 2. Data and Enable Setup and Hold Times

Octal D-type flip-flop with enable

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TEST CIRCUIT AND WAVEFORM



Octal D-type flip-flop with enable

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| DEFINITIONS | | |
|---------------------------|------------------------|--|
| Data Sheet Identification | Product Status | Definition |
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Let's make things better.

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74ABT377**DIP20: plastic dual in-line package; 20 leads (300 mil)****SOT146-1**

Octal D-type flip-flop with enable

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SO20: plastic small outline package; 20 leads; body width 7.5 mm**SOT163-1**

Octal D-type flip-flop with enable

74ABT377

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

Octal D-type flip-flop with enable**74ABT377**

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm**SOT360-1**