74ABT623

Octal transceiver with dual enable; non-inverting; 3-state

Rev. 03 — 22 October 2009

Product data sheet

1. General description

The 74ABT623 high performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT623 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. This octal bus transceiver is designed for asynchronous two-way communication between data buses.

The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (pins OEAB and $\overline{\text{OEBA}}$). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of pins OEAB and $\overline{\text{OEBA}}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high-impedance OFF-state, both sets of the bus lines will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical.

2. Features

- Octal bidirectional bus interface
- 3-state buffers
- Power-up 3-state
- Output capability: +64 mA and –32 mA
- data inputs are disabled during 3-state mode
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT623D	–40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ABT623DB	–40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74ABT623PW	–40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

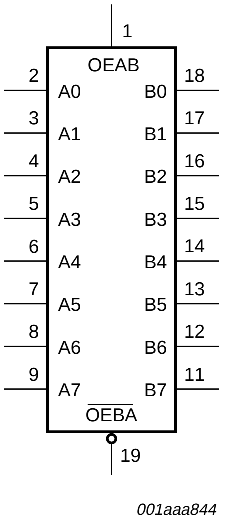


Fig 1. Logic symbol.

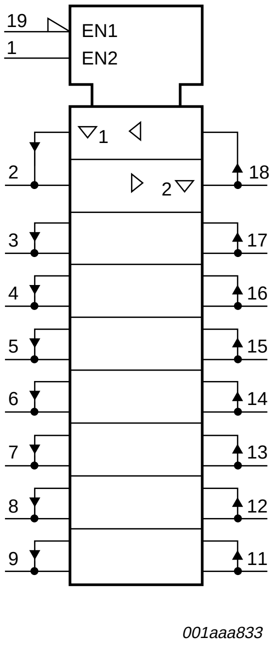


Fig 2. IEC logic symbol.

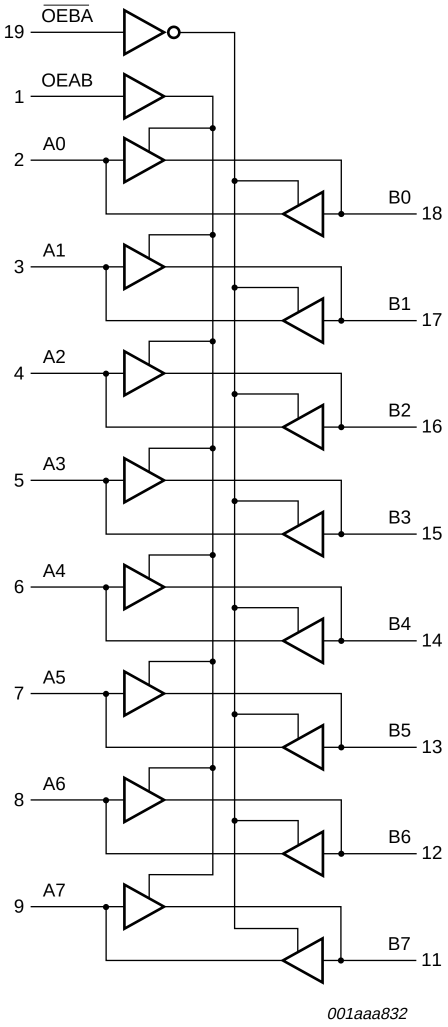


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning

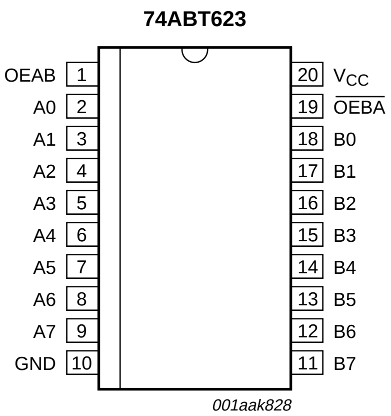


Fig 4. Pin configuration SO20

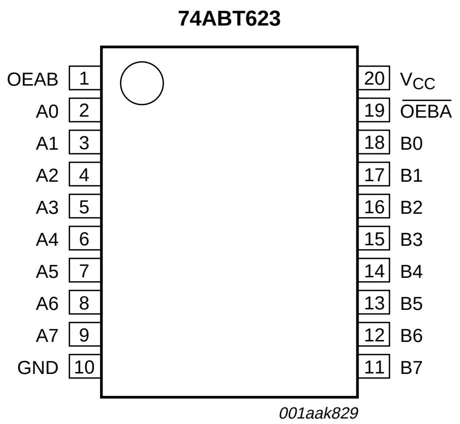


Fig 5. Pin configuration (T)SSOP20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
OEAB	1	output enable input (active HIGH)
A0 to A7	2, 3, 4, 5, 6, 7, 8, 9	data input or output
B0 to B7	18, 17, 16, 15, 14, 13, 12, 11	data input or output
GND	10	ground (0 V)
$\overline{OEBA}$	19	output enable input (active LOW)
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table[1]

Input		Input or output	
OEAB	**$\overline{OEBA}$**	**An**	**Bn**
L	L	An = Bn	input
H	H	input	Bn = An
L	H	Z	Z
H	L	An = Bn	input
H	L	input	Bn = An

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage		[1]	–1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	–0.5	+5.5	V
I_{IK}	input diode current	$V_I < 0$ V		–18	-	mA
I_{OK}	output diode current	$V_O < 0$ V		–50	-	mA
I_O	output current	output in LOW-state		-	128	mA
T_j	junction temperature		[2]	-	150	°C
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C	[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[3] For SO20 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For SSOP20 and TSSOP20 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		–32	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise or fall rate		0	-	10	ns/V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA	-	–0.9	–1.2	-	–1.2	V
V_{OH}	HIGH-level output voltage	V_I = V_{IL} or V_{IH}						
		V_{CC} = 4.5 V; I_{OH} = –3 mA	2.5	2.9	-	2.5	-	V
		V_{CC} = 5.0 V; I_{OH} = –3 mA	3.0	3.4	-	3.0	-	V
		V_{CC} = 4.5 V; I_{OH} = –32 mA	2.0	2.4	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}	-	0.42	0.55	-	0.55	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V						
		OEAB, $\overline{\text{OEBA}}$	-	±0.01	±1.0	-	±1.0	µA
		An, Bn	-	±5.0	±100	-	±100	µA
I_{OFF}	power-off leakage current	V_{CC} = 0.0 V; V_I or V_O ≤ 4.5 V	-	±5.0	±100	-	±100	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} = 2.0 V; V_O = 0.5 V; V_I = GND or V_{CC}; OEAB = GND; $\overline{\text{OEBA}}$ = V_{CC} [1]	-	±5.0	±50	-	±50	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}						
		V_O = 2.7 V	-	5.0	50	-	50	µA
		V_O = 0.5 V	-	–5.0	–50	-	–50	µA
I_{LO}	output leakage current	HIGH-state; V_O = 5.5 V; V_{CC} = 5.5 V; V_I = GND or V_{CC}	-	5.0	50	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V [2]	–180	–100	–50	–180	–50	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}						
		outputs HIGH-state	-	50	250	-	250	µA
		outputs LOW-state	-	24	30	-	30	mA
		outputs disabled	-	50	250	-	250	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input pin at 3.4 V, other inputs at V_{CC} or GND [3]						
		outputs enabled	-	0.5	1.5	-	1.5	mA
		outputs disabled	-	50	250	-	250	mA
		one enable input at 3.4 V and other inputs at V_{CC} or GND; outputs disabled	-	0.5	1.5	-	1.5	mA
C_I	input capacitance	V_I = 0 V or V_{CC}	-	4	-	-	-	pF
$C_{I/O}$	input/output capacitance	outputs disabled; V_O = 0 V or V_{CC}	-	7	-	-	-	pF

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 %, a transition time of up to 100 ms is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

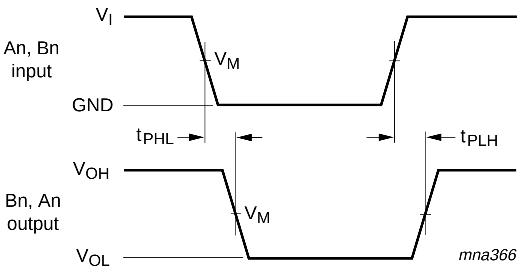
10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Figure 9.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			−40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	An to Bn or Bn to An; see Figure 6	1.0	2.6	4.1	1.0	4.6	ns
t_{PHL}	HIGH to LOW propagation delay	An to Bn or Bn to An; see Figure 6	1.0	2.7	4.2	1.0	4.6	ns
t_{PZH}	OFF-state to HIGH propagation delay	OEAB, $\overline{OEBA}$ to An or Bn; see Figure 7 and Figure 8	1.7	3.4	6.5	1.7	7.5	ns
t_{PZL}	OFF-state to LOW propagation delay	OEAB, $\overline{OEBA}$ to An or Bn; see Figure 7 and Figure 8	1.7	4.8	6.5	1.7	7.5	ns
t_{PHZ}	HIGH to OFF-state propagation delay	OEAB, $\overline{OEBA}$ to An or Bn; see Figure 7 and Figure 8	1.7	3.6	6.5	1.7	7.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	OEAB, $\overline{OEBA}$ to An or Bn; see Figure 7 and Figure 8	1.7	3.1	6.5	1.7	7.5	ns

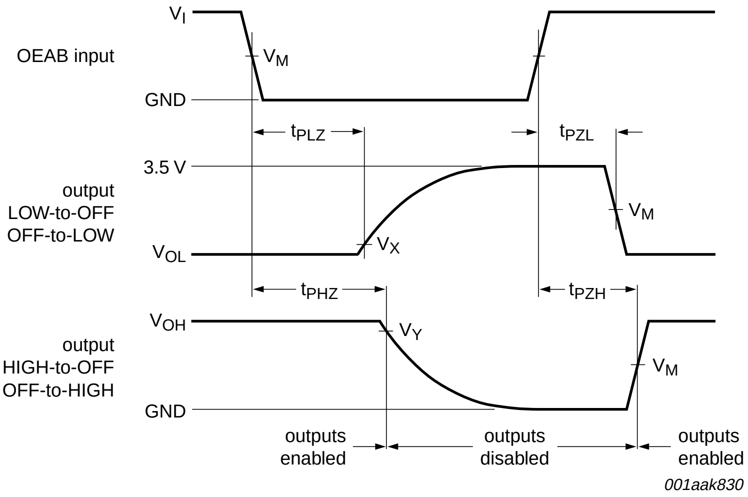
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

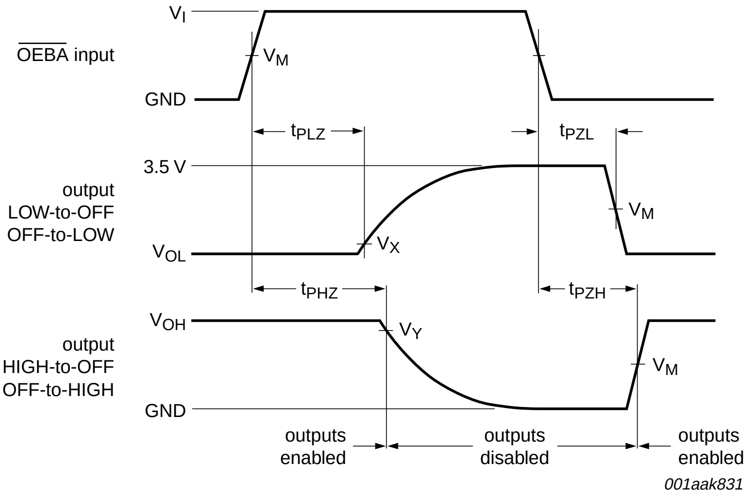
Fig 6. Propagation delay input (An, Bn) to output (Bn, An)



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Enable and disable times for OEAB input.



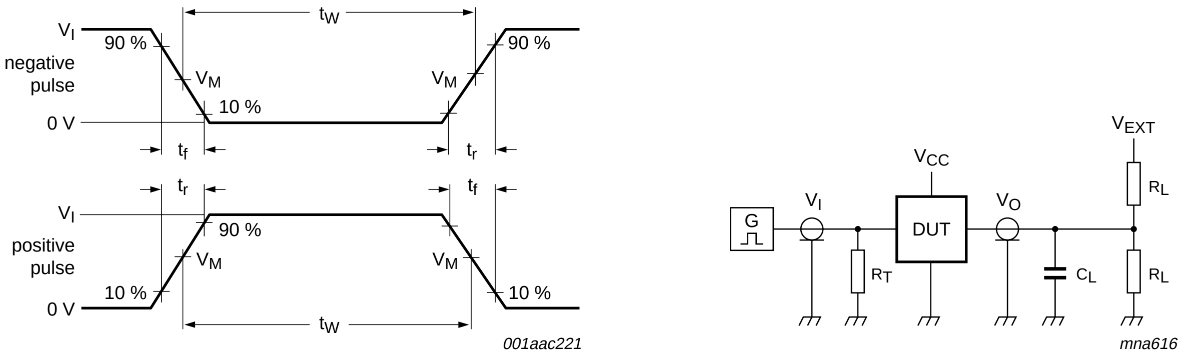
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Enable and disable times for $\overline{\text{OEBA}}$ input.

Table 8. Measurement points

Input		**Output**	
V_I	**V_M**	**V_X**	**V_Y**
3.0 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V



a. Input pulse definition

b. Test circuit

Test data and V_{EXT} levels are given in Table 9.

C_L = Load capacitance including jig and probe capacitance.

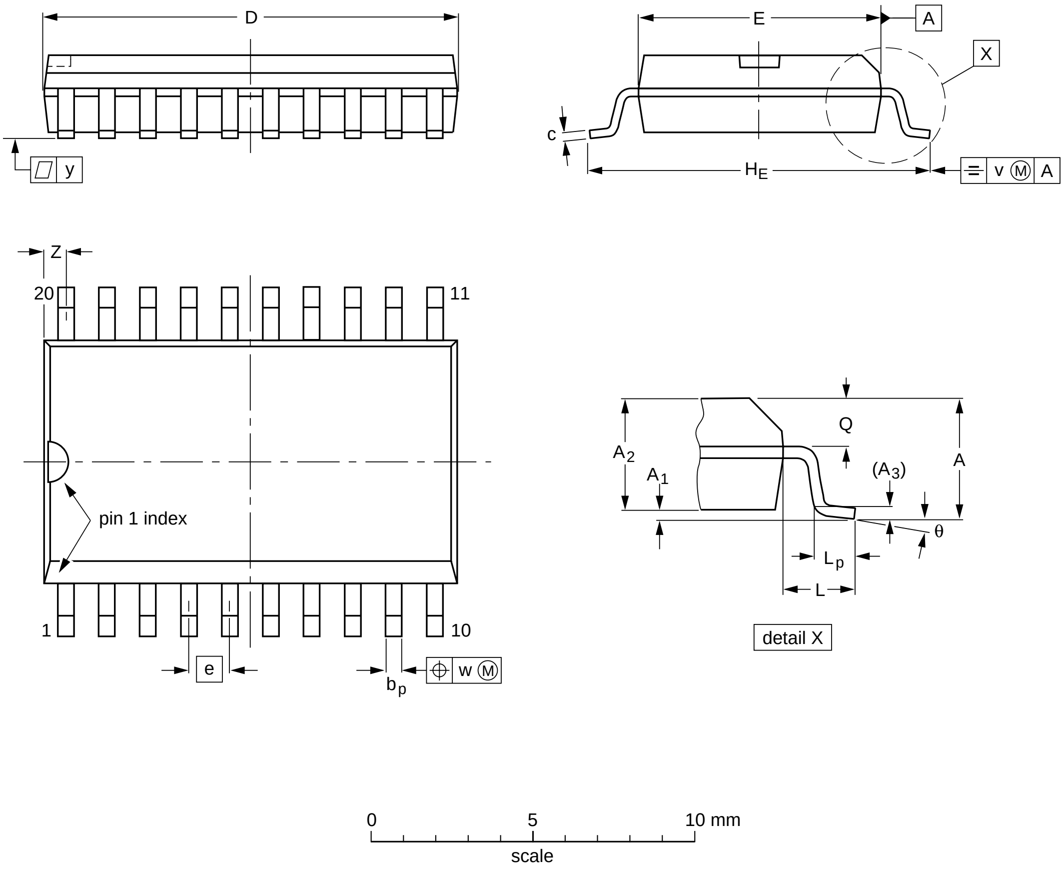
Fig 9. Test circuit for measuring switching times

Table 9. Test data

Input	Load		V_{EXT}		
t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

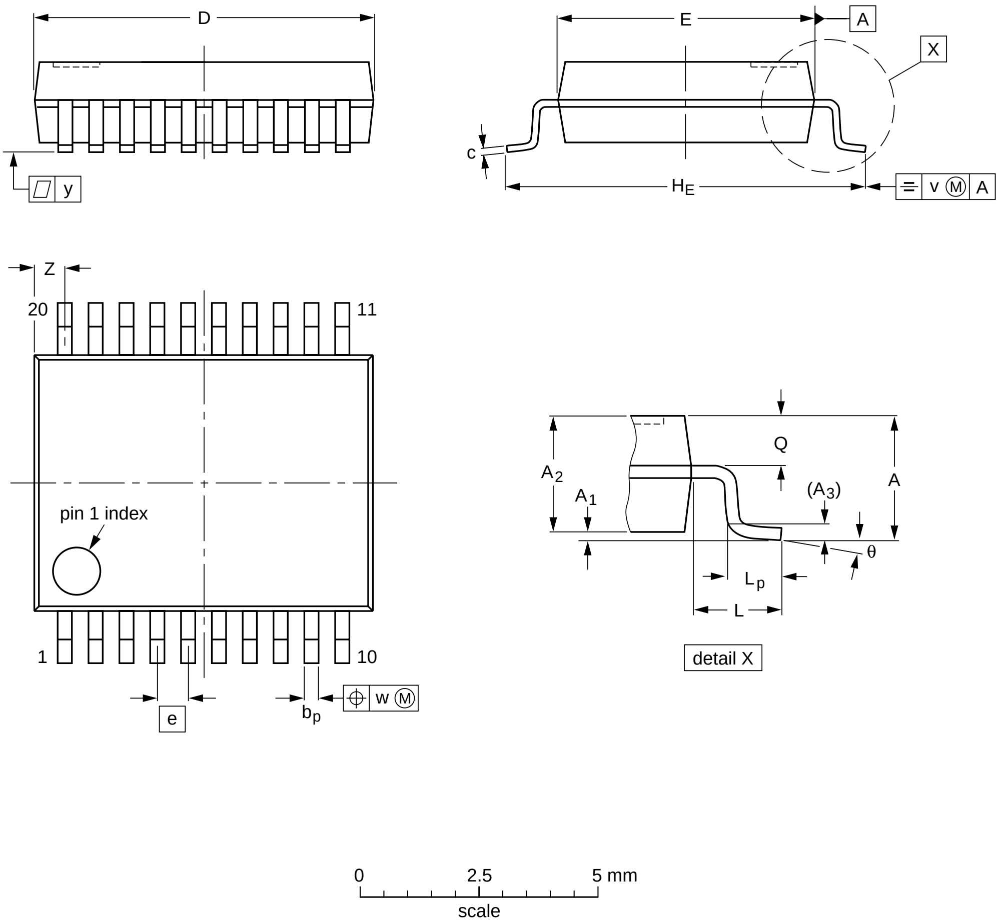
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT163-1.

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

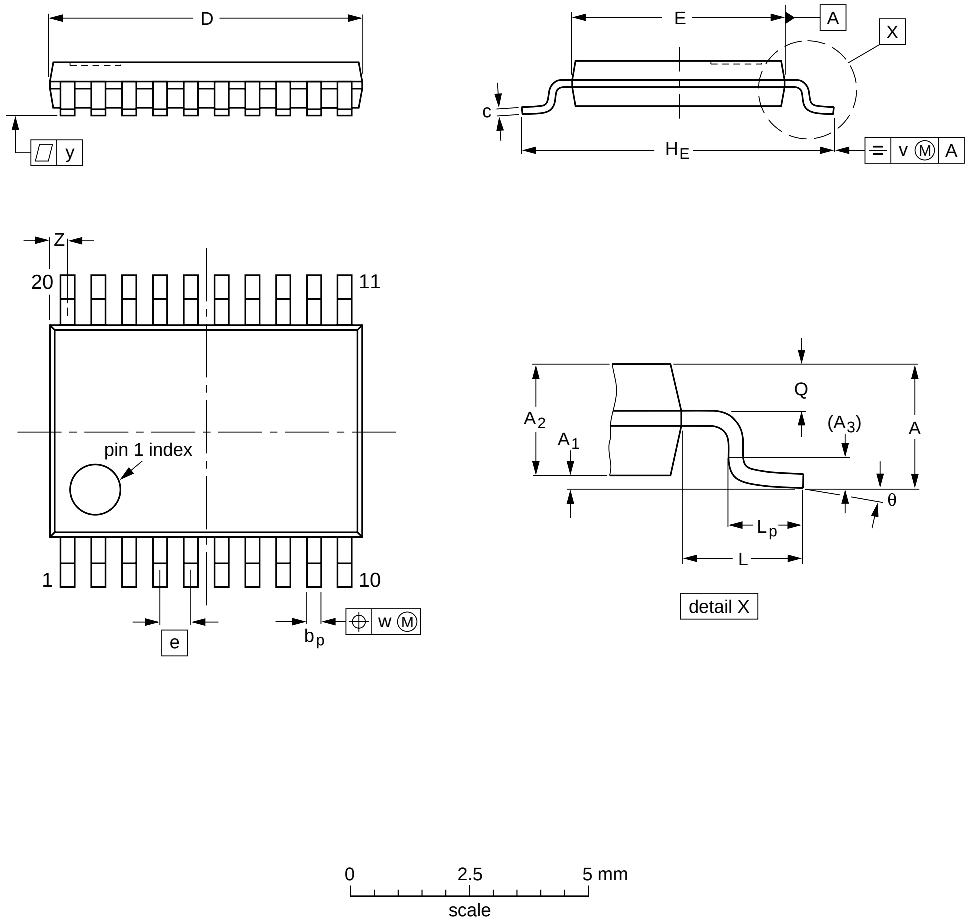
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT339-1.

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [1]	E [2]	e	H_E	L	L_p	Q	v	w	y	Z [1]	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT360-1.

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	BIpolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT623_3	20091022	Product data sheet	-	74ABT623_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • DIP20 package removed from Section 3 “Ordering information” and Section 12 “Package outline”.			
74ABT623_2	19980116	Product specification	-	74ABT623_1
74ABT623_1	19960925	-	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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