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January 2008

74AC273, 74ACT273
Octal D-Type Flip-Flop

Features

■ Ideal buffer for microprocessor or memory
■ Eight edge-triggered D-type flip-flops
■ Buffered common clock
■ Buffered, asynchronous master reset
■ See 377 for clock enable version
■ See 373 for transparent latch version
■ See 374 for 3-STATE version
■ Outputs source/sink 24mA
■ 74ACT273 has TTL-compatible inputs

General Description

The AC273 and ACT273 have eight edge-triggered D-type flip-flops with individual D-type inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D-type input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Ordering Information

Order Number	Package Number	Package Description
74AC273SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC273PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT273SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

$\overline{MR}$	1	20	V_{CC}
Q_0	2	19	Q_7
D_0	3	18	D_7
D_1	4	17	D_6
Q_1	5	16	Q_6
Q_2	6	15	Q_5
D_2	7	14	D_5
D_3	8	13	D_4
Q_3	9	12	Q_4
GND	10	11	CP
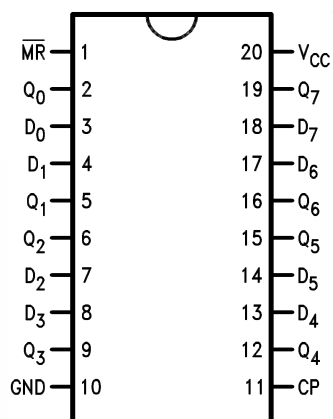
Pin Description

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

Logic Symbols

D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7

CP

MR

Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7

IEEE/IEC

$\overline{MR}$	R
CP	C1
D_0 1D	Q_0
D_1	Q_1
D_2	Q_2
D_3	Q_3
D_4	Q_4
D_5	Q_5
D_6	Q_6
D_7	Q_7
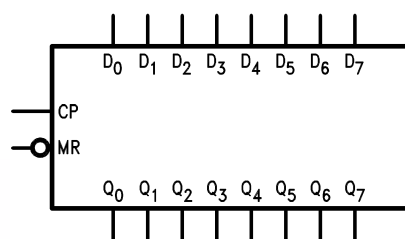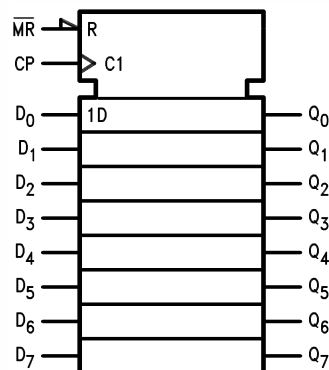
Mode Select-Function Table

	Inputs			Outputs
Operating Mode	$\overline{MR}$	**CP**	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	H	H
Load '0'	H	⌐	L	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

⌐ = LOW-to-HIGH Transition

Logic Diagram
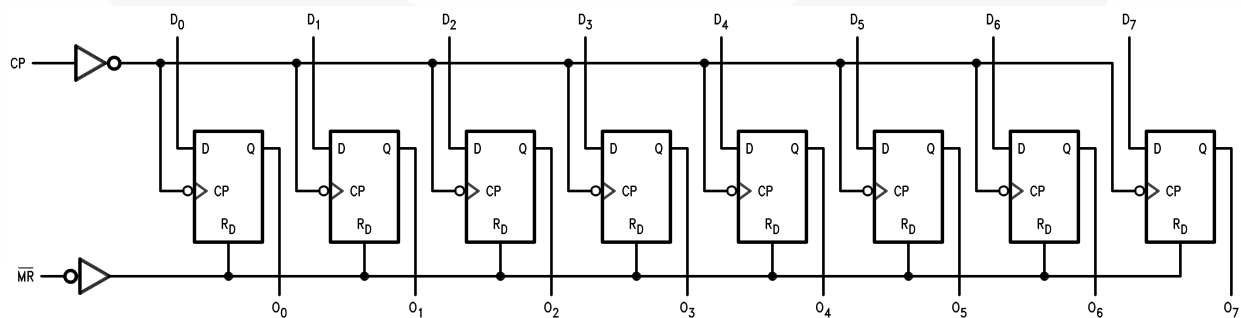
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current	
	$V_I = -0.5V$	–20mA
	$V_I = V_{CC} + 0.5$	+20mA
V_I	DC Input Voltage	–0.5V to V_{CC} + 0.5V
I_{OK}	DC Output Diode Current	
	$V_O = -0.5V$	–20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	
	AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC}, V_{CC} @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics for AC

Symbol	Parameter	V_CC (V)	Conditions	T_A = +25°C Typ.	Guaranteed Limits	T_A = −40°C to +85°C Guaranteed Limits	Units
V_{IH}	Minimum HIGH Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} − 0.1V	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V_{IL}	Maximum LOW Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} − 0.1V	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V_{OH}	Minimum HIGH Level Output Voltage	3.0	I_{OUT} = −50µA	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −12mA		2.56	2.46	
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −24mA		3.86	3.76	
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −24mA[1]		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	3.0	I_{OUT} = 50µA	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 12mA		0.36	0.44	
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA		0.36	0.44	
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]		0.36	0.44	
I_{IN}[2]	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND		±0.1	±1.0	µA
I_{OLD}	Minimum Dynamic Output Current[3]	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85V Min.			−75	mA
I_{CC}[2]	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND		4.0	40.0	µA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.

2. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

3. Maximum test duration 2.0ms, one output loaded at a time.

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C		T_A = −40°C to +85°C	Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} − 0.1V	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} − 0.1V	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	I_{OUT} = −50µA	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} = −24mA		3.86	3.76	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} = −24mA[4]		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	I_{OUT} = 50µA	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} = 24mA		0.36	0.44	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} = 24mA[4]		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	µA
I_{CCT}	Maximum I_{CC}/Input	5.5	$V_I = V_{CC}$ − 2.1V	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current[5]	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85V Min.			−75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	µA

Notes:

4. All outputs loaded; thresholds on input associated with output under test.

5. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)[6]	T_A = +25°C, C_L = 50pF			T_A = −40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	3.3	90	125		75		MHz
		5.0	140	175		125		
t_{PLH}	Propagation Delay, Clock to Output	3.3	4.0	7.0	12.5	3.0	14.0	ns
		5.0	3.0	5.5	9.0	2.5	10.0	
t_{PHL}	Propagation Delay, Clock to Output	3.3	4.0	7.0	13.0	3.5	14.5	ns
		5.0	3.0	5.0	10.0	2.5	11.0	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Output	3.3	4.0	7.0	13.0	3.5	14.0	ns
		5.0	3.0	5.0	10.0	2.5	10.5	

Note:

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements for AC

Symbol	Parameter	V_{CC} (V)[7]	T_A = +25°C, C_L = 50pF	T_A = −40°C to +85°C, C_L = 50pF		Units
			Typ.	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW, Data to CP	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	
t_H	Hold Time, HIGH or LOW, Data to CP	3.3	−2.0	0	0	ns
		5.0	−1.0	1.0	1.0	
t_W	Clock Pulse Width, HIGH or LOW	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	
t_W	$\overline{MR}$ Pulse Width, HIGH or LOW	3.3	2.0	5.5	6.0	ns
		5.0	1.5	4.0	4.5	
t_{rec}	Recovery Time, $\overline{MR}$ to CP	3.3	1.5	3.5	4.5	ns
		5.0	1.0	2.0	3.0	

Note:

7. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)[8]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	2.0	125	189		110		MHz
t_{PLH}, t_{PHL}	Propagation Delay, CP to Q_n	5.0	1.5	6.5	8.5	1.5	9.0	ns
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n	5.0	1.5	7.0	9.0	1.5	8.5	ns

Note:

8. Voltage range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements for ACT

Symbol	Parameter	V_{CC} (V)[9]	T_A = +25°C, C_L = 50pF		T_A = –40°C to +85°C, C_L = 50pF	Units
			Typ.	Guaranteed Minimum	Guaranteed Minimum	
t_S	Setup Time, HIGH or LOW, D_n to CP	5.0	1.0	3.5	3.5	ns
t_H	Hold Time, HIGH or LOW, D_n to CP	5.0	–0.5	1.5	1.5	ns
t_W	Clock Pulse Width, HIGH or LOW	5.0	2.0	4.0	4.0	ns
t_W	$\overline{MR}$ Pulse Width, HIGH or LOW	5.0	1.5	4.0	4.0	ns
t_W	Recovery Time, $\overline{MR}$ to CP	5.0	0.5	3.0	3.0	ns

Note:

9. Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance for AC	V_{CC} = 5.0V	50.0	pF
	Power Dissipation Capacitance for ACT		40.0	

Physical Dimensions

13.00
12.60

A

11.43

20

11

B

10.65
10.00

7.60
7.40

9.50

2.25

PIN ONE
INDICATOR

1

10

0.51
0.35

1.27

⊕ | 0.25 Ⓜ | C | B | A

1.27

0.65

LAND PATTERN RECOMMENDATION

2.65 MAX

C

⌒ | 0.10 | C

0.30
0.10

SEE DETAIL A

0.33
0.20

SEATING PLANE

0.75
0.25

X 45°

(R0.10)

GAGE PLANE

(R0.10)

0.25

8°
0°

1.27
0.40

SEATING PLANE

(1.40)

DETAIL A
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC
   MS-013, VARIATION AC, ISSUE E
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD
   FLASH OR BURRS.
D) CONFORMS TO ASME Y14.5M-1994
E) LANDPATTERN STANDARD: SOIC127P1030X265-20L
F) DRAWING FILENAME: MKT-M20BREV3

Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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Physical Dimensions (Continued)

12.6±0.10
−A−

0.40 TYP

20   11

7.8

5.3±0.10
−B−

3.9

PIN #1 IDENT.

1   10

△ 0.2 C B A
ALL LEAD TIPS

20   19   12   11

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2   9   10

1.27 TYP   0.6 TYP

LAND PATTERN RECOMMENDATION

ALL LEAD TIPS
△ 0.1 C

2.1 MAX.

1.8±0.1

−C−

0.15±0.05

1.27 TYP

0.35−0.51

⊕ 0.12Ⓜ C A

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.15−0.25
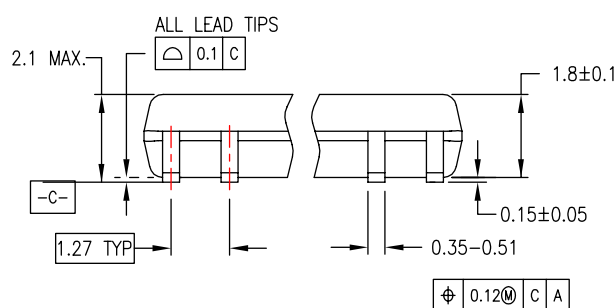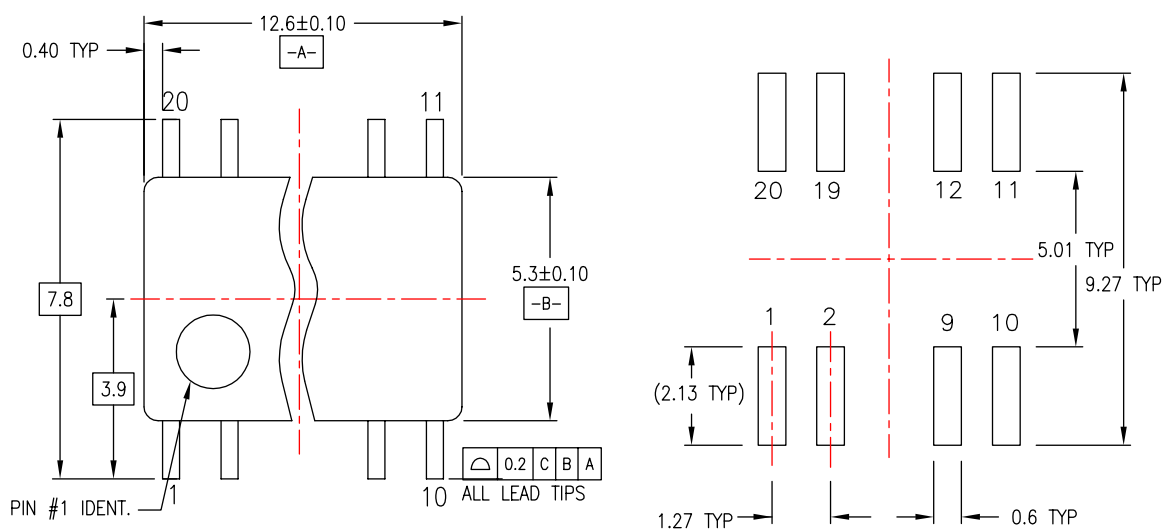
NOTES:
A. CONFORMS TO EIAJ EDR−7320 REGISTRATION,
   ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
   FLASH, AND TIE BAR EXTRUSIONS.

7° TYP

GAGE PLANE

0.25

0°−8° TYP

0.60±0.15

1.25

SEATING PLANE
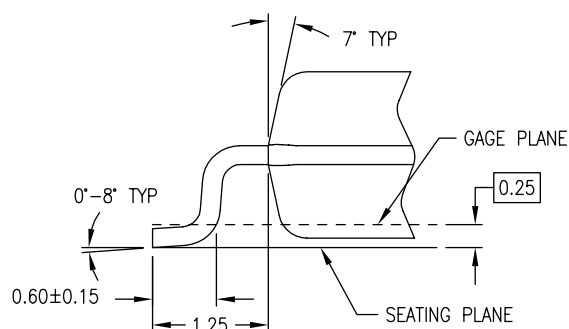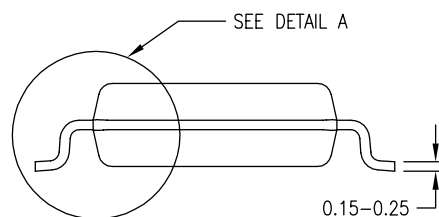
DETAIL A

M20DREVC

Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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
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Physical Dimensions (Continued)

6.5±0.1
-A-

0.20

20   11

-C-

4.4±0.1 -B-

6.4

3.2

1   10

△ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

LAND PATTERN RECOMMENDATION

4.16   7.72

1.78

0.65   0.42

△ 0.1 C
ALL LEAD TIPS

0.90 +0.15 -0.10

1.2 max

-C-

0.1±0.05

0.65

0.19-0.30
⊕ 0.10Ⓜ A BⓈ CⓈ

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.09-0.20

12.00°

R0.09min

GAGE PLANE

0 - 8°

0.25

SEATING PLANE

0.6±0.1

R0.09min

1.00

DETAIL A
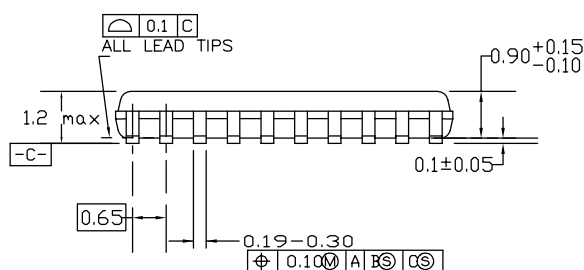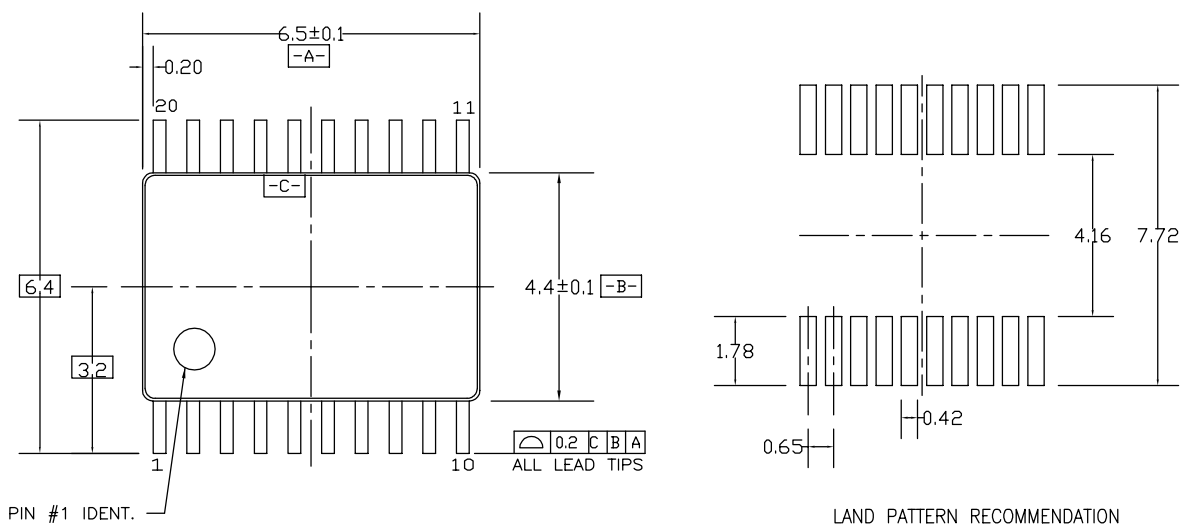
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC,
   REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH,
   AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
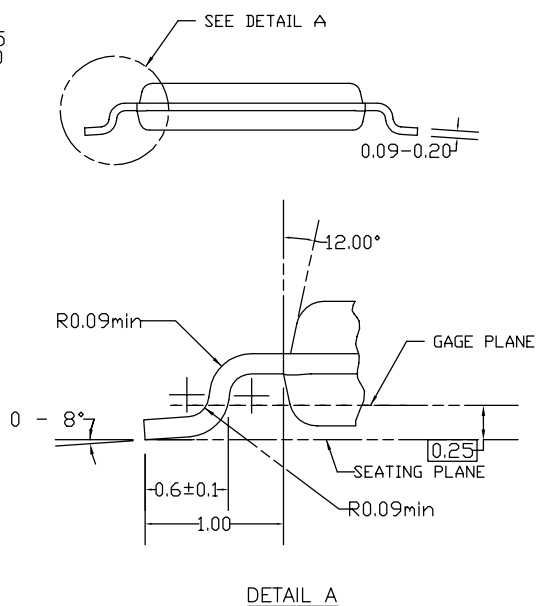
MTC20REVD1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions (Continued)

26.92
24.89
ⒸC

20   11

PIN #1

7.11
6.09
ⒸC

1   10

Ⓐ A   Ⓑ B

ⒹD

(0.97)   1.78
             1.14   7° TYP

3.43
3.17
5.33 MAX

7° TYP

7.87

Ⓒ C

2.54   0.36
              0.56

3.55
3.17
0.38 MIN   10.92 MAX   7.62

0.20
0.35

⊕ .001[.025] Ⓜ C

NOTES:
  A. CONFORMS TO JEDEC REGISTRATION MS-001,
     VARIATIONS AD.
  B. ALL DIMENSIONS ARE IN MILLIMETERS
  Ⓒ. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
     MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED
     0.25MM.
  Ⓓ. DOES NOT INCLUDE DAMBAR PROTRUSIONS.
     DAMBAR PROTRUSIONS SHALL NOT EXCEED
     0.25MM.
  E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  F. DRAWING FILE NAME: N20AREV8

Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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FACT Quiet Series™
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FAST®
FastvCore™
FlashWriter® *

FPS™
FRFET®
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Green FPS™ e-Series™
GTO™
i-Lo™
IntelliMAX™
ISOPLANAR™
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MICROCOUPLER™
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SuperFET™
SuperSOT™-3
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SuperSOT™-8

SyncFET™
SYSTEM GENERAL®
The Power Franchise®
the power franchise®
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