

#### Is Now Part of



## ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at <a href="https://www.onsemi.com">www.onsemi.com</a>

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any EDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officer



January 2008

# 74AC373, 74ACT373 Octal Transparent Latch with 3-STATE Outputs

#### **Features**

- I<sub>CC</sub> and I<sub>OZ</sub> reduced by 50%
- Eight latches in a single package
- 3-STATE outputs for bus interfacing
- Outputs source/sink 24mA
- ACT373 has TTL-compatible inputs

#### **General Description**

The AC/ACT373 consists of eight latches with 3-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable  $(\overline{OE})$  is LOW. When  $\overline{OE}$  is HIGH, the bus output is in the high impedance state.

## **Ordering Information**

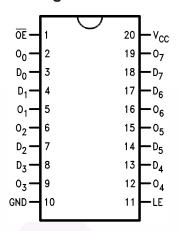
Order Number	Package Number	Package Description
74AC373SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC373PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT373SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT373MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ACT373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT373PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



All packages are lead free per JEDEC: J-STD-020B standard.

#### **Connection Diagram**



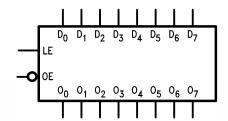
#### **Pin Description**

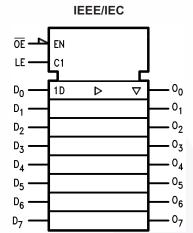
Pin Names	Description
D <sub>0</sub> –D <sub>7</sub>	Data Inputs
LE	Latch Enable Input
OE	Output Enable Input
O <sub>0</sub> -O <sub>7</sub>	3-STATE Latch Outputs

#### **Functional Description**

The AC/ACT373 contains eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D-type input changes. When LE is LOW, the latches store the information that was present on the D-type inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable  $(\overline{OE})$  input. When  $\overline{OE}$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

#### **Logic Symbols**





#### **Truth Table**

	Inputs				
LE	ŌĒ	D <sub>n</sub>	O <sub>n</sub>		
X	Н	Х	Z		
Н	L	L	L		
Н	L	Н	Н		
L	L	Х	O <sub>0</sub>		

H = HIGH Voltage Level

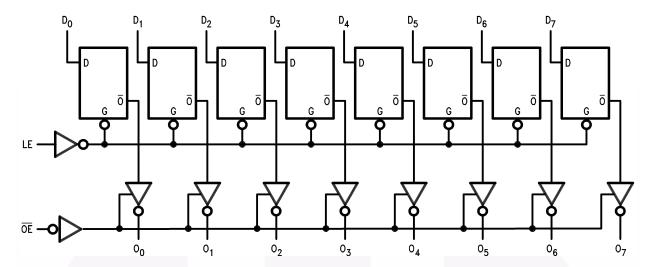
L = LOW Voltage Level

Z = High Impedance

X = Immaterial

 ${\rm O_0} = {\rm Previous} \; {\rm O_0} \; {\rm before} \; {\rm HIGH\text{-}to\text{-}LOW} \; {\rm transition} \; {\rm of} \; {\rm Latch} \; {\rm Enable} \;$ 

## **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V <sub>CC</sub>	Supply Voltage	-0.5V to +7.0V
I <sub>IK</sub>	DC Input Diode Current	
	$V_{I} = -0.5V$	-20mA
	$V_{I} = V_{CC} + 0.5$	+20mA
V <sub>I</sub>	DC Input Voltage	-0.5V to V <sub>CC</sub> + 0.5V
I <sub>OK</sub>	DC Output Diode Current	
	$V_{O} = -0.5V$	-20mA
	$V_{O} = V_{CC} + 0.5V$	+20mA
V <sub>O</sub>	DC Output Voltage	$-0.5V$ to $V_{CC} + 0.5V$
Io	DC Output Source or Sink Current	±50mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current per Output Pin	±50mA
T <sub>STG</sub>	Storage Temperature	–65°C to +150°C
$T_J$	Junction Temperature	140°C

#### **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V <sub>CC</sub>	Supply Voltage	
	AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
V <sub>I</sub>	Input Voltage	0V to V <sub>CC</sub>
V <sub>O</sub>	Output Voltage	0V to V <sub>CC</sub>
T <sub>A</sub>	Operating Temperature	-40°C to +85°C
ΔV / Δt	Minimum Input Edge Rate, AC Devices:	125mV/ns
	$V_{\text{IN}}$ from 30% to 70% of $V_{\text{CC}}$ , $V_{\text{CC}}$ @ 3.3V, 4.5V, 5.5V	
ΔV / Δt	Minimum Input Edge Rate, ACT Devices:	125mV/ns
	$V_{\rm IN}$ from 0.8V to 2.0V, $V_{\rm CC}$ @ 4.5V, 5.5V	

#### **DC Electrical Characteristics for AC**

				<b>T</b> <sub>A</sub> = -	+25°C	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	
Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	Тур.	G	uaranteed Limits	Units
V <sub>IH</sub>	Minimum HIGH Level	3.0	$V_{OUT} = 0.1V$ or	1.5	2.1	2.1	V
	Input Voltage	4.5	V <sub>CC</sub> – 0.1V	2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V <sub>IL</sub>	Maximum LOW Level	3.0	$V_{OUT} = 0.1V$ or	1.5	0.9	0.9	V
	Input Voltage	4.5	V <sub>CC</sub> – 0.1V	2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V <sub>OH</sub>	Minimum HIGH Level	3.0	$I_{OUT} = -50\mu A$	2.99	2.9	2.9	V
	Output Voltage	4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -12\text{mA}$		2.56	2.46	
		4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24\text{mA}$		3.86	3.76	
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24\text{mA}^{(1)}$		4.86	4.76	
V <sub>OL</sub>	Maximum LOW Level	3.0	$I_{OUT} = 50\mu A$	0.002	0.1	0.1	V
	Output Voltage	4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 12\text{mA}$		0.36	0.44	
		4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24\text{mA}$		0.36	0.44	
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24\text{mA}^{(1)}$		0.36	0.44	
I <sub>IN</sub> <sup>(2)</sup>	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$ , GND		±0.1	±1.0	μA
l <sub>OZ</sub>	Maximum 3-STATE Leakage Current	5.5	$\begin{aligned} &V_{I}\left(OE\right)=V_{IL},V_{IH};\\ &V_{I}=V_{CC},GND;\\ &V_{O}=V_{CC},GND \end{aligned}$		±0.25	±2.5	μA
I <sub>OLD</sub>	Minimum Dynamic	5.5	V <sub>OLD</sub> = 1.65V Max.			75	mA
I <sub>OHD</sub>	Output Current <sup>(3)</sup>	5.5	V <sub>OHD</sub> = 3.85V Min.			<b>-75</b>	mA
I <sub>CC</sub> <sup>(2)</sup>	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA

#### Notes:

- 1. All outputs loaded; thresholds on input associated with output under test.
- 2.  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .
- 3. Maximum test duration 2.0ms, one output loaded at a time.

### **DC Electrical Characteristics for ACT**

				<b>T</b> <sub>A</sub> = -	+25°C	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	
Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	Тур.	G	uaranteed Limits	Units
V <sub>IH</sub>	Minimum HIGH Level	4.5	$V_{OUT} = 0.1V$ or	1.5	2.0	2.0	V
	Input Voltage	5.5	V <sub>CC</sub> – 0.1V	1.5	2.0	2.0	
V <sub>IL</sub>	Maximum LOW	4.5	$V_{OUT} = 0.1V$ or	1.5	0.8	0.8	V
	Level Input Voltage	5.5	V <sub>CC</sub> – 0.1V	1.5	0.8	0.8	
V <sub>OH</sub>	Minimum HIGH Level	4.5	$I_{OUT} = -50\mu A$	4.49	4.4	4.4	V
	Output Voltage	5.5		5.49	5.4	5.4	
		4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24\text{mA}$		3.86	3.76	
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24\text{mA}^{(4)}$		4.86	4.76	
V <sub>OL</sub>	Maximum LOW	4.5	$I_{OUT} = 50\mu A$	0.001	0.1	0.1	V
	Level Output Voltage	5.5		0.001	0.1	0.1	
		4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24\text{mA}$		0.36	0.44	
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24\text{mA}^{(4)}$		0.36	0.44	
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$ , GND		±0.1	±1.0	μA
I <sub>OZ</sub>	Maximum 3-STATE Leakage Current	5.5	$V_I = V_{IL}, V_{IH};$ $V_O = V_{CC}, GND$		±0.25	±2.5	μA
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	$V_I = V_{CC} - 2.1V$	0.6		1.5	mA
I <sub>OLD</sub>	Minimum Dynamic	5.5	OLD			75	mA
I <sub>OHD</sub>	Output Current <sup>(5)</sup>	5.5				-75	mA
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA

#### Notes:

- 4. All outputs loaded; thresholds on input associated with output under test.
- 5. Maximum test duration 2.0ms, one output loaded at a time.

### **AC Electrical Characteristics for AC**

				$T_A = +25^{\circ}C$ , $C_L = 50pF$		$T_A = -40$ °C to +85°C, $C_L = 50$ pF		
Symbol	Parameter	$V_{CC}(V)^{(6)}$	Min.	Тур.	Max.	Min.	Max.	Units
t <sub>PLH</sub>	Propagation Delay, D <sub>n</sub> to O <sub>n</sub>	3.3	1.5	10.0	13.5	1.5	15.0	ns
		5.0	1.5	7.0	9.5	1.5	10.5	
t <sub>PHL</sub>	Propagation Delay, D <sub>n</sub> to O <sub>n</sub>	3.3	1.5	9.5	13.0	1.5	14.5	ns
		5.0	1.5	7.0	9.5	1.5	10.5	
t <sub>PLH</sub>	Propagation Delay, LE to O <sub>n</sub>	3.3	1.5	10.0	13.5	1.5	15.0	ns
		5.0	1.5	7.5	9.5	1.5	10.5	
t <sub>PHL</sub>	Propagation Delay, LE to O <sub>n</sub>	3.3	1.5	9.5	12.5	1.5	14.0	ns
		5.0	1.5	7.0	9.5	1.5	10.5	
t <sub>PZH</sub>	Output Enable Time	3.3	1.5	9.0	11.5	1.0	13.0	ns
		5.0	1.5	7.0	8.5	1.0	9.5	
t <sub>PZL</sub>	Output Enable Time	3.3	1.5	8.5	11.5	1.0	13.0	ns
		5.0	1.5	6.5	8.5	1.0	9.5	
t <sub>PHZ</sub>	Output Disable Time	3.3	1.5	10.0	12.5	1.0	14.5	ns
		5.0	1.5	8.0	11.0	1.0	12.5	
t <sub>PLZ</sub>	Output Disable Time	3.3	1.5	8.0	11.5	1.0	12.5	ns
		5.0	1.5	6.5	8.5	1.0	10.0	

#### Note:

6. Voltage range 3.3 is  $3.3V \pm 0.3V$ . Voltage range 5.0 is  $5.0V \pm 0.5V$ .

## AC Operating Requirements for AC

			T <sub>A</sub> = + C <sub>L</sub> =	⊦25°C, 50pF	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C},$ $C_L = 50\text{pF}$	
Symbol	Parameter	$V_{CC}(V)^{(7)}$	Тур	Gua	ranteed Minimum	Units
t <sub>S</sub>	Setup Time, HIGH or LOW, D <sub>n</sub> to LE	3.3	3.5	5.5	6.0	ns
		5.0	2.0	4.0	4.5	
t <sub>H</sub>	Hold Time, HIGH or LOW, D <sub>n</sub> to LE	3.3	-3.0	1.0	1.0	ns
		5.0	-1.5	1.0	1.0	
t <sub>W</sub>	LE Pulse Width, HIGH	3.3	4.0	5.5	6.0	ns
		5.0	2.0	4.0	4.5	

#### Note:

7. Voltage range 3.3 is 3.3V  $\pm$  0.3V. Voltage range 5.0 is 5.0V  $\pm$  0.5V.

### **AC Electrical Characteristics for ACT**

			T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF		$T_A = -40$ °C to +85°C, $C_L = 50$ pF			
Symbol	Parameter	V <sub>CC</sub> (V) <sup>(8)</sup>	Min.	Тур.	Max.	Min.	Max.	Units
t <sub>PLH</sub>	Propagation Delay, D <sub>n</sub> to O <sub>n</sub>	5.0	2.5	8.5	10.0	1.5	11.5	ns
t <sub>PHL</sub>	Propagation Delay, D <sub>n</sub> to O <sub>n</sub>	5.0	2.0	8.0	10.0	1.5	11.5	ns
t <sub>PLH</sub>	Propagation Delay, LE to O <sub>n</sub>	5.0	2.5	8.5	11.0	2.0	11.5	ns
t <sub>PHL</sub>	Propagation Delay, LE to O <sub>n</sub>	5.0	2.0	8.0	10.0	1.5	11.5	ns
t <sub>PZH</sub>	Output Enable Time	5.0	2.0	8.0	9.5	1.5	10.5	ns
t <sub>PZL</sub>	Output Enable Time	5.0	2.0	7.5	9.0	1.5	10.5	ns
t <sub>PHZ</sub>	Output Disable Time	5.0	2.5	9.0	11.0	2.5	12.5	ns
t <sub>PLZ</sub>	Output Disable Time	5.0	1.5	7.5	8.5	1.0	10.0	ns

#### Note:

8. Voltage range 5.0 is  $5.0V \pm 0.5V$ .

## **AC Operating Requirements for ACT**

			T <sub>A</sub> = +	-25°C, 50pF	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C},$ $C_L = 50\text{pF}$	
Symbol	Parameter	$V_{CC}(V)^{(9)}$	Тур	Gua	aranteed Minimum	Units
t <sub>S</sub>	Setup Time, HIGH or LOW, D <sub>n</sub> to LE	5.0	0.8	2.5	3.5	ns
t <sub>H</sub>	Hold Time, HIGH or LOW, D <sub>n</sub> to LE	5.0	0	0	1.0	ns
t <sub>W</sub>	LE Pulse Width, HIGH	5.0	2.0	7.0	8.0	ns

#### Note:

9. Voltage range 5.0 is  $5.0V \pm 0.5V$ .

## Capacitance

Symbol	Parameter	Conditions	Тур.	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = OPEN	4.5	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 5.0V	40.0	pF

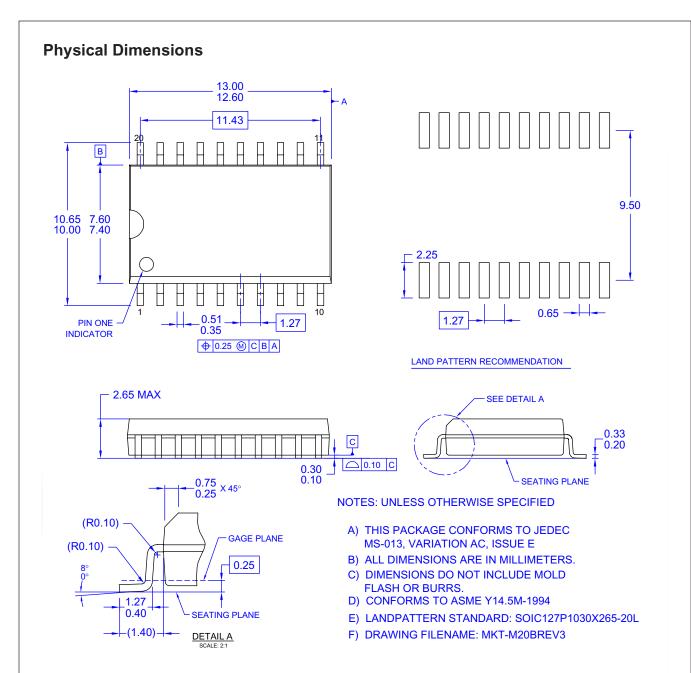
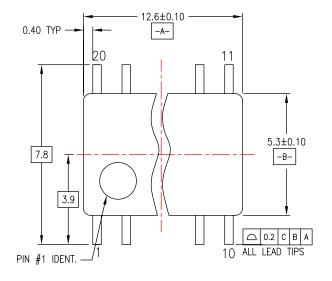
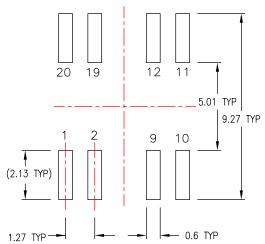


Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

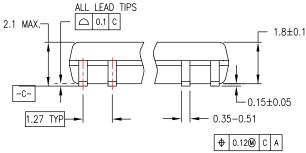
Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

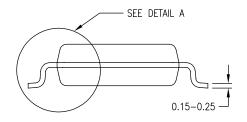
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/





LAND PATTERN RECOMMENDATION

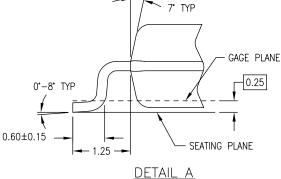




DIMENSIONS ARE IN MILLIMETERS

#### NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  B. DIMENSIONS ARE IN MILLIMETERS.
  C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



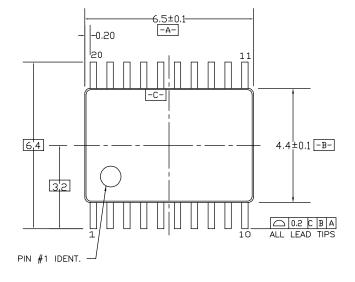
M20DREVC

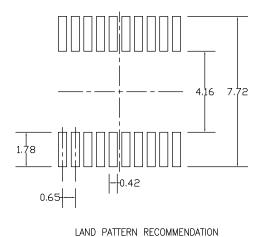
Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

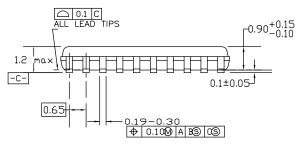
Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/packaging/



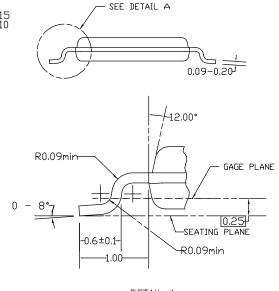






#### NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MD-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



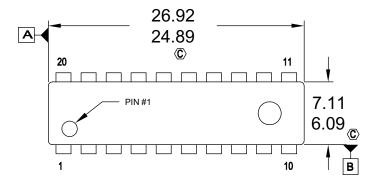
DETAIL A

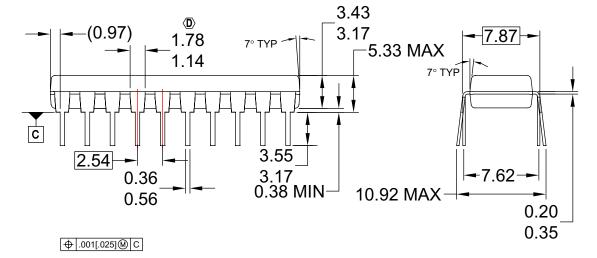
#### MTC20REVD1

#### Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/





NOTES:
A. CONFORMS TO JEDEC REGISTRATION MS-001,
VARIATIONS AD.

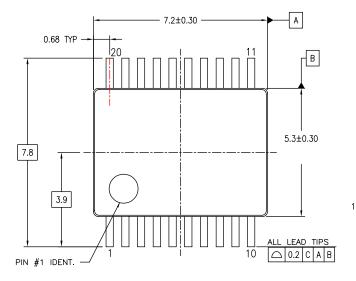
- **B. ALL DIMENSIONS ARE IN MILLIMETERS**
- © DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
  MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED
- 0.25MM.

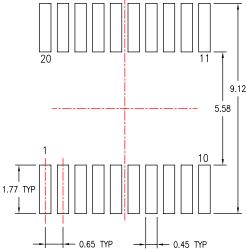
  D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED
- E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- F. DRAWING FILE NAME: N20AREV8

Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

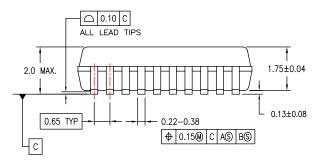
Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

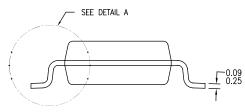
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/





LAND PATTERN RECOMMENDATIONS

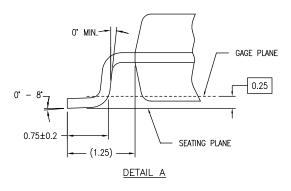




#### DIMENSIONS ARE IN MILLIMETERS

#### NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-150, VARIATION AE, DATE 1/94.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M 1994.



#### MSA20REVB

Figure 5. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/





#### **TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

Build it Now™ CorePLUS™  $CROSSVOLT^{\text{\tiny TM}}$ **CTL™** 

Current Transfer Logic™ EcoSPARK® EZSWITCH™ \*

Fairchild<sup>®</sup> Fairchild Semiconductor® FACT Quiet Series™

FACT<sup>®</sup>  $\mathsf{FAST}^{\mathbb{R}}$ FastvCore™ FlashWriter® FPS™  $\mathsf{FRFET}^{\scriptscriptstyle{\textcircled{\tiny{\$}}}}$ 

Global Power Resource<sup>™</sup>

Green FPS™

Green FPS™ e-Series™

**GTO™** i-Lo™ IntelliMAX™ ISOPLANAR™

MegaBuck™ MICROCOUPLER™ MicroFET™

MicroPak™ MillerDrive™ Motion-SPM™ OPTOLOGIC®

OPTOPLANAR®

PDP-SPM™ Power220® Power247® POWEREDGE® Power-SPM™

Programmable Active Droop™

QFET<sup>©</sup> QS<sup>TM</sup>

QT Optoelectronics™ Quiet Series™ RapidConfigure™ SMART START™

SPM® STEALTH™ SuperFET™ SuperSOT™-3

SuperSOT™-6 SuperSOT™-8

SyncFET™ SYSTEM ®
GENERAL The Power Franchise® bwer franchise PowerTrench® TinyBoost™

TinvBuck™  $\mathsf{TinyLogic}^{\mathbb{R}}$ TINYOPTO™ TinyPower™ TinyPWM™ TinyWire™ uSerDes™ **UHC**®

Ultra FRFET™ UniFET™  $VCX^{TM}$ 

\* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

#### DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS. NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- 2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### **PRODUCT STATUS DEFINITIONS**

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. 132

ON Semiconductor and in are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at <a href="www.onsemi.com/site/pdf/Patent-Marking.pdf">www.onsemi.com/site/pdf/Patent-Marking.pdf</a>. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor and see no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and h

#### **PUBLICATION ORDERING INFORMATION**

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor 19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com N. American Technical Support: 800–282–9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81–3–5817–1050

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative