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FAIRCHILD

SEMICONDUCTOR®

74AC16244 • 74ACT16244
16-Bit Buffer/Line Driver with 3-STATE Outputs

General Description

The AC16244 and ACT16244 contain sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

Features

■ Separate control logic for each byte and nibble
■ 16-bit version of the AC244/ACT244
■ Outputs source/sink 24 mA
■ ACT16244 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC16244SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACT16244SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACT16244MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol
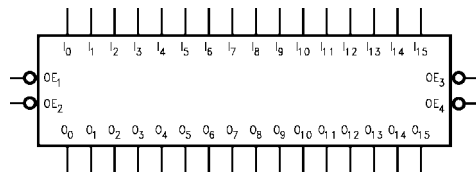
Connection Diagram
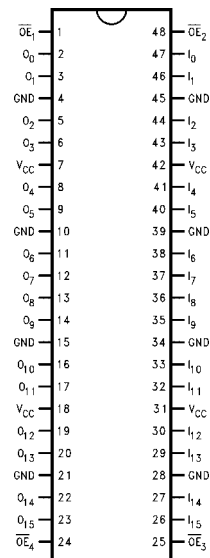
Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$I_0 - I_{15}$	Inputs
$O_0 - O_{15}$	Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Functional Description

The AC16244 and ACT16244 contain sixteen non-inverting buffers with 3-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram
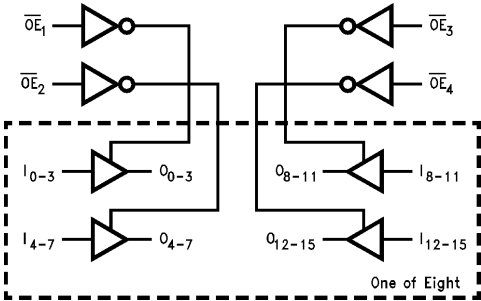
Absolute Maximum Ratings(Note 1)

Supply Voltage (V$_{CC}$)	−0.5V to +7.0V
DC Input Diode Current (I$_{IK}$)	
V$_I$ = − 0.5V	−20 mA
V$_I$ = V$_{CC}$ + 0.5V	+20 mA
DC Output Diode Current (I$_{OK}$)	
V$_O$ = −0.5V	−20 mA
V$_O$ = V$_{CC}$ + 0.5V	+20 mA
DC Output Voltage (V$_O$)	−0.5V to V$_{CC}$ + 0.5V
DC Output Source/Sink Current (I$_O$)	±50 mA
DC V$_{CC}$ or Ground Current	
per Output Pin	±50 mA
Junction Temperature	+140°C
Storage Temperature	−65°C to +150°C

Recommended Operating Conditions

Supply Voltage (V$_{CC}$)	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V$_I$)	0V to V$_{CC}$
Output Voltage (V$_O$)	0V to V$_{CC}$
Operating Temperature (T$_A$)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	
AC Devices	
V$_{IN}$ from 30% to 70%	
V$_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
ACT Devices	
V$_{IN}$ from 0.8V to 2.0V	
V$_{CC}$ @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V$_{CC}$ (V)	T$_A$ = +25°C Typ	T$_A$ = +25°C Guaranteed Limits	T$_A$ = −40°C to +85°C Guaranteed Limits	Units	Conditions
V$_{IH}$	Minimum HIGH Input Voltage	3.0	1.5	2.1	2.1		V$_{OUT}$ = 0.1V
		4.5	2.25	3.15	3.15	V	or V$_{CC}$ − 0.1V
		5.5	2.75	3.85	3.85		
V$_{IL}$	Maximum LOW Input Voltage	3.0	1.5	0.9	0.9		V$_{OUT}$ = 0.1V
		4.5	2.25	1.35	1.35	V	or V$_{CC}$ − 0.1V
		5.5	2.75	1.65	1.65		
V$_{OH}$	Minimum HIGH Output Voltage	3.0	2.99	2.9	2.9		
		4.5	4.49	4.4	4.4	V	I$_{OUT}$ = −50 μA
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46		I$_{OH}$ = -12 mA
		4.5		3.86	3.76	V	I$_{OH}$ = −24 mA
		5.5		4.86	4.76		I$_{OH}$ = −24 mA (Note 2)
V$_{OL}$	Maximum LOW Output Voltage	3.0	0.002	0.1	0.1		
		4.5	0.001	0.1	0.1	V	I$_{OUT}$ = 50 μA
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44		I$_{OL}$ = 12 mA
		4.5		0.36	0.44	V	I$_{OL}$ = 24 mA
		5.5		0.36	0.44		I$_{OL}$ = 24 mA (Note 2)
I$_{OZ}$	Maximum 3-STATE Leakage Current	5.5		0.50	± 5.0	μA	V$_I$ (OE) = V$_{IL}$, V$_{IH}$ V$_I$ = V$_{CC}$, GND V$_O$ = V$_{CC}$, GND
I$_{IN}$	Maximum Input Leakage Current (Note 3)	5.5		± 0.1	± 1.0	μA	V$_I$ = V$_{CC}$, GND
I$_{CC}$	Max Quiescent Supply Current (Note 3)	5.5		8.0	80.0	μA	V$_{IN}$ = V$_{CC}$ or GND
I$_{OLD}$	Minimum Dynamic	5.5			75	mA	V$_{OLD}$ = 1.65V Max
I$_{OHD}$	Output Current (Note 4)	5.5			−75	mA	V$_{OHD}$ = 3.85V Min

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: I$_{IN}$ and I$_{CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V$_{CC}$.

Note 4: Maximum test duration 2.0 millisecond; one output loaded at a time.

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = +25°C$ Guaranteed Limits	$T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
V_{IH}	Minimum HIGH Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA
		5.5		4.86	4.76		$I_{OH} = -24$ mA (Note 5)
V_{OL}	Maximum LOW Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = 24$ mA
		5.5		0.36	0.44		$I_{OH} = 24$ mA (Note 5)
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		± 0.5	± 5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} -2.1V$
I_{CC}	Max Quiescent Supply Current	5.5		8.0	80.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 6)				−75	mA	$V_{OHD} = 3.85V$ Min

Note 5: All outputs loaded; thresholds associated with output under test.

Note 6: Maximum test duration 2.0 millisecond; one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_CC (V) (Note 7)	T_A = +25°C, C_L = 50 pF Min	Typ	Max	T_A = −40°C to +85°C, C_L = 50 pF Min	Max	Units
t_{PLH}	Propagation Delay Data to Output	3.3	2.0	6.3	9.4	2.0	10.8	ns
		5.0	1.6	4.6	6.5	1.6	7.1	
t_{PHL}	Propagation Delay Data to Output	3.3	2.4	5.7	10.7	2.4	11.8	ns
		5.0	2.0	4.3	7.0	2.0	7.9	
t_{PZH}	Output Enable Time	3.3	2.2	6.2	10	2.2	11.5	ns
		5.0	1.7	4.6	6.7	1.7	7.5	
t_{PZL}	Output Enable Time	3.3	2.9	6.4	13.0	2.9	14.6	ns
		5.0	2.2	4.7	8.1	2.2	9.0	
t_{PHZ}	Output Disable Time	3.3	3.1	5.5	8.4	3.1	9.1	ns
		5.0	1.9	3.9	7.8	1.9	8.4	
t_{PLZ}	Output Disable Time	3.3	2.4	4.7	8.1	2.4	8.8	ns
		5.0	1.7	3.6	7.2	1.7	7.6	

Note 7: Voltage Range 5.0 is 5.0V ± 0.5V.
Voltage Range 3.3 is 3.3V ± 0.3V.
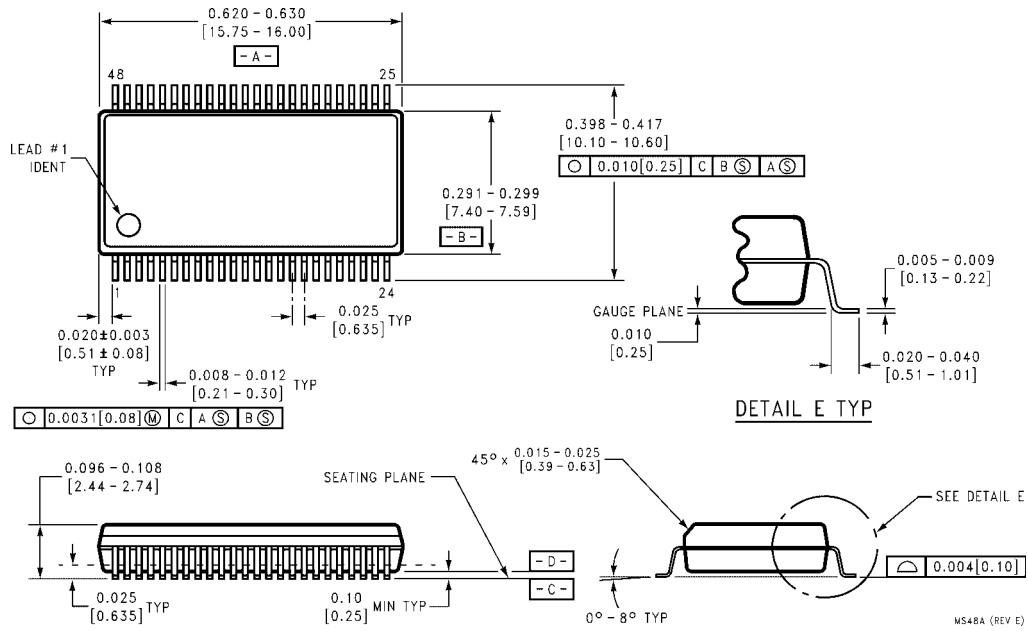
AC Electrical Characteristics for ACT

Symbol	Parameter	V_CC (V) (Note 8)	T_A = +25°C, C_L = 50 pF Min	Typ	Max	T_A = −40°C to +85°C, C_L = 50 pF Min	Max	Units
t_{PLH}	Propagation Delay	5.0	3.0	5.2	7.3	3.0	7.8	ns
t_{PHL}	Data to Output		2.5	4.8	6.8	2.5	7.3	
t_{PZH}	Output Enable	5.0	2.5	5.0	7.4	2.5	7.9	ns
t_{PZL}	Time		2.7	4.6	7.5	2.7	8.0	
t_{PHZ}	Output Disable	5.0	2.3	5.0	7.9	2.3	8.2	ns
t_{PLZ}	Time		2.0	4.6	7.4	2.0	7.9	

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter		Typ	Units	Conditions
C_{IN}	Input Pin Capacitance		4.5	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance		12	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	74AC16244	35	pF	$V_{CC} = 5.0V$
		74ACT16244	30		

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Physical Dimensions inches (millimeters) unless otherwise noted

0.620 – 0.630
[15.75 – 16.00]
– A –

48   25

LEAD #1
IDENT

0.398 – 0.417
[10.10 – 10.60]
○ | 0.010 [0.25] | C | B ⓢ | A ⓢ

0.291 – 0.299
[7.40 – 7.59]
– B –

0.005 – 0.009
[0.13 – 0.22]

GAUGE PLANE
0.010
[0.25]

0.020 – 0.040
[0.51 – 1.01]

DETAIL E TYP

1   24

0.020±0.003
[0.51 ± 0.08]
TYP

0.025
[0.635] TYP

0.008 – 0.012
[0.21 – 0.30] TYP

○ | 0.0031 [0.08] Ⓜ | C | A ⓢ | B ⓢ

0.096 – 0.108
[2.44 – 2.74]

SEATING PLANE

45° x 0.015 – 0.025
[0.39 – 0.63]

SEE DETAIL E

– D –
– C –

0.025
[0.635] TYP

0.10
[0.25] MIN TYP

0° – 8° TYP

△ | 0.004 [0.10]

MS48A (REV E)

**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A**

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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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