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August 1999 Revised May 2005

74AC16244 • 74ACT16244 16-Bit Buffer/Line Driver with 3-STATE Outputs

General Description

The AC16244 and ACT16244 contain sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

Features

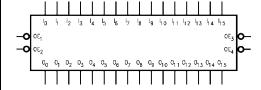
- Separate control logic for each byte and nibble
- 16-bit version of the AC244/ACT244
- Outputs source/sink 24 mA
- ACT16244 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC16244SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACT16244SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACT16244MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

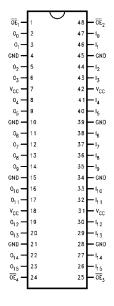
Logic Symbol



Pin Descriptions

Pin Names	Description
OE _n	Output Enable Input (Active LOW)
I ₀ - I ₁₅	Inputs
O ₀ - 0 ₁₅	Outputs

Connection Diagram



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Functional Description

The AC16244 and ACT16244 contain sixteen non-inverting buffers with 3-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The

3-STATE outputs are controlled by an Output Enable (\overline{OE}_n) input for each nibble. When \overline{OE}_n is LOW, the outputs are in 2-state mode. When \overline{OE}_n is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Truth Tables

In	Inputs		
ŌE ₁	I ₀ –I ₃	O ₀ -O ₃	
L	L	L	
L	Н	н	
Н	X	Z	

Inp	Inputs		
ŌE ₂	I ₄ –I ₇	O ₄ -O ₇	
L	L	L	
L	Н	Н	
Н	X	Z	

 $I_{12} - I_{15}$

Н

Χ

Outputs

O₁₂-O₁₅

H Z

Inputs

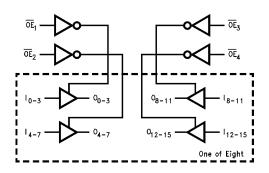
Inj	Inputs		
ŌE ₃	I ₈ –I ₁₁	O ₈ -O ₁₁	
L	L	L	
L	Н	Н	
н	X	Z	

H X = Immaterial

OE₄

L L

Logic Diagram



L = LOW Voltage Level H = HIGH Voltage Level

X = Immaterial Z = High Impedance

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) -0.5V to +7.0V

DC Input Diode Current (I_{IK})

 $V_{I} = -0.5V$ -20 mA $V_{I} = V_{CC} + 0.5V$ +20 mA

DC Output Diode Current (I_{OK})

 $\begin{aligned} & \text{V}_{\text{O}} = -0.5 \text{V} & -20 \text{ mA} \\ & \text{V}_{\text{O}} = \text{V}_{\text{CC}} + 0.5 \text{V} & \pm 20 \text{ mA} \\ & \text{DC Output Voltage (V}_{\text{O}}) & -0.5 \text{V to V}_{\text{CC}} + 0.5 \text{V} \\ & \text{DC Output Source/Sink Current (I}_{\text{O}}) & \pm 50 \text{ mA} \end{aligned}$

DC V_{CC} or Ground Current

per Output Pin ± 50 mA

Junction Temperature +140 °C

Storage Temperature -65 °C to +150 °C

Recommended Operating Conditions

Supply Voltage (V_{CC})

AC 2.0V to 6.0V ACT 4.5V to 5.5V Input Voltage (V_I) 0V to V_{CC} Output Voltage (V_O) 0V to V_{CC} Operating Temperature (T_A) -40°C to +85°C

Minimum Input Edge Rate $(\Delta V/\Delta t)$

AC Devices

V_{IN} from 30% to 70%

V_{CC} @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate ($\Delta V/\Delta t$)

ACT Devices

 V_{IN} from 0.8V to 2.0V

V_{CC} @ 4.5V, 5.5V 125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACTT circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	v _{cc}	T _A = -	+25°C	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions	
Syllibol	Farameter	(V)	Тур	Gua	Guaranteed Limits		Conditions	
V _{IH}	Minimum HIGH Input Voltage	3.0	1.5	2.1	2.1		V _{OUT} = 0.1V	
		4.5	2.25	3.15	3.15	V	or V _{CC} - 0.1V	
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum LOW Input Voltage	3.0	1.5	0.9	0.9		V _{OUT} = 0.1V	
		4.5	2.25	1.35	1.35	V	or V _{CC} – 0.1V	
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum HIGH Output Voltage	3.0	2.99	2.9	2.9			
		4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46		I _{OH} = -12 mA	
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$	
		5.5		4.86	4.76		$I_{OH} = -24 \text{ mA (Note 2)}$	
V _{OL}	Maximum LOW Output Voltage	3.0	0.002	0.1	0.1			
		4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44		I _{OL} = 12 mA	
		4.5		0.36	0.44	V	$I_{OL} = 24 \text{ mA}$	
		5.5		0.36	0.44		I _{OL} = 24 mA (Note 2)	
I _{OZ}	Maximum 3-STATE Leakage Current	5.5		0.50	± 5.0	μА	V_{I} (OE) = V_{IL} , V_{IH}	
							$V_I = V_{CC}$, GND	
							$V_O = V_{CC}$, GND	
I _{IN}	Maximum Input Leakage Current (Note 3)	5.5		± 0.1	± 1.0	μА	$V_I = V_{CC}$, GND	
I _{CC}	Max Quiescent Supply Current (Note 3)	5.5		8.0	80.0	μА	V _{IN} = V _{CC} or GND	
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max	
I _{OHD}	Output Current (Note 4)	5.5			-75	mA	V _{OHD} = 3.85V Min	

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: $I_{\rm IN}$ and $I_{\rm CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V $V_{\rm CC}$.

Note 4: Maximum test duration 2.0 millisecond; one output loaded at a time.

74AC16244 • 74ACT16244

DC Electrical Characteristics for ACT $T_A = +25^{\circ}C$ $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ v_{cc} Units Conditions Symbol (V) Guaranteed Limits Тур Minimum HIGH Input Voltage 4.5 1.5 $V_{OUT} = 0.1V$ 5.5 1.5 2.0 or V_{CC} - 0.1V V_{IL} V_{OUT} = 0.1V Maximum LOW Input Voltage 4.5 1.5 0.8 5.5 or V_{CC} – 0.1V1.5 8.0 0.8 V_{OH} Minimum HIGH Output Voltage 4.5 4.49 4.4 4.4 $I_{OUT} = -50 \ \mu A$ 5.5 5.49 5.4 5.4 $V_{IN} = V_{IL}$ or V_{IH} 4.5 3.86 3.76 ٧ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 5)}$ 5.5 4.86 4.76 Maximum LOW Output Voltage 4.5 0.001 0.1 0.1 V_{OL} $I_{OUT} = 50 \; \mu A$ 0.1 $V_{IN} = V_{IL}$ or V_{IH} 4.5 0.44 0.36 $I_{OH}=24\ mA$ $I_{OH} = 24 \text{ mA (Note 5)}$ 5.5 0.36 0.44 Maximum 3-STATE Leakage Current 5.5 ± 0.5 ± 5.0 $V_I = V_{IL}, V_{IH}$ I_{OZ} μΑ $V_O = V_{CC}$, GND $V_I = V_{CC}$, GND I_{IN} Maximum Input Leakage Current 5.5 $\pm\,0.1$ ± 1.0 μА Maximum I_{CC}/Input 5.5 1.5 $V_I = V_{CC} - 2.1V$ I_{CCT} 0.6 Max Quiescent Supply Current 5.5 8.0 80.0 $V_{IN} = V_{CC}$ or GND μА I_{CC} V_{OLD} = 1.65V Max Minimum Dynamic 75 I_{OLD} mΑ Output Current (Note 6) -75 mA V_{OHD} = 3.85V Min I_{OHD}

Note 5: All outputs loaded; thresholds associated with output under test.

Note 6: Maximum test duration 2.0 millisecond; one output loaded at a time.

AC Electrical Characteristics for AC

		V _{CC}		$T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		
Symbol	Parameter	(V)	C _L = 50 pF			$C_L = 50 pF$		Units
		(Note 7)	Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay	3.3	2.0	6.3	9.4	2.0	10.8	ns
	Data to Output	5.0	1.6	4.6	6.5	1.6	7.1	115
t _{PHL}	Propagation Delay	3.3	2.4	5.7	10.7	2.4	11.8	ns
	Data to Output	5.0	2.0	4.3	7.0	2.0	7.9	115
t _{PZH}	Output Enable Time	3.3	2.2	6.2	10	2.2	11.5	ns
		5.0	1.7	4.6	6.7	1.7	7.5	115
t _{PZL}	Output Enable Time	3.3	2.9	6.4	13.0	2.9	14.6	ns
		5.0	2.2	4.7	8.1	2.2	9.0	115
t _{PHZ}	Output Disable Time	3.3	3.1	5.5	8.4	3.1	9.1	ns
		5.0	1.9	3.9	7.8	1.9	8.4	115
t _{PLZ}	Output Disable Time	3.3	2.4	4.7	8.1	2.4	8.8	ns
		5.0	1.7	3.6	7.2	1.7	7.6	115

Note 7: Voltage Range 5.0 is $5.0V \pm 0.5V$. Voltage Range 3.3 is $3.3V \pm 0.3V$.

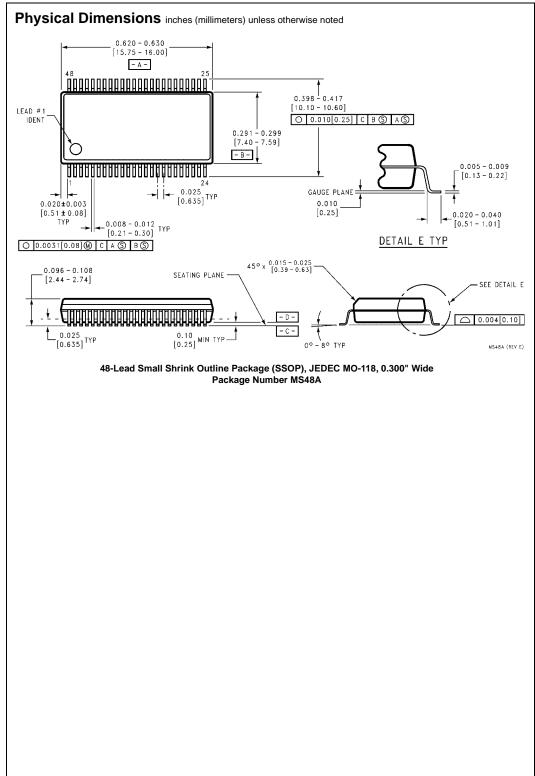
AC Electrical Characteristics for ACT

		V _{CC}		$T_A = +25^{\circ}C$		T _A = -40°	C to +85°C	
Symbol	Parameter	(V)	C _L = 50 pF			$C_L = 50 \text{ pF}$		Units
		(Note 8)	Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay	5.0	3.0	5.2	7.3	3.0	7.8	ns
t _{PHL}	Data to Output	5.0	2.5	4.8	6.8	2.5	7.3	115
t _{PZH}	Output Enable	F.0	2.5	5.0	7.4	2.5	7.9	no
t_{PZL}	Time	5.0	2.7	4.6	7.5	2.7	8.0	ns
t _{PHZ}	Output Disable	5.0	2.3	5.0	7.9	2.3	8.2	ns
t _{PLZ}	Time	3.0	2.0	4.6	7.4	2.0	7.9	115

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter		Тур	Units	Conditions
C _{IN}	Input Pin Capacitance	nput Pin Capacitance			V _{CC} = 5.0V
C _{OUT}	Output Pin Capacitance		12	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	74AC16244	35	pF	V 50V
		74ACT16244	30	þг	V _{CC} = 5.0V



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 12.50±0.10 0.40 TYP -B-0±0.10 4.60 -B.10 4.05 O.2 C B A ALL LEAD TIPS PIN #1 IDENT - 0.30 LAND PATTERN RECOMMENDATION □ 0.1 C SEE DETAIL A 0.90+0.15 0.09-0.20 0.10±0.05 0.50 0.17-0.27 ♦ 0.13\(\text{A} \) A B\(\text{S} \) C\(\text{S} \) 12.00' TOP & BOTTOM R0.16 DIMENSIONS ARE IN MILLIMETERS GAGE PLANE 0.25 NOTES: A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED. DATE 4/97. B. DIMENSIONS ARE IN MILLIMETERS. SEATING PLANE 0.60±0.10 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. DETAIL A MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

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