FAIRCHILD SEMICONDUCTOR®

August 1999
Revised May 2005

74ACT16245
16-Bit Transceiver with 3-STATE Outputs

General Description

The ACT16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each has separate control inputs which can be shorted together for full 16-bit operation. The T/$\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

Features

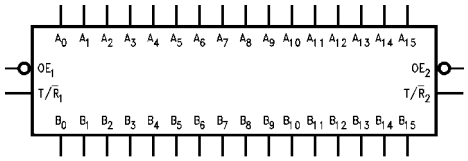
- Bidirectional non-inverting buffers
- Separate control logic for each byte
- 16-bit version of the ACT245
- Outputs source/sink 24 mA
- TTL-compatible inputs

Ordering Code:

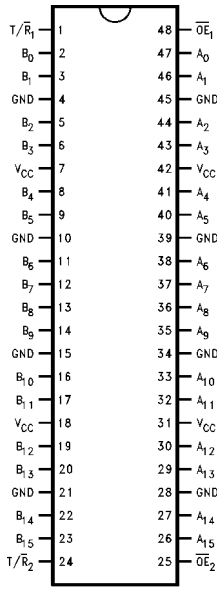
Order Number	Package Number	Package Description
74ACT16245SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACT16245MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/Outputs
B_0–B_{15}	Side B Outputs/Inputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Functional Description

The ACT16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the T/$\overline{R}$ input is HIGH, then Bus A data is transmitted to Bus B. When the T/$\overline{R}$ input is LOW, Bus B data is transmitted to Bus A. The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each byte. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

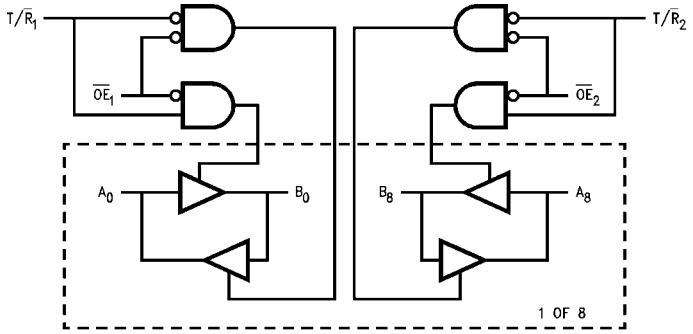
Truth Tables

Inputs		Outputs
$\overline{OE}_1$	T/$\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	T/$\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to + 7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source/Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin	± 50 mA
Storage Temperature	−65°C to +150°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C	T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Input Voltage	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 2)
V_{OL}	Maximum LOW Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.5	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} −2.1V
I_{CC}	Max Quiescent Supply Current	5.5		8.0	80.0	μA	V_{IN} = V_{CC} or GND
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}					−75	mA	V_{OHD} = 3.85V Min

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: Maximum test duration 2.0 ms; one output loaded at a time.

AC Electrical Characteristics

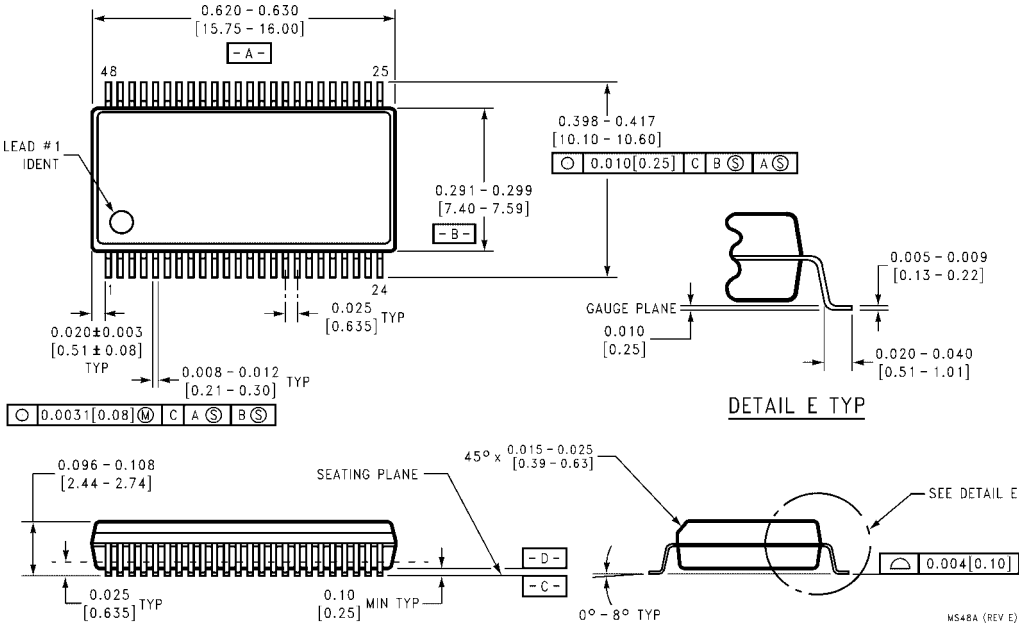
Symbol	Parameter	V_{CC} (V) (Note 4)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation	5.0	3.2	5.7	8.4	3.2	9.0	ns
t_{PHL}	Delay A_n, B_n to B_n, A_n		2.6	5.1	7.9	2.6	8.4	
t_{PZH}	Output Enable	5.0	3.7	6.4	9.4	2.7	10.0	ns
t_{PZL}	Time		4.1	7.4	10.5	3.4	11.6	
t_{PHZ}	Output Disable	5.0	2.2	5.4	8.7	2.2	9.3	ns
t_{PLZ}	Time		2.0	5.2	8.2	2.0	8.8	

Note 4: Voltage Range 5.0 is 5.0V ± 0.5V.

Capacitance

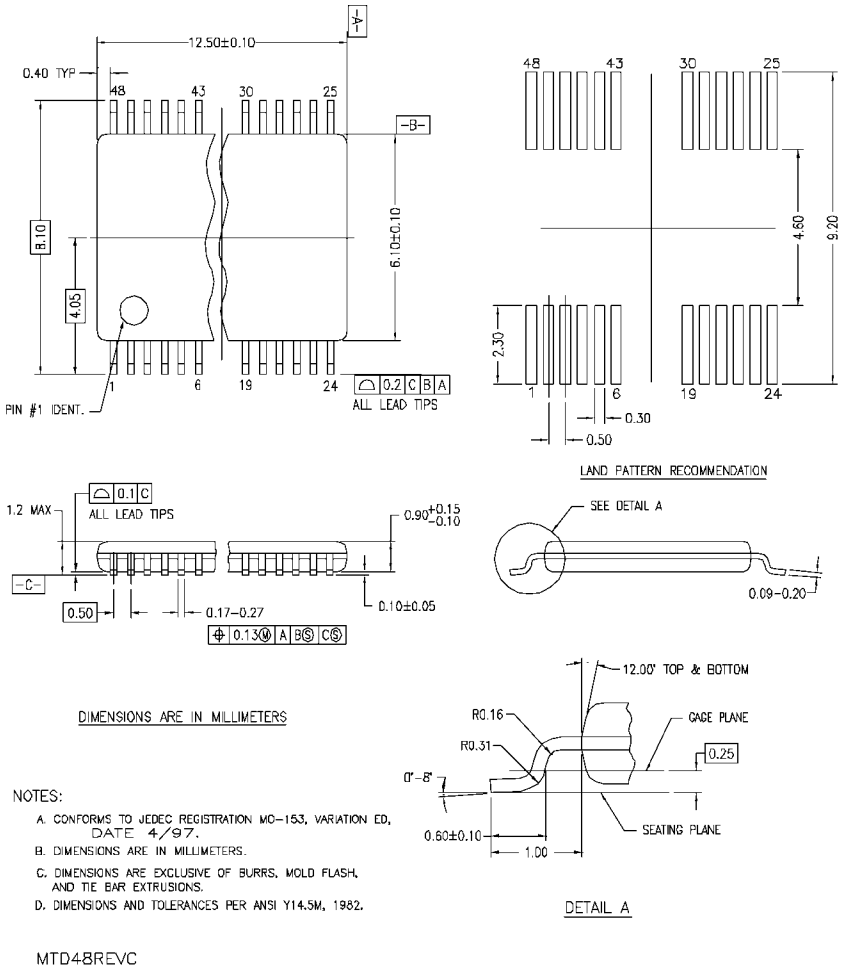
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	25	pF	$V_{CC} = 5.0V$

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com