

# 74ACTQ32

## Quiet Series Quad 2-Input OR Gate

### Features

- $I_{CC}$  reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Minimum 4kV ESD protection
- TTL-compatible inputs
- Outputs source/sink 24mA

### General Description

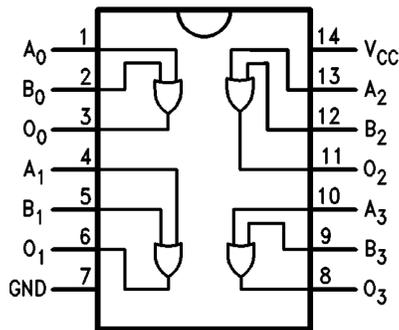
The ACTQ320 contains four, 2-input OR gates and utilizes Fairchild Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior ACMOS performance.

### Ordering Information

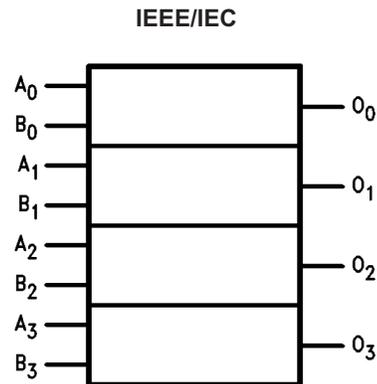
Order Number	Package Number	Package Description
74ACTQ32SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACTQ32SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

### Connection Diagram



### Logic Symbol



### Pin Description

Pin Names	Descriptions
$A_n, B_n$	Inputs
$\bar{O}_n$	Outputs

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$I_{IK}$	DC Input Diode Current	
	$V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	-20mA +20mA
$V_I$	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
$I_{OK}$	DC Output Diode Current	
	$V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	-20mA +20mA
$V_O$	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
$I_O$	DC Output Source or Sink Current	$\pm 50mA$
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Output Pin	$\pm 50mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C
	DC Latch-Up Source or Sink Current	$\pm 300mA$
$T_J$	Junction Temperature	140°C

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	4.5V to 5.5V
$V_I$	Input Voltage	0V to $V_{CC}$
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate: $V_{IN}$ from 0.8V to 2.0V, $V_{CC}$ @ 4.5V, 5.5V	125mV/ns

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -55°C to +125°C	T <sub>A</sub> = -40°C to +85°C	Units
				Typ.	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.0	2.0	2.0	V
		5.5		1.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.8	0.8	0.8	V
		5.5		1.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	I <sub>OUT</sub> = -50μA	4.49	4.4	4.4	4.4	V
		5.5		5.49	5.4	5.4	5.4	
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> : I <sub>OH</sub> = -24mA		3.86	3.70	3.76	
		5.5	I <sub>OH</sub> = -24mA <sup>(1)</sup>		4.86	4.70	4.76	
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	I <sub>OUT</sub> = 50μA	0.001	0.1	0.1	0.1	V
		5.5		0.001	0.1	0.1	0.1	
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> : I <sub>OL</sub> = 24mA		0.36	0.50	0.44	
		5.5	I <sub>OL</sub> = 24mA <sup>(1)</sup>		0.36	0.50	0.44	
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	±1.0	±1.0	μA
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	0.6		1.6	1.5	mA
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(2)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			50	75	mA
I <sub>OHD</sub>		5.5	V <sub>OHD</sub> = 3.85V Min.			-50	-75	mA
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.0	40.0	20.0	μA
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	Figures 1 & 2 <sup>(3)</sup>	1.1	1.5			V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	Figures 1 & 2 <sup>(3)</sup>	-0.6	-1.2			V
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	5.0	<sup>(4)</sup>	1.9	2.2			V
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage	5.0	<sup>(4)</sup>	1.2	0.8			V

**Notes:**

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. Max number of outputs defined as (n). Data inputs are 0V to 3V. One output @ GND.
4. Max number of data inputs (n) switching. (n-1) inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1MHz.

## AC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V) <sup>(5)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50$ pF			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , $C_L = 50$ pF		Units
			Min.	Typ.	Max.	Min	Max	
$t_{PLH}$	Propagation Delay, Data to Output	5.0	2.5	6.0	6.5	2.5	7.0	ns
$t_{PHL}$	Propagation Delay, Data to Output	5.0	2.0	6.0	6.5	2.5	7.0	ns
$t_{OSHL}$ , $t_{OSLH}$	Output to Output Skew <sup>(6)</sup>	5.0		0.5	1.0		1.0	ns

### Notes:

- Voltage range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ .
- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Conditions	Typ.	Units
$C_{IN}$	Input Capacitance	$V_{CC} = \text{OPEN}$	4.5	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CC} = 5.0\text{V}$	68	pF

## FACT Noise Characteristics

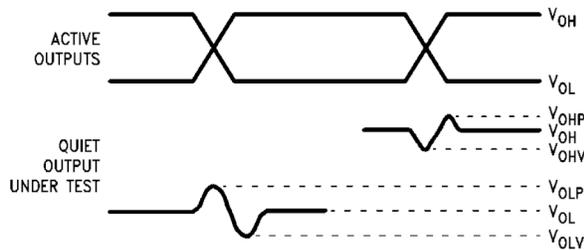
The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

### Equipment

Hewlett Packard Model 8180A Word Generator  
 PC-163A Test Fixture  
 Tektronics Model 7854 Oscilloscope

### Procedure:

1. Verify Test Fixture Loading: Standard Load 50pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.



### Notes:

7.  $V_{OHV}$  and  $V_{OLP}$  are measured with respect to ground reference.
8. Input pulses have the following characteristics:  
 $f = 1\text{MHz}$ ,  $t_r = 3\text{ns}$ ,  $t_f = 3\text{ns}$ , skew < 150ps.

**Figure 1. Quiet Output Noise Voltage Waveforms**

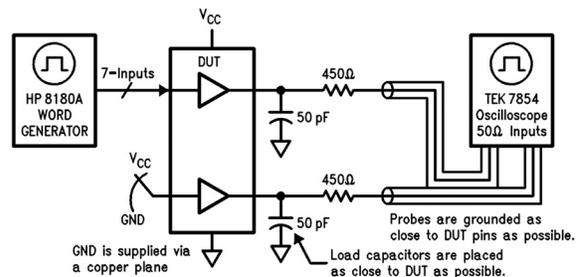
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACTQ devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

### $V_{OLP}/V_{OLV}$ and $V_{OHP}/V_{OHV}$ :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure  $V_{OLP}$  and  $V_{OLV}$  on the quiet output during the worst case transition for active and enable. Measure  $V_{OHP}$  and  $V_{OHV}$  on the quiet output during the worst case transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

### $V_{ILD}$ and $V_{IHD}$ :

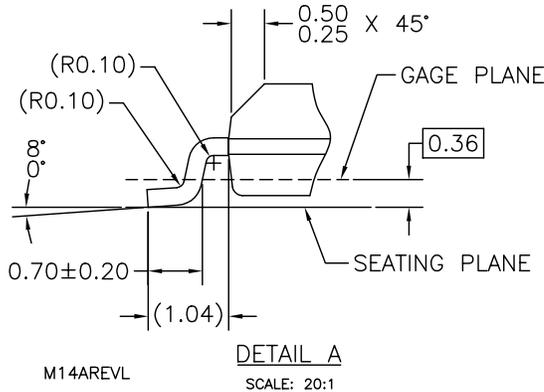
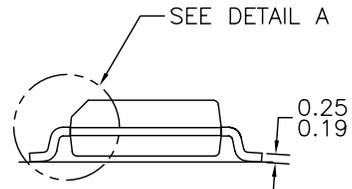
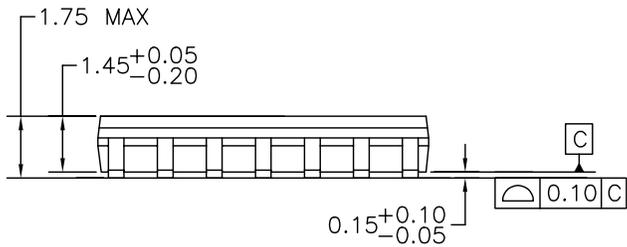
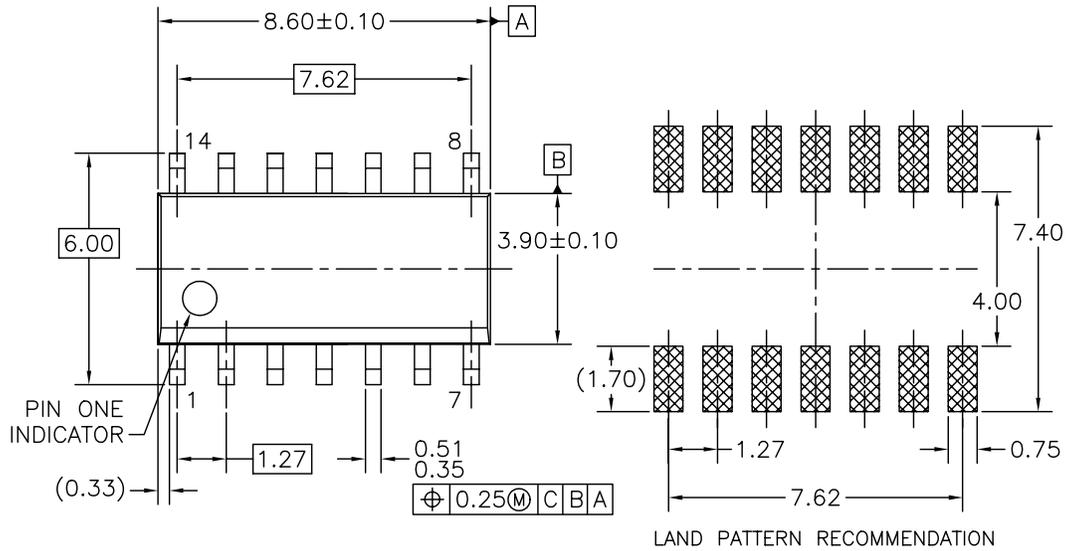
- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level,  $V_{IL}$ , until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input LOW voltage level at which oscillation occurs is defined as  $V_{ILD}$ .
- Next decrease the input HIGH voltage level,  $V_{IH}$ , until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input HIGH voltage level at which oscillation occurs is defined as  $V_{IHD}$ .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.



**Figure 2. Simultaneous Switching Test Circuit**

**Physical Dimensions**

Dimensions are in inches (millimeters) unless otherwise noted.



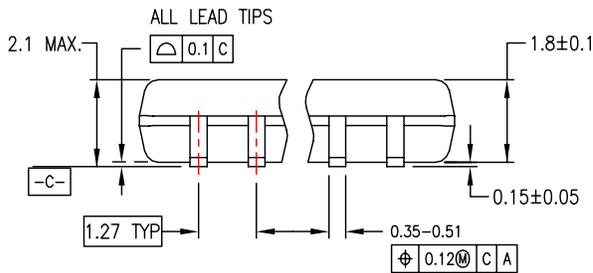
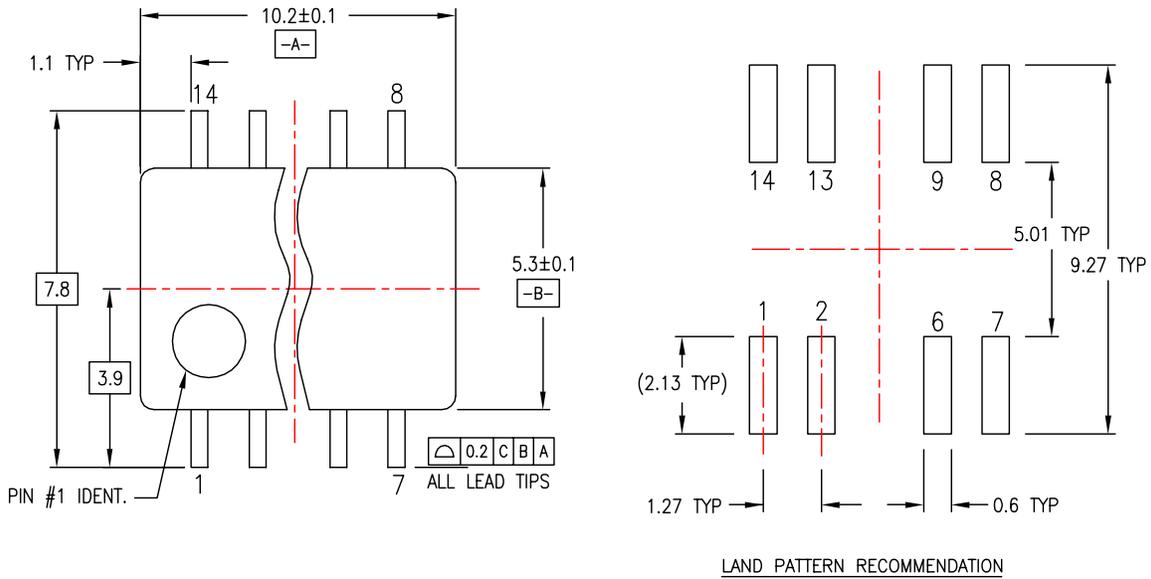
NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.

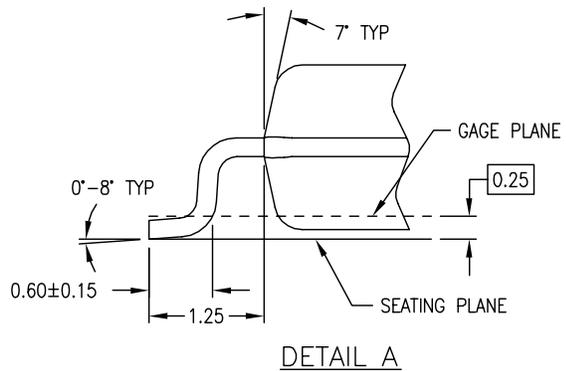
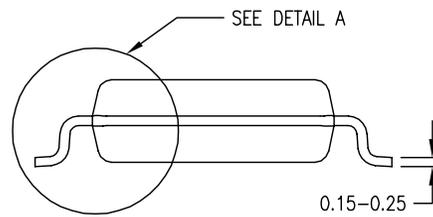
**Figure 3. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A**

**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.



DIMENSIONS ARE IN MILLIMETERS



NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DREVC

**Figure 4. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D**



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FAST <sup>®</sup>	PDP-SPM <sup>™</sup>	SuperSOT <sup>™</sup> -6	
FASTr <sup>™</sup>	POP <sup>™</sup>	SuperSOT <sup>™</sup> -8	
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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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