

74AHC32; 74AHCT32

Quad 2-input OR gate

Rev. 04 — 22 May 2008

Product data sheet

1. General description

The 74AHC32; 74AHCT32 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC32; 74AHCT32 provides the 2-input OR function.

2. Features

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - ◆ For 74AHC32: CMOS level
 - ◆ For 74AHCT32: TTL level
- ESD protection:
 - ◆ HBM EIA/JESD22-A114E exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V
 - ◆ CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to $+85\text{ °C}$ and from -40 °C to $+125\text{ °C}$

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|----------------|-------------------------------------|----------|---|----------|
| | Temperature range | Name | Description | Version |
| 74AHC32 | | | | |
| 74AHC32D | -40 °C to $+125\text{ °C}$ | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74AHC32PW | -40 °C to $+125\text{ °C}$ | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74AHC32BQ | -40 °C to $+125\text{ °C}$ | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$ | SOT762-1 |

Table 1. Ordering information ...continued

| Type number | Package | | | Version |
|-----------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74AHCT32 | | | | |
| 74AHCT32D | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74AHCT32PW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74AHCT32BQ | -40 °C to +125 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |

4. Functional diagram

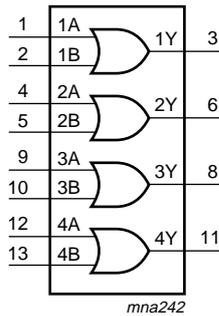


Fig 1. Logic symbol

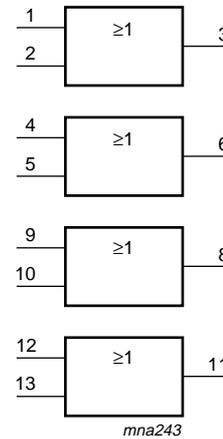


Fig 2. IEC logic symbol

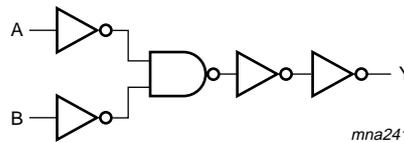
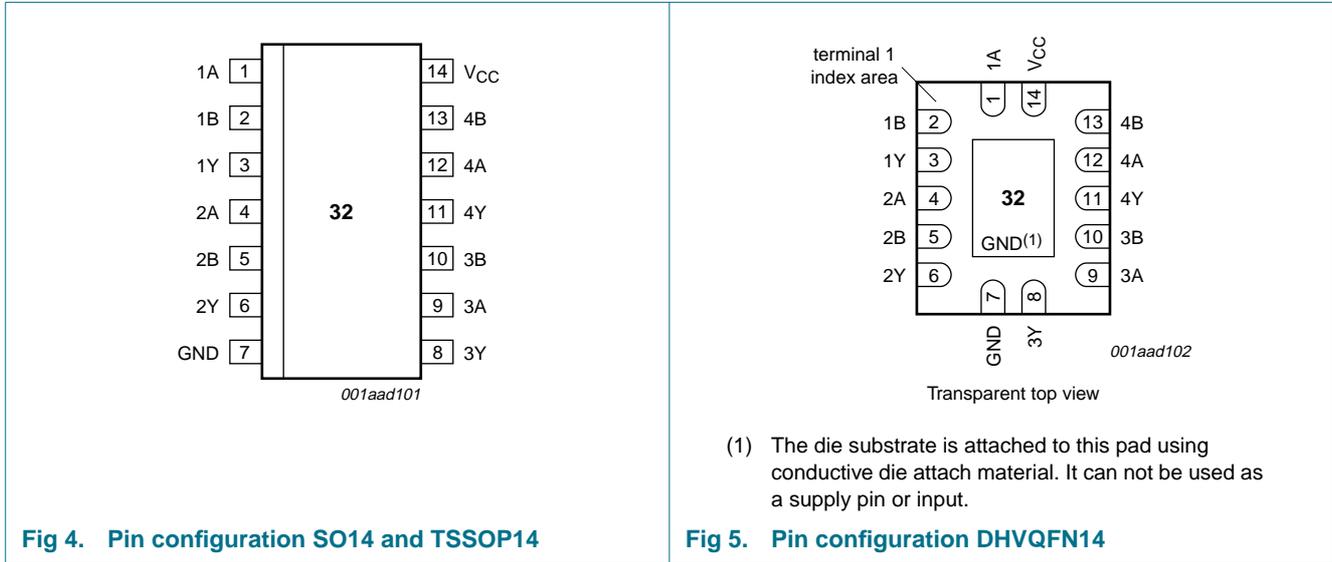


Fig 3. Logic diagram (one gate)

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|-----|----------------|
| 1A | 1 | data input |
| 1B | 2 | data input |
| 1Y | 3 | data output |
| 2A | 4 | data input |
| 2B | 5 | data input |
| 2Y | 6 | data output |
| GND | 7 | ground (0 V) |
| 3Y | 8 | data output |
| 3A | 9 | data input |
| 3B | 10 | data input |
| 4Y | 11 | data output |
| 4A | 12 | data input |
| 4B | 13 | data input |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table^[1]

| Input | | Output | |
|-------|----|--------|--|
| nA | nB | nY | |
| L | L | L | |
| X | H | H | |
| H | X | H | |

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|--------------------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5$ V | ^[1] -20 | - | mA |
| I_{OK} | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V | ^[1] -20 | +20 | mA |
| I_O | output current | $V_O = -0.5$ V to $(V_{CC} + 0.5$ V) | -25 | +25 | mA |
| I_{CC} | supply current | | - | +75 | mA |
| I_{GND} | ground current | | -75 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C | ^[2] - | 500 | mW |

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] For SO14 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
 For TSSOP14 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

8. Recommended operating conditions

Table 5. Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---------------------------|-----|-----|----------|------|
| 74AHC32 | | | | | | |
| V_{CC} | supply voltage | | 2.0 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 3.0$ V to 3.6 V | - | - | 100 | ns/V |
| | | $V_{CC} = 4.5$ V to 5.5 V | - | - | 20 | ns/V |

Table 5. Operating conditions ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|-------------------------------------|----------------------------------|-----|-----|-----------------|------|
| 74AHCT32 | | | | | | |
| V _{CC} | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | 5.5 | V |
| V _O | output voltage | | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 4.5 V to 5.5 V | - | - | 20 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---|--|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74AHC32 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | V _{CC} = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | V _{CC} = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -50 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| | I _O = -8.0 mA; V _{CC} = 4.5 V | 3.94 | - | - | 3.80 | - | 3.70 | - | V | |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 50 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | I _O = 8.0 mA; V _{CC} = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V | |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 2.0 | - | 20 | - | 40 | μA |
| C _I | input capacitance | V _I = V _{CC} or GND | - | 3 | 10 | - | 10 | - | 10 | pF |
| C _O | output capacitance | | - | 4 | - | - | - | - | - | pF |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|---|-------|-----|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74AHCT32 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -50 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -8.0 mA | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 50 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 8.0 mA | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 2.0 | - | 20 | - | 40 | μA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V; other pins at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| C _I | input capacitance | V _I = V _{CC} or GND | - | 3 | 10 | - | 10 | - | 10 | pF |
| C _O | output capacitance | | - | 4 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------------------|--|-------|--------------------|------|------------------|-----|-------------------|------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | Min | Max | |
| 74AHC32 | | | | | | | | | | |
| t _{pd} | propagation delay | nA, nB to nY; see Figure 6 ^[2] | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | | | | | | | | |
| | | C _L = 15 pF | - | 3.9 | 7.9 | 1.0 | 9.5 | 1.0 | 10.0 | ns |
| | | C _L = 50 pF | - | 5.6 | 11.4 | 1.0 | 13 | 1.0 | 14.5 | ns |
| | | V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | C _L = 15 pF | - | 2.8 | 5.5 | 1.0 | 6.5 | 1.0 | 7.0 | ns |
| | | C _L = 50 pF | - | 4.1 | 7.5 | 1.0 | 8.5 | 1.0 | 9.5 | ns |
| C _{PD} | power dissipation capacitance | f _i = 1 MHz; V _I = GND to V _{CC} ^[3] | - | 10 | - | - | - | - | - | pF |

Table 7. Dynamic characteristics ...continued
 Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|--|-------------------------------|--|-------|--------------------|-----|------------------|-----|-------------------|------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | Min | Max | |
| 74AHCT32; V_{CC} = 4.5 V to 5.5 V | | | | | | | | | | |
| t _{pd} | propagation delay | nA, nB to nY; see Figure 6 ^[2] | | | | | | | | |
| | | C _L = 15 pF | - | 3.1 | 6.9 | 1.0 | 8.0 | 1.0 | 9.0 | ns |
| | | C _L = 50 pF | - | 4.3 | 7.9 | 1.0 | 9.0 | 1.0 | 10.0 | ns |
| C _{PD} | power dissipation capacitance | f _i = 1 MHz; V _I = GND to V _{CC} ^[3] | - | 12 | - | - | - | - | - | pF |

- [1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

11. Waveforms

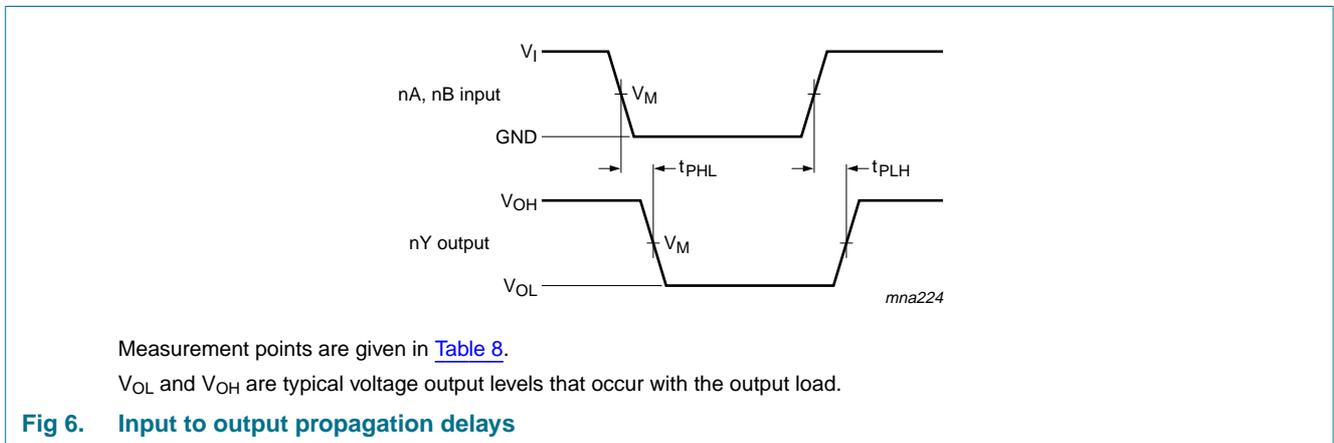
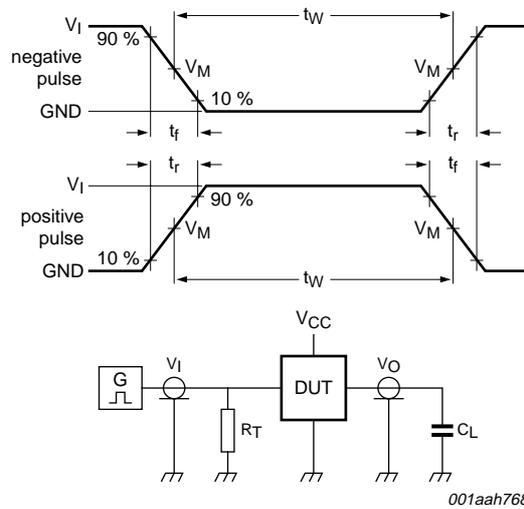


Table 8. Measurement points

| Type | Input | Output |
|----------|-----------------------|-----------------------|
| | V _M | V _M |
| 74AHC32 | 0.5 × V _{CC} | 0.5 × V _{CC} |
| 74AHCT32 | 1.5 V | 0.5 × V _{CC} |



001aah768

Test data is given in [Table 9](#).

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig 7. Load circuitry for measuring switching times

Table 9. Test data

| Type | Input | | Load | Test |
|----------|----------|---------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | |
| 74AHC32 | V_{CC} | ≤ 3.0 ns | 15 pF, 50 pF | t_{PLH}, t_{PHL} |
| 74AHCT32 | 3.0 V | ≤ 3.0 ns | 15 pF, 50 pF | t_{PLH}, t_{PHL} |

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

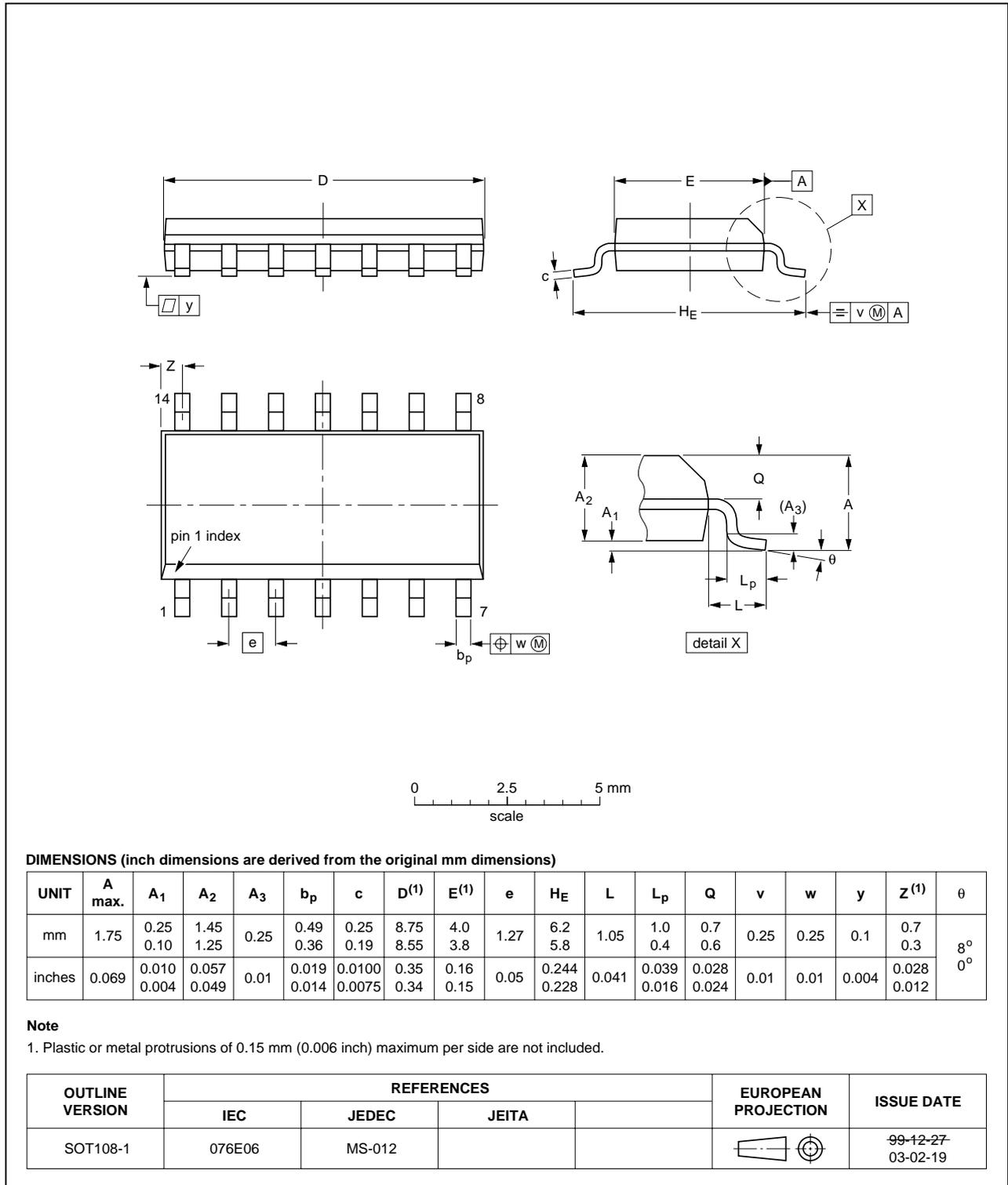


Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

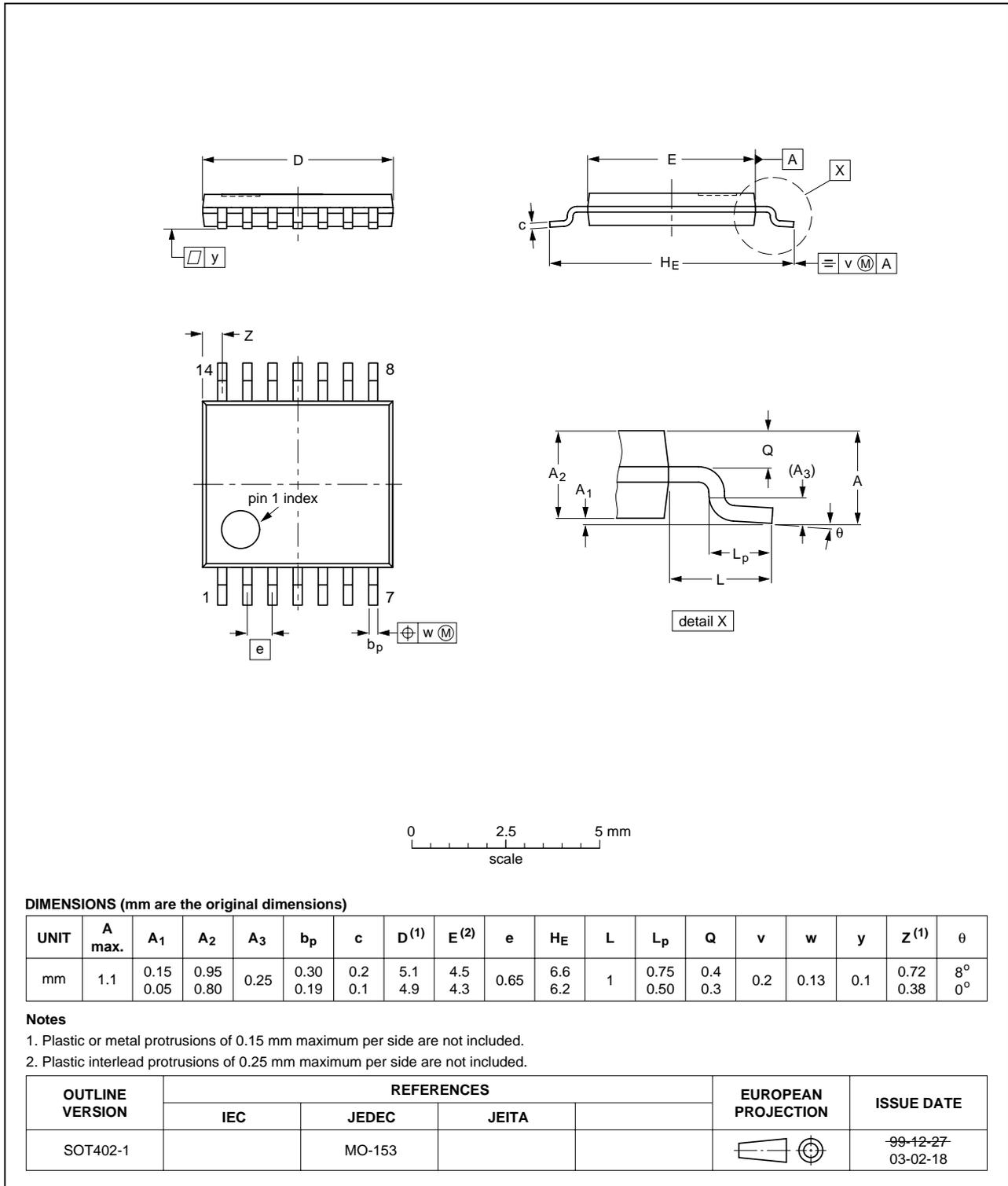


Fig 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

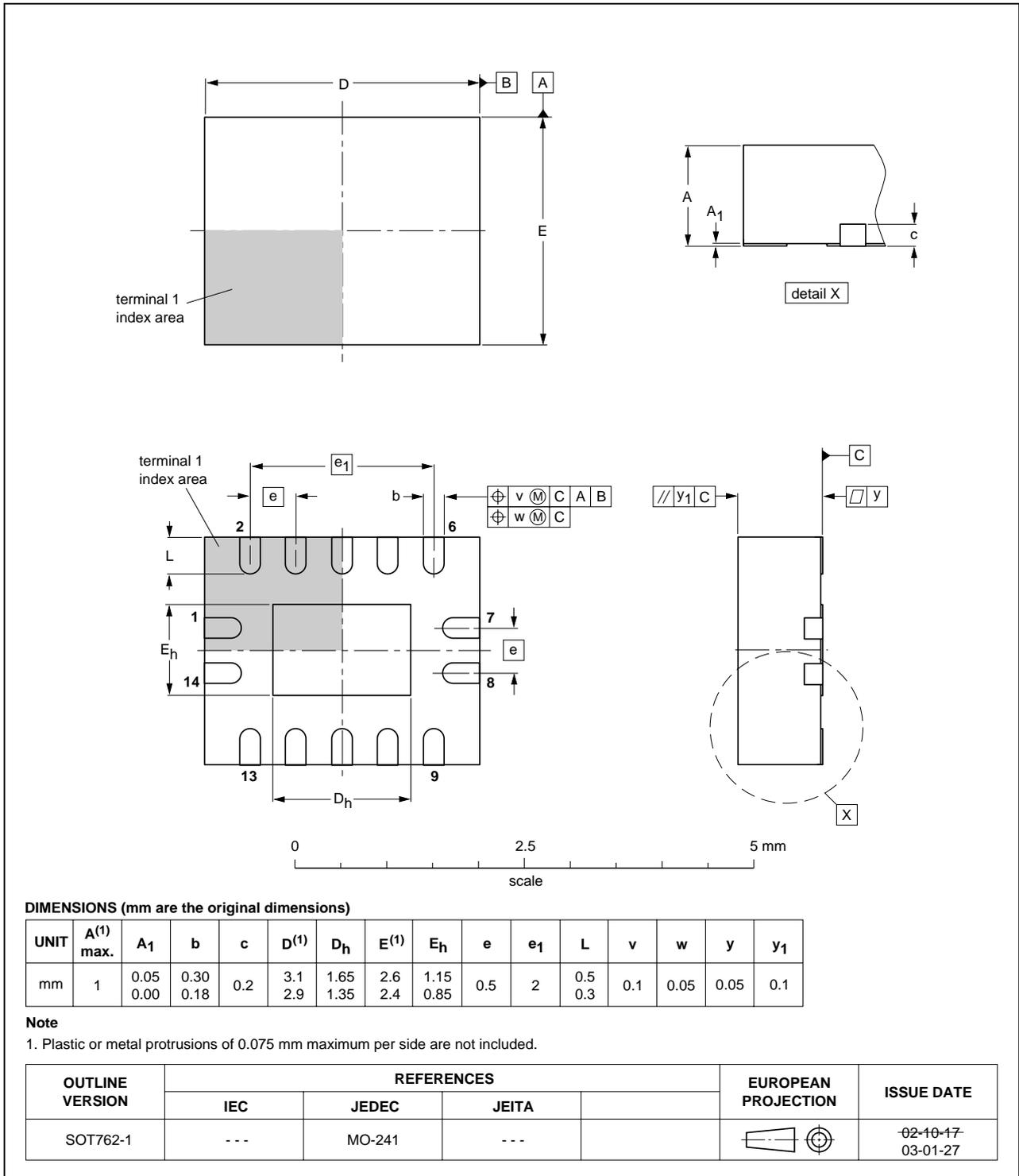


Fig 10. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|--|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| LSTTL | Low-power Schottky Transistor-Transistor Logic |
| MM | Machine Model |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|---------------------------|---------------|----------------|
| 74AHC_AHCT32_4 | 20080522 | Product data sheet | - | 74AHC_AHCT32_3 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Table 6: the conditions for input leakage current have been changed. | | | |
| 74AHC_AHCT32_3 | 20040519 | Product specification | - | 74AHC_AHCT32_2 |
| 74AHC_AHCT32_2 | 19990927 | Product specification | - | 74AHC_AHCT32_1 |
| 74AHC_AHCT32_1 | 19981209 | Preliminary specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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