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Team Nexperia

# 74AHC126-Q100; 74AHCT126-Q100

Quad buffer/line driver; 3-state

Rev. 1 — 10 July 2012

Product data sheet

## 1. General description

The 74AHC126-Q100; 74AHCT126-Q100 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHC126-Q100; 74AHCT126-Q100 provides four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs ( $nY$ ) are controlled by the output enable input ( $nOE$ ). A LOW-level at pin  $nOE$  causes the outputs to assume a high-impedance OFF-state.

The 74AHC126-Q100; 74AHCT126-Q100 is identical to the 74AHC125-Q100; 74AHCT125-Q100 but has active HIGH output enable inputs.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Balanced propagation delays
- All inputs have Schmitt trigger action
- Inputs accept voltages higher than  $V_{CC}$
- Input levels:
  - ◆ For 74AHC126-Q100: CMOS level
  - ◆ For 74AHCT126-Q100: TTL level
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200 \text{ pf}$ ,  $R = 0 \Omega$ )
- Multiple package options



### 3. Ordering information

Table 1. Ordering information

Type number	Package		Description	Version
	Temperature range	Name		
74AHC126D-Q100	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCT126D-Q100				
74AHC126PW-Q100	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCT126PW-Q100				
74AHC126BQ-Q100	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74AHCT126BQ-Q100				

### 4. Functional diagram

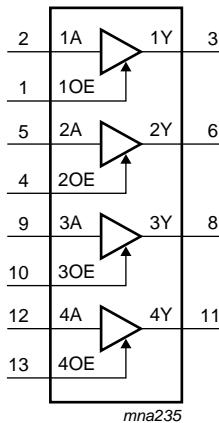


Fig 1. Functional diagram

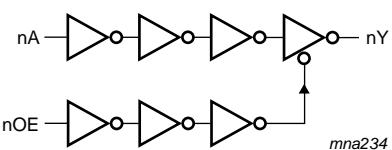


Fig 2. Logic symbol

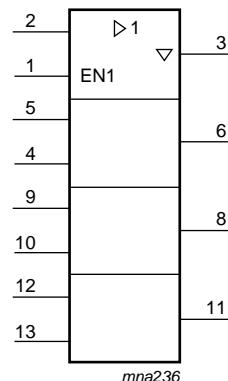


Fig 3. IEC logic symbol

## 5. Pinning information

### 5.1 Pinning

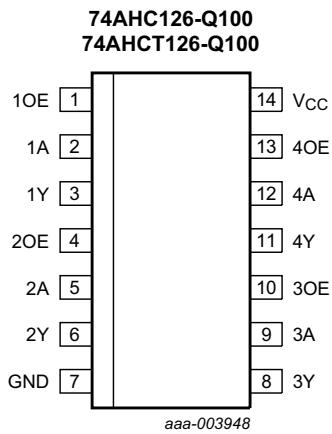


Fig 4. Pin configuration SO14 and TSSOP14

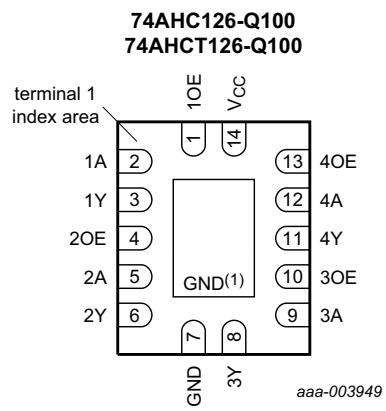


Fig 5. Pin configuration DHVQFN14

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE	1	output enable input 1 (active HIGH)
1A	2	data input 1
1Y	3	data output 1
2OE	4	output enable input 2 (active HIGH)
2A	5	data input 2
2Y	6	data output 2
GND	7	ground (0 V)
3Y	8	data output 3
3A	9	data input 3
3OE	10	output enable input 3 (active HIGH)
4Y	11	data output 4
4A	12	data input 4
4OE	13	output enable input 4 (active HIGH)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3. Function table<sup>[1]</sup>**

Control	Input	Output
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

[1] H = HIGH voltage state;

L = LOW voltage state;

X = don't care;

Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	[1] -20	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	[1] -20	+20	mA
I <sub>O</sub>	output current	V <sub>O</sub> = -0.5 V to (V <sub>CC</sub> + 0.5 V)	-25	+25	mA
I <sub>CC</sub>	supply current		-	+75	mA
I <sub>GND</sub>	ground current		-75	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 packages: above 70 °C the value of P<sub>tot</sub> derates linearly at 8 mW/K.

For TSSOP14 packages: above 60 °C the value of P<sub>tot</sub> derates linearly at 5.5 mW/K.

For DHVQFN14 packages: above 60 °C the value of P<sub>tot</sub> derates linearly at 4.5 mW/K.

## 8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>74AHC126-Q100</b>						
$V_{CC}$	supply voltage		2.0	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	20	ns/V
<b>74AHCT126-Q100</b>						
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	20	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC126-Q100</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0 \text{ V}$	1.5	-	-	1.5	-	1.5	-	V
		$V_{CC} = 3.0 \text{ V}$	2.1	-	-	2.1	-	2.1	-	V
		$V_{CC} = 5.5 \text{ V}$	3.85	-	-	3.85	-	3.85	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0 \text{ V}$	-	-	0.5	-	0.5	-	0.5	V
		$V_{CC} = 3.0 \text{ V}$	-	-	0.9	-	0.9	-	0.9	V
		$V_{CC} = 5.5 \text{ V}$	-	-	1.65	-	1.65	-	1.65	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -50 \mu\text{A}; V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50 \mu\text{A}; V_{CC} = 3.0 \text{ V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
		$I_O = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.80	-	3.70	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 50 \mu\text{A}; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu\text{A}; V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.25	-	±2.5	-	±10.0	μA
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μA
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
$C_O$	output capacitance		-	4	-	-	-	-	-	pF

## 74AHCT126-Q100

$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	$I_O = -50 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	4.4	V
	$I_O = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	3.70	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	$I_O = 50 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	-	V
	$I_O = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	-	V
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND per input pin; other inputs at $V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	±0.25	-	±2.5	-	±10.0	μA
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μA
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; other pins at $V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
$C_O$	output capacitance		-	4	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
<b>74AHC126-Q100</b>										
$t_{pd}$	propagation delay	nA to nY; see <a href="#">Figure 6</a> <sup>[2]</sup> $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	4.7	8.0	1.0	9.5	1.0	10.0	ns
		$C_L = 50 \text{ pF}$	-	6.7	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	3.3	5.5	1.0	6.5	1.0	7.0	ns
		$C_L = 50 \text{ pF}$	-	4.7	7.5	1.0	8.5	1.0	9.5	ns
$t_{en}$	enable time	nOE to nY; see <a href="#">Figure 7</a> <sup>[3]</sup> $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	5.3	8.0	1.0	9.5	1.0	10.0	ns
		$C_L = 50 \text{ pF}$	-	7.6	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	3.6	5.3	1.0	6.1	1.0	7.0	ns
		$C_L = 50 \text{ pF}$	-	5.1	7.6	1.0	8.7	1.0	9.5	ns
$t_{dis}$	disable time	nOE to nY; see <a href="#">Figure 7</a> <sup>[4]</sup> $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	6.6	9.7	1.0	11.5	1.0	12.5	ns
		$C_L = 50 \text{ pF}$	-	9.4	13.2	1.0	15.0	1.0	16.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	4.7	6.8	1.0	8.0	1.0	8.5	ns
		$C_L = 50 \text{ pF}$	-	6.7	8.8	1.0	10.0	1.0	11.0	ns
$C_{PD}$	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$ <sup>[5]</sup>	-	10	-	-	-	-	-	pF
<b>74AHCT126-Q100; <math>V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}</math></b>										
$t_{pd}$	propagation delay	nA to nY; see <a href="#">Figure 6</a> <sup>[2]</sup> $C_L = 15 \text{ pF}$	-	3.0	5.5	1.0	6.5	1.0	7.0	ns
		$C_L = 50 \text{ pF}$	-	4.3	7.5	1.0	8.5	1.0	9.5	ns
$t_{en}$	enable time	nOE to nY; see <a href="#">Figure 7</a> <sup>[3]</sup> $C_L = 15 \text{ pF}$	-	3.3	5.1	1.0	6.0	1.0	6.5	ns
		$C_L = 50 \text{ pF}$	-	4.7	7.1	1.0	8.0	1.0	9.0	ns
$t_{dis}$	disable time	nOE to nY; see <a href="#">Figure 7</a> <sup>[4]</sup> $C_L = 15 \text{ pF}$	-	4.8	6.8	1.0	8.0	1.0	8.5	ns
		$C_L = 50 \text{ pF}$	-	6.9	8.9	1.0	10.0	1.0	11.5	ns
$C_{PD}$	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$ <sup>[5]</sup>	-	12	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3$  V and  $V_{CC} = 5.0$  V).

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

[4]  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

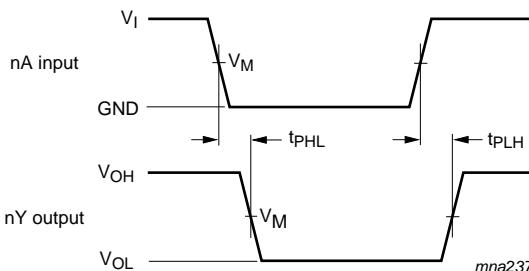
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

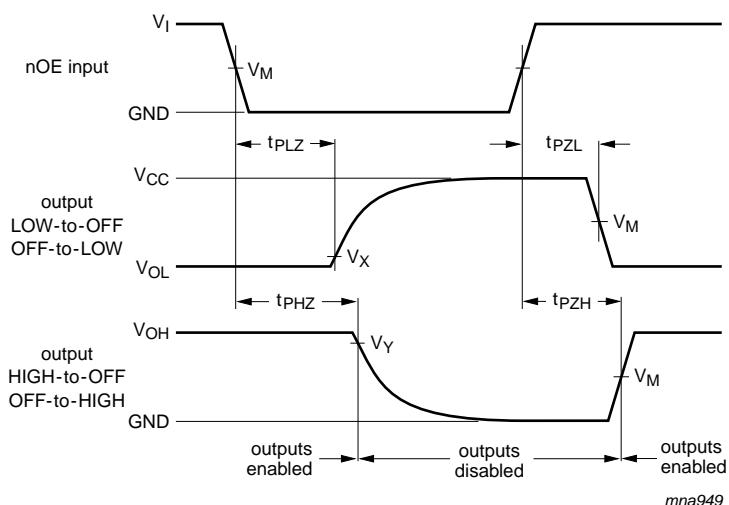
## 11. Waveforms



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. Input to output propagation delays**



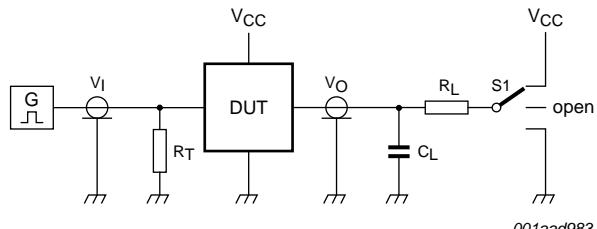
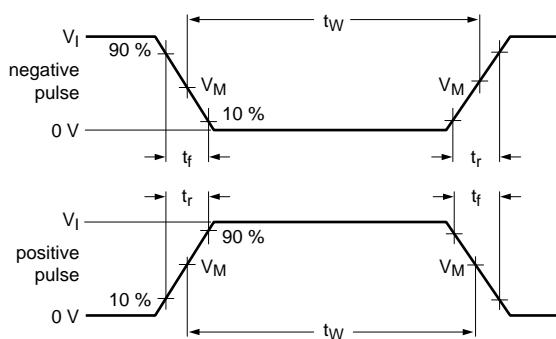
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Enable and disable times**

Table 8. Measurement points

Type	Input		Output	
	$V_M$	$V_M$	$V_X$	$V_Y$
74AHC126-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
74AHCT126-Q100	1.5 V	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

$R_L$  = load resistance.

$S1$  = test selection switch.

Fig 8. Test circuitry for measuring switching times

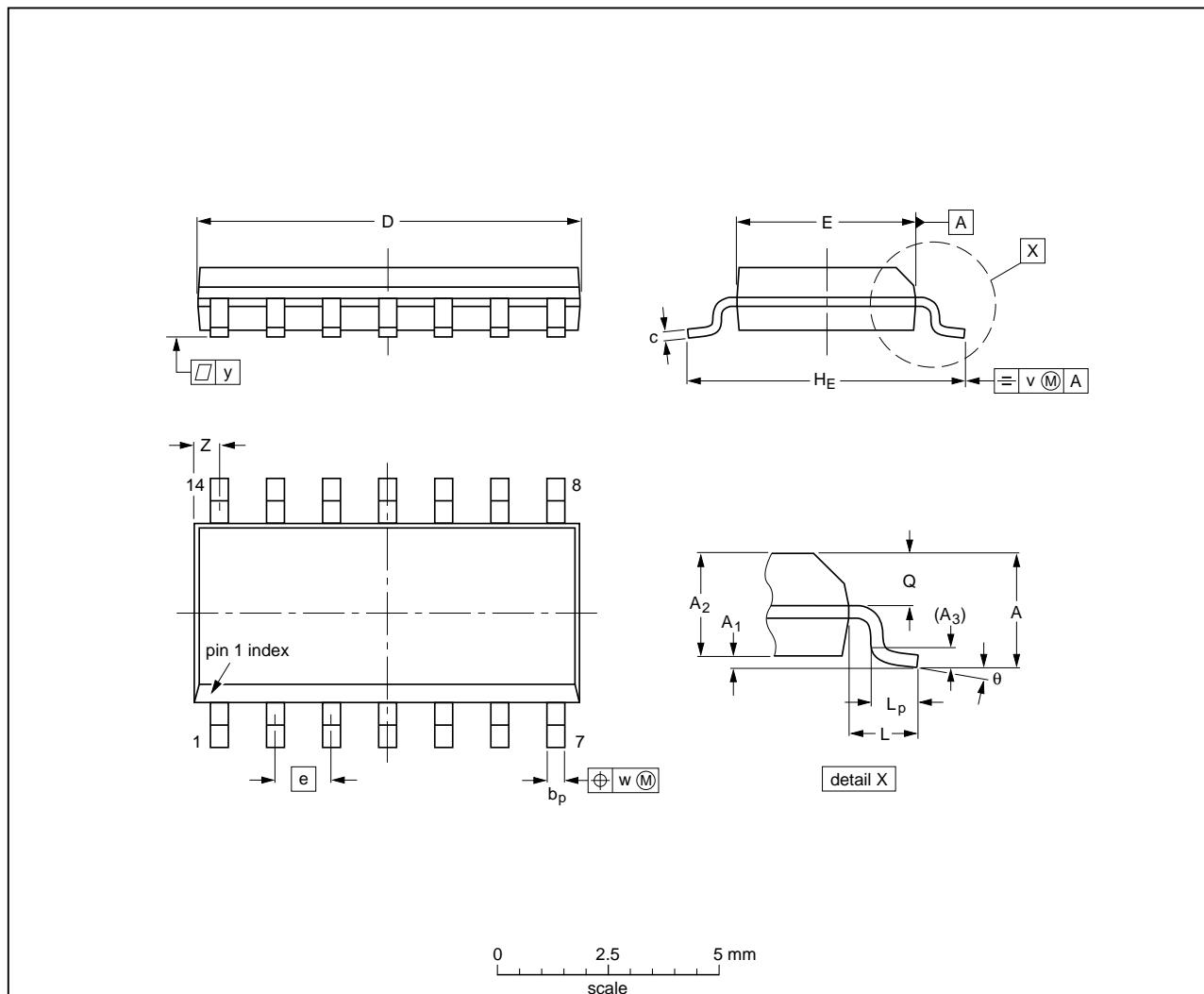
Table 9. Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74AHC126-Q100	$V_{CC}$	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74AHCT126-Q100	3.0 V	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

## 12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



## DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25	1.45	0.25	0.49	0.25	8.75	4.0	1.27	6.2	1.05	1.0	0.7	0.25	0.25	0.1	0.7	8°
inches	0.069	0.010	0.057	0.01	0.019	0.0100	0.35	3.8	0.16	5.8	0.4	0.4	0.6	0.025	0.025	0.012	0.3	0°

## Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

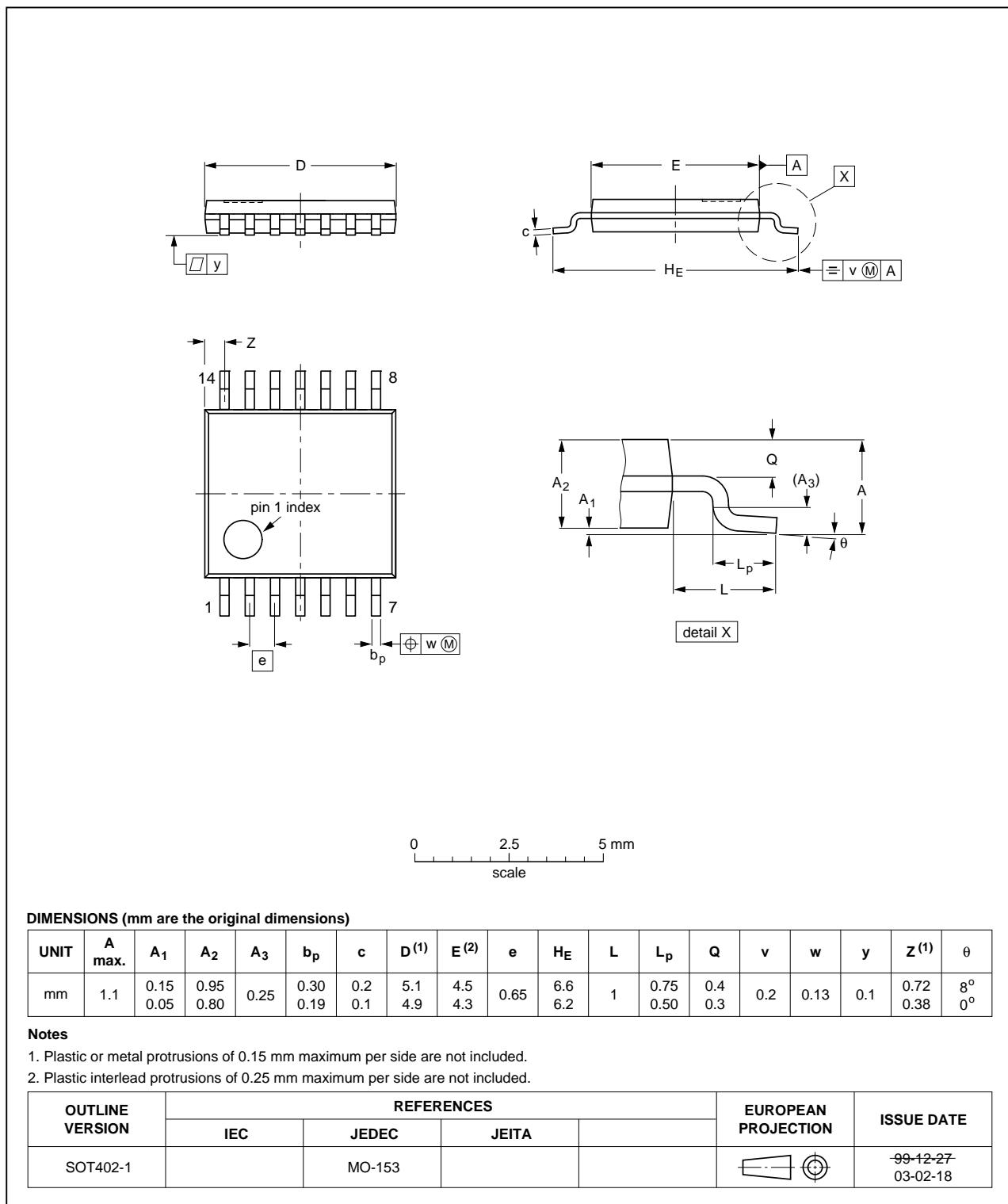


Fig 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

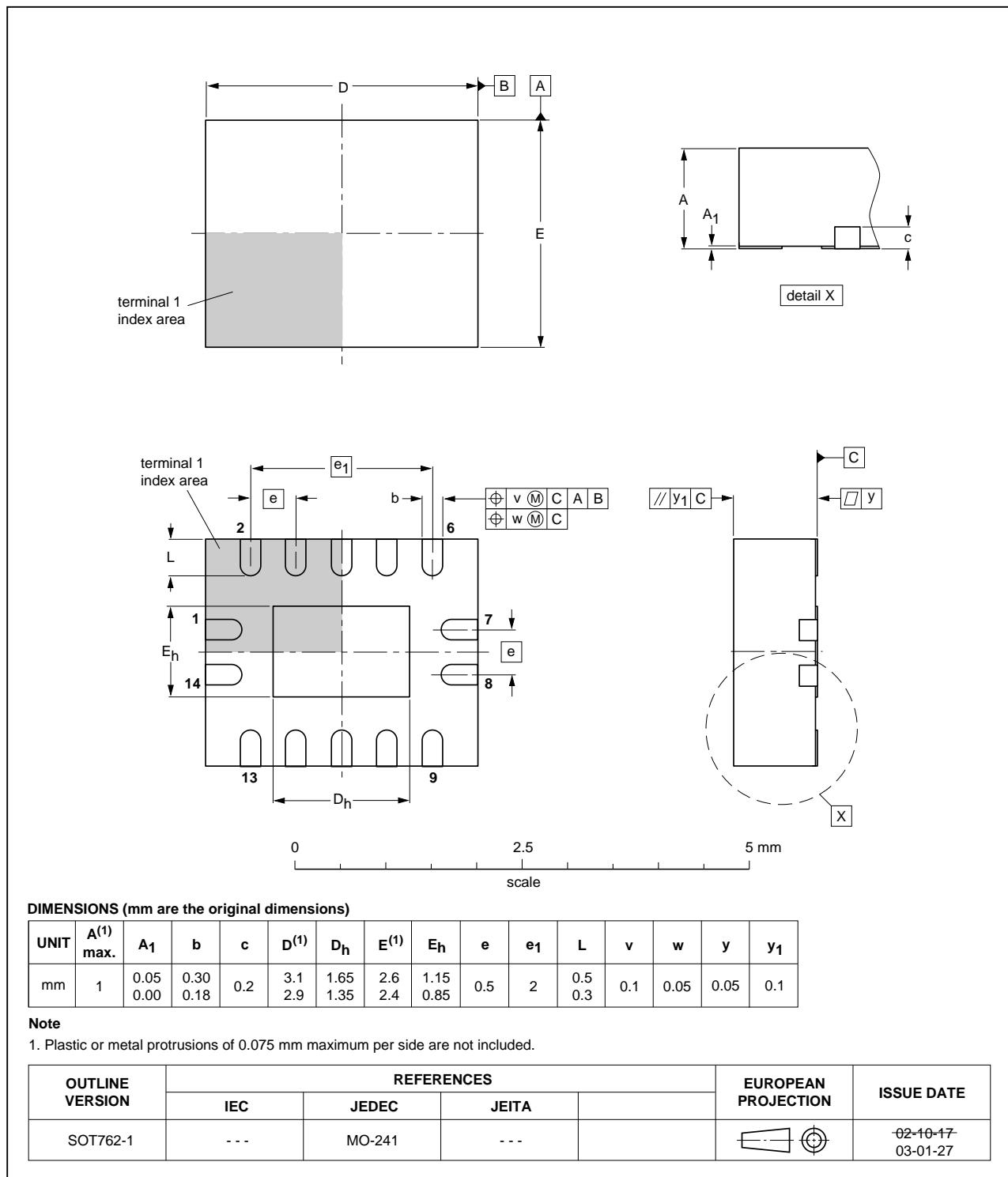


Fig 11. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
MIL	Military

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT126_Q100 v.1	20120710	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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