

# 74AHC259-Q100; 74AHCT259-Q100

8-bit addressable latch

Rev. 1 — 22 July 2013

Product data sheet

## 1. General description

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The 74AHC259-Q100; 74AHCT259-Q100 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC259-Q100; 74AHCT259-Q100 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single-line data in eight addressable latches. It provides a 3-to-8 decoder and multiplexer function with active HIGH outputs (Q0 to Q7). It also incorporates an active LOW common reset ( $\overline{MR}$ ) for resetting all latches as well as an active LOW enable input ( $\overline{LE}$ ).

The 74AHC259-Q100; 74AHCT259-Q100 has four modes of operation:

- In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states.
- In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.
- In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the data input (D) with all other outputs in the LOW state.
- In the reset mode, all outputs are LOW and unaffected by the address inputs (A0 to A2) and data input (D).

When operating the 74AHC259-Q100; 74AHCT259-Q100 as an address latch, changing more than 1 bit of the address could impose a transient-wrong address. Therefore, only change more than 1 bit while in the memory mode.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

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- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ °C}$  to  $+85\text{ °C}$  and from  $-40\text{ °C}$  to  $+125\text{ °C}$
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability



- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Inputs accept voltages higher than  $V_{CC}$
- Input levels:
  - ◆ For 74AHC259-Q100: CMOS level
  - ◆ For 74AHCT259-Q100: TTL level
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0  $\Omega$ )
- Multiple package options

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<b>74AHC259-Q100</b>				
74AHC259D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC259PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
<b>74AHCT259-Q100</b>				
74AHCT259D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHCT259PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

### 4. Functional diagram

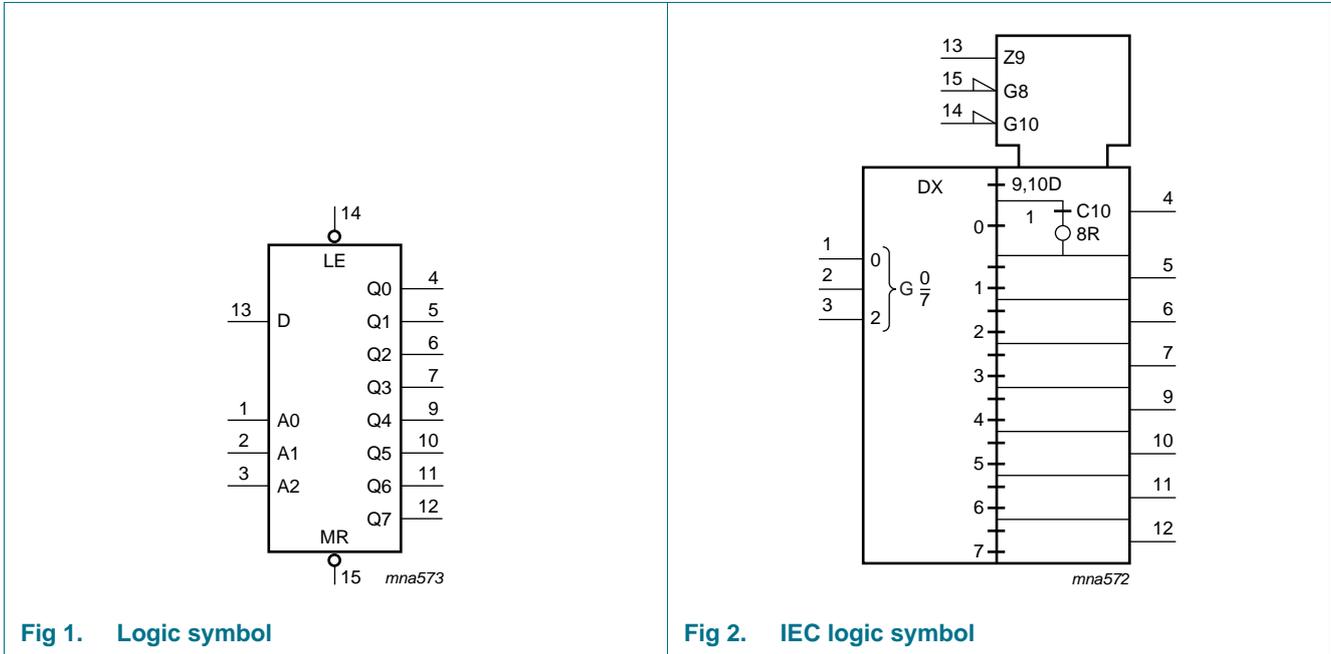


Fig 1. Logic symbol

Fig 2. IEC logic symbol

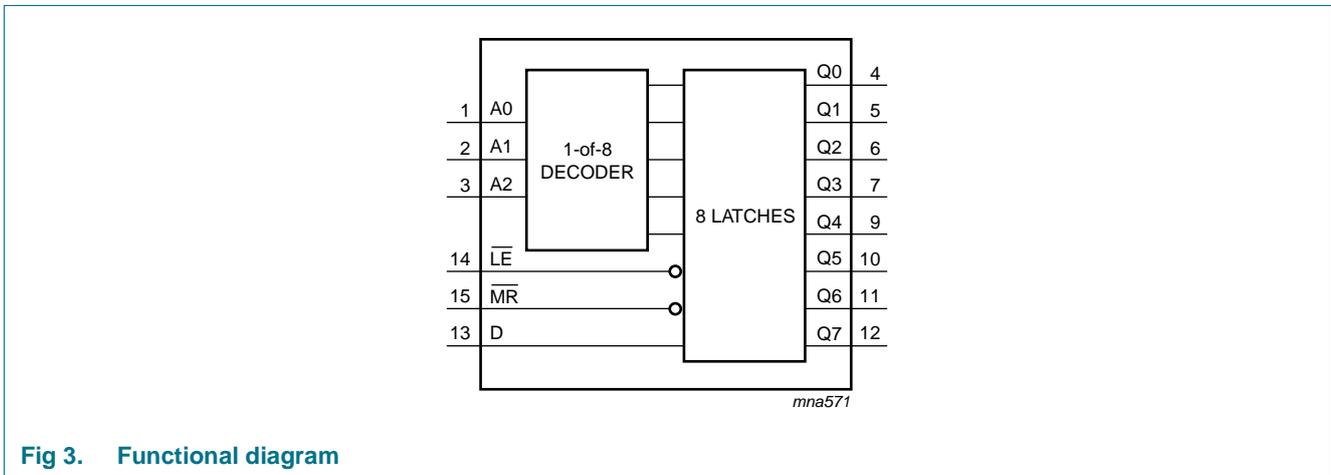


Fig 3. Functional diagram

## 5. Pinning information

### 5.1 Pinning

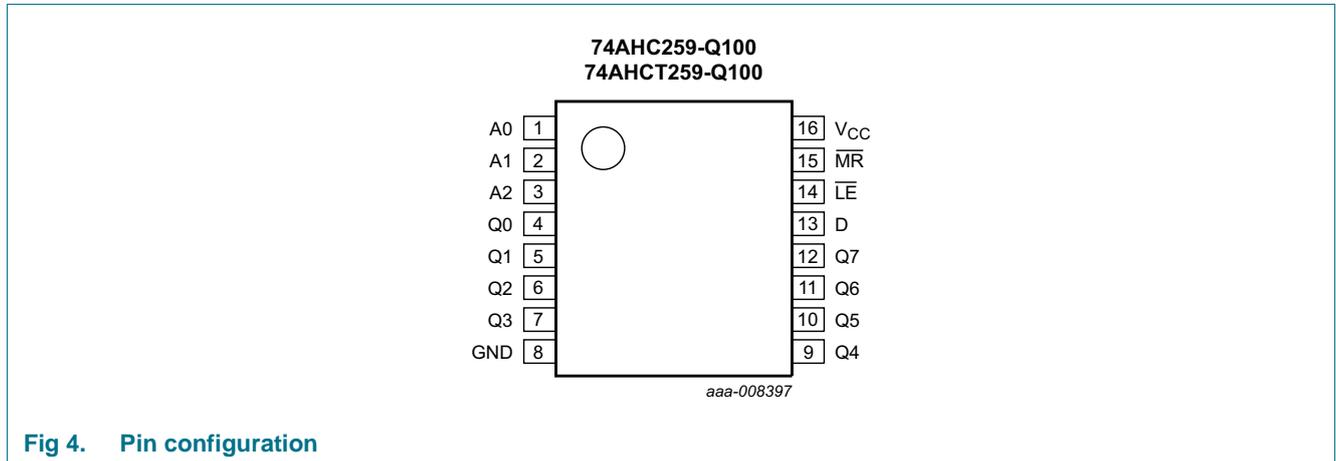


Fig 4. Pin configuration

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0	1	address input
A1	2	address input
A2	3	address input
Q0	4	latch output
Q1	5	latch output
Q2	6	latch output
Q3	7	latch output
GND	8	ground (0 V)
Q4	9	latch output
Q5	10	latch output
Q6	11	latch output
Q7	12	latch output
D	13	data input
$\overline{\text{LE}}$	14	latch enable input (active LOW)
$\overline{\text{MR}}$	15	conditional reset input (active LOW)
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating mode	Input						Output							
	MR	LE	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Reset (clear)	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplexer (active HIGH 8-channel) decoder (when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
			d	H	L	L	L	Q = d	L	L	L	L	L	L
			d	L	H	L	L	L	Q = d	L	L	L	L	L
			d	H	H	L	L	L	L	Q = d	L	L	L	L
			d	L	L	H	L	L	L	L	Q = d	L	L	L
			d	H	L	H	L	L	L	L	L	Q = d	L	L
			d	L	H	H	L	L	L	L	L	L	Q = d	L
			d	H	H	H	L	L	L	L	L	L	L	L
Memory (no action)	H	H	X	X	X	X	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
Addressable latch	H	L	d	L	L	L	Q = d	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
			d	H	L	L	q <sub>0</sub>	Q = d	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
			d	L	H	L	q <sub>0</sub>	q <sub>1</sub>	Q = d	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
			d	H	H	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	Q = d	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
			d	L	L	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	Q = d	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
			d	H	L	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	Q = d	q <sub>6</sub>	q <sub>7</sub>
			d	L	H	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	Q = d	q <sub>7</sub>
			H	H	H	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	Q = d

[1] H = HIGH voltage level;

L = LOW voltage level;

X = don't care;

d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH LE transition;

q = lower case letter indicates the state of the referenced input one set-up time prior to the LOW-to-HIGH transition.

Table 4. Operating mode select table<sup>[1]</sup>

LE	MR	Mode
L	H	addressable latch
H	H	memory
L	L	active HIGH 8-channel demultiplexer
H	L	reset

[1] H = HIGH voltage level; L = LOW voltage level.

## 7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	<sup>[1]</sup> -20	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	<sup>[1]</sup> -20	+20	mA
I <sub>O</sub>	output current	V <sub>O</sub> = -0.5 V to (V <sub>CC</sub> + 0.5 V)	-25	+25	mA
I <sub>CC</sub>	supply current		-	+75	mA
I <sub>GND</sub>	ground current		-75	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	<sup>[2]</sup> -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 packages: above 70 °C the value of P<sub>tot</sub> derates linearly at 8 mW/K.  
For TSSOP16 packages: above 60 °C the value of P<sub>tot</sub> derates linearly at 5.5 mW/K.

## 8. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>74AHC259-Q100</b>						
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	100	ns/V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	20	ns/V
<b>74AHCT259-Q100</b>						
V <sub>CC</sub>	supply voltage		4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	20	ns/V

## 9. Static characteristics

**Table 7. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC259-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
	I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.80	-	3.70	-	V	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
	I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V	
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	µA
C <sub>I</sub>	input capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND	-	3	10	-	10	-	10	pF
C <sub>O</sub>	output capacitance		-	4	-	-	-	-	-	pF
<b>74AHCT259-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V

**Table 7. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other pins at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND	-	3	10	-	10	-	10	pF
C <sub>O</sub>	output capacitance		-	4	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 11](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max		
<b>74AHC259-Q100</b>											
t <sub>pd</sub>	propagation delay	D to Qn; see <a href="#">Figure 5</a>									[2]
		V <sub>CC</sub> = 3.0 V to 3.6 V									
		C <sub>L</sub> = 15 pF	-	5.8	11.5	1.0	13.5	1.0	15.0	ns	
		C <sub>L</sub> = 50 pF	-	7.3	14.5	1.0	17.0	1.0	18.5	ns	
		V <sub>CC</sub> = 4.5 V to 5.5 V									
		C <sub>L</sub> = 15 pF	-	4.1	7.5	1.0	9.0	1.0	10.0	ns	
		C <sub>L</sub> = 50 pF	-	5.3	9.5	1.0	11.0	1.0	12.0	ns	
		An to Qn; see <a href="#">Figure 6</a>									[2]
		V <sub>CC</sub> = 3.0 V to 3.6 V									
		C <sub>L</sub> = 15 pF	-	7.5	14.5	1.0	17.0	1.0	18.5	ns	
		C <sub>L</sub> = 50 pF	-	9.1	18.0	1.0	21.0	1.0	23.0	ns	
		V <sub>CC</sub> = 4.5 V to 5.5 V									
		C <sub>L</sub> = 15 pF	-	5.3	9.5	1.0	11.5	1.0	12.5	ns	
		C <sub>L</sub> = 50 pF	-	6.5	11.5	1.0	13.5	1.0	15.0	ns	
LE to Qn; see <a href="#">Figure 7</a>									[2]		
V <sub>CC</sub> = 3.0 V to 3.6 V											
C <sub>L</sub> = 15 pF	-	6.2	12.0	1.0	14.0	1.0	15.2	ns			
C <sub>L</sub> = 50 pF	-	7.7	15.5	1.0	17.5	1.0	19.0	ns			
V <sub>CC</sub> = 4.5 V to 5.5 V											
C <sub>L</sub> = 15 pF	-	4.3	8.0	1.0	9.5	1.0	10.5	ns			
C <sub>L</sub> = 50 pF	-	5.5	10.0	1.0	11.5	1.0	12.5	ns			

**Table 8. Dynamic characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 11](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
t <sub>pd</sub>	propagation delay	$\overline{MR}$ to Qn; see <a href="#">Figure 8</a> <sup>[3]</sup> V <sub>CC</sub> = 3.0 V to 3.6 V								
		C <sub>L</sub> = 15 pF	-	5.4	10.5	1.0	12.5	1.0	13.5	ns
		C <sub>L</sub> = 50 pF	-	7.0	13.5	1.0	15.5	1.0	17.0	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	3.9	7.0	1.0	8.5	1.0	9.5	ns
		C <sub>L</sub> = 50 pF	-	5.1	9.0	1.0	10.5	1.0	11.5	ns
t <sub>w</sub>	pulse width	$\overline{LE}$ HIGH or LOW; see <a href="#">Figure 7</a> V <sub>CC</sub> = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		$\overline{MR}$ LOW; see <a href="#">Figure 8</a> V <sub>CC</sub> = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		t <sub>su</sub>	set-up time	D, An to $\overline{LE}$ ; see <a href="#">Figure 9</a> and <a href="#">Figure 10</a> V <sub>CC</sub> = 3.0 V to 3.6 V	4.0	-	-	4.0	-	4.0
		V <sub>CC</sub> = 4.5 V to 5.5 V	4.0	-	-	4.0	-	4.0	-	ns
t <sub>h</sub>	hold time	D, An to $\overline{LE}$ ; see <a href="#">Figure 9</a> and <a href="#">Figure 10</a> V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	-	-	1.0	-	1.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.0	-	-	1.0	-	1.0	-	ns
		C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[4]</sup>	-	13	-	-	-	-

**74AHCT259-Q100; V<sub>CC</sub> = 4.5 V to 5.5 V**

t <sub>pd</sub>	propagation delay	D to Qn; see <a href="#">Figure 5</a> <sup>[2]</sup> C <sub>L</sub> = 15 pF	-	4.1	7.5	1.0	9.0	1.0	10.0	ns		
		C <sub>L</sub> = 50 pF	-	5.4	9.5	1.0	11.0	1.0	12.0	ns		
		An to Qn; see <a href="#">Figure 6</a> <sup>[2]</sup> C <sub>L</sub> = 15 pF	-	5.5	9.5	1.0	11.5	1.0	12.5	ns		
		C <sub>L</sub> = 50 pF	-	6.6	12.0	1.0	14.0	1.0	15.5	ns		
		$\overline{LE}$ to Qn; see <a href="#">Figure 7</a> <sup>[2]</sup> C <sub>L</sub> = 15 pF	-	4.3	8.0	1.0	9.5	1.0	10.4	ns		
		C <sub>L</sub> = 50 pF	-	5.5	10.0	1.0	12.0	1.0	13.0	ns		
		$\overline{MR}$ to Qn; see <a href="#">Figure 8</a> <sup>[3]</sup> C <sub>L</sub> = 15 pF	-	3.9	7.0	1.0	8.5	1.0	9.5	ns		
		C <sub>L</sub> = 50 pF	-	5.1	9.0	1.0	10.5	1.0	11.5	ns		
		t <sub>w</sub>	pulse width	$\overline{LE}$ HIGH or LOW; see <a href="#">Figure 7</a> V <sub>CC</sub> = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
				$\overline{MR}$ LOW; see <a href="#">Figure 8</a> V <sub>CC</sub> = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns

**Table 8. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 11](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
t <sub>su</sub>	set-up time	D, An to $\overline{LE}$ ; see <a href="#">Figure 9</a> and <a href="#">Figure 10</a>	4.0	-	-	4.0	-	4.0	-	ns
t <sub>h</sub>	hold time	D, An to $\overline{LE}$ ; see <a href="#">Figure 9</a> and <a href="#">Figure 10</a>	1.0	-	-	1.0	-	1.0	-	ns
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[4]</sup>	-	17	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V and V<sub>CC</sub> = 5.0 V).

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] t<sub>pd</sub> is the same as t<sub>PHL</sub> only.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

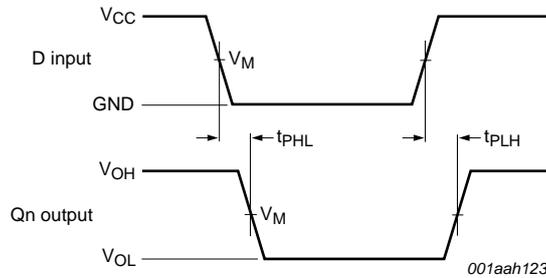
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

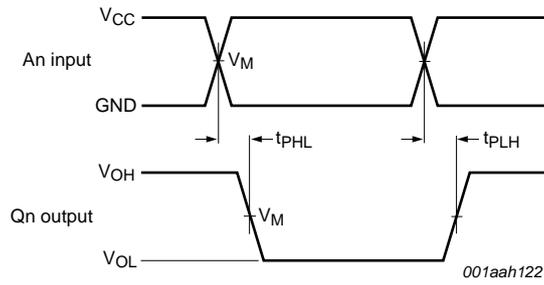
## 11. Waveforms



Measurement points are given in [Table 9](#).

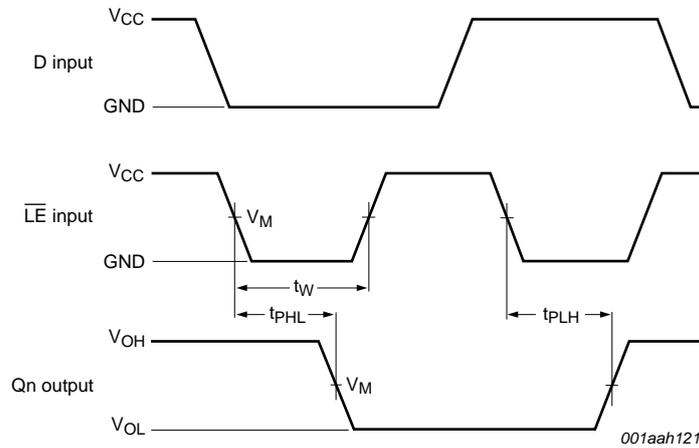
V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

**Fig 5. Data input to output propagation delays**



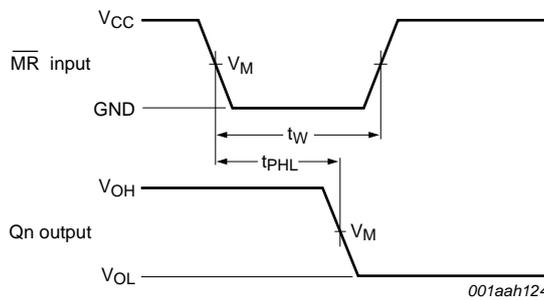
Measurement points are given in [Table 9](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. Address input to output propagation delays**



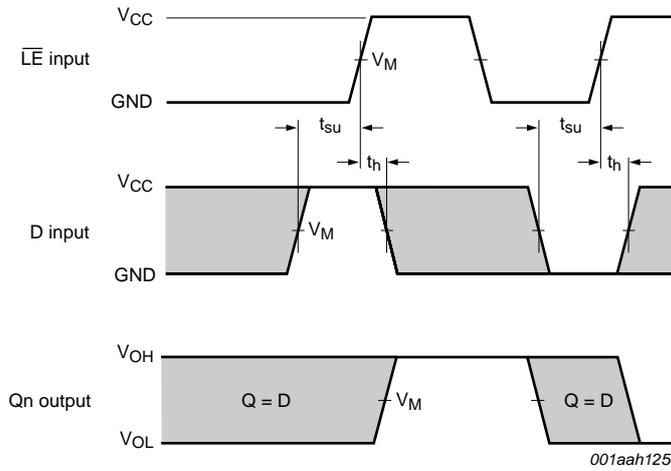
Measurement points are given in [Table 9](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Enable input to output propagation delays and pulse width**



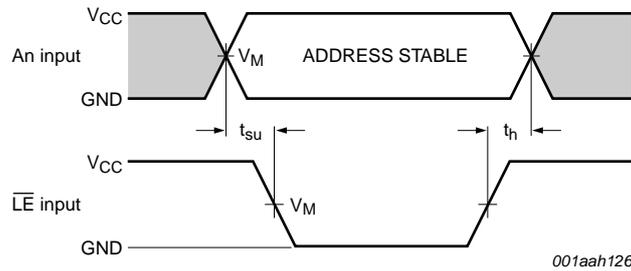
Measurement points are given in [Table 9](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 8. Conditional reset input to output propagation delays**



Measurement points are given in [Table 9](#).  
 The shaded areas indicate when the input is permitted to change for predictable output performance.  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 9. Data input to latch enable input set-up and hold times**

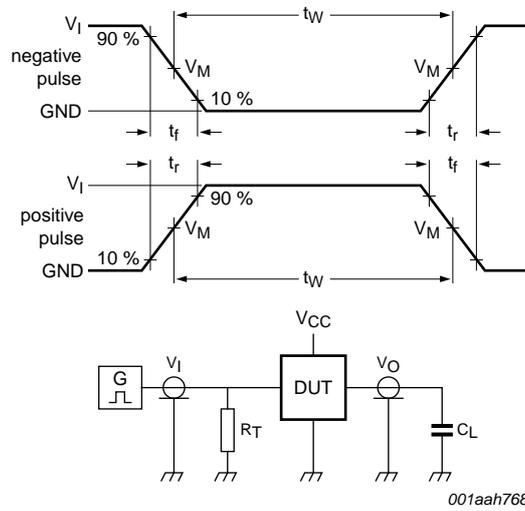


Measurement points are given in [Table 9](#).  
 The shaded areas indicate when the input is permitted to change for predictable output performance.  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 10. Address input to latch enable input set-up and hold times**

**Table 9. Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74AHC259-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT259-Q100	1.5 V	$0.5 \times V_{CC}$



001aah768

Test data is given in [Table 10](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

**Fig 11. Load circuitry for measuring switching times**

**Table 10. Test data**

Type	Input		Load	Test
	$V_I$	$t_r, t_f$	$C_L$	
74AHC259-Q100	$V_{CC}$	$\leq 3.0$ ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74AHCT259-Q100	3.0 V	$\leq 3.0$ ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

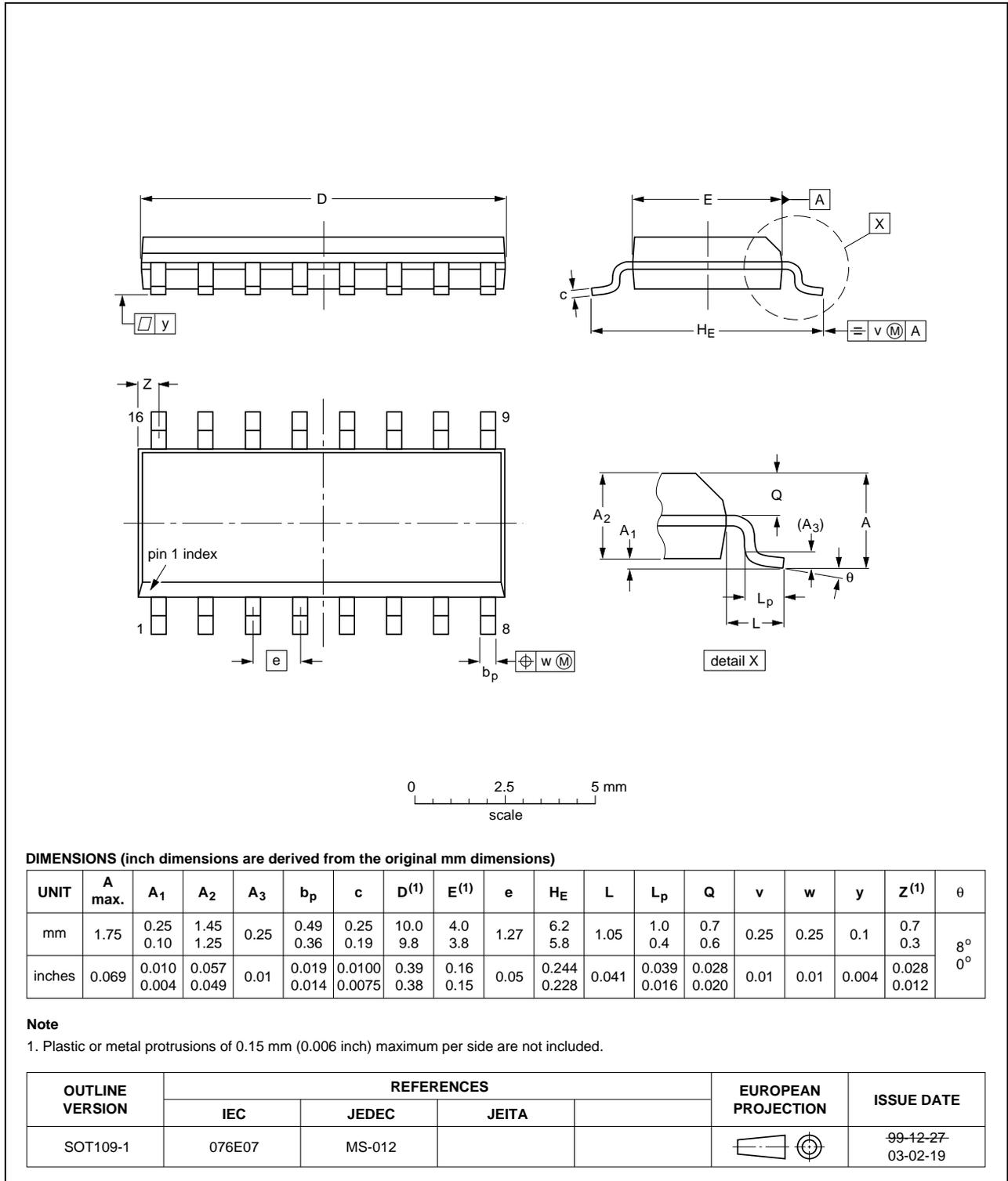


Fig 12. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

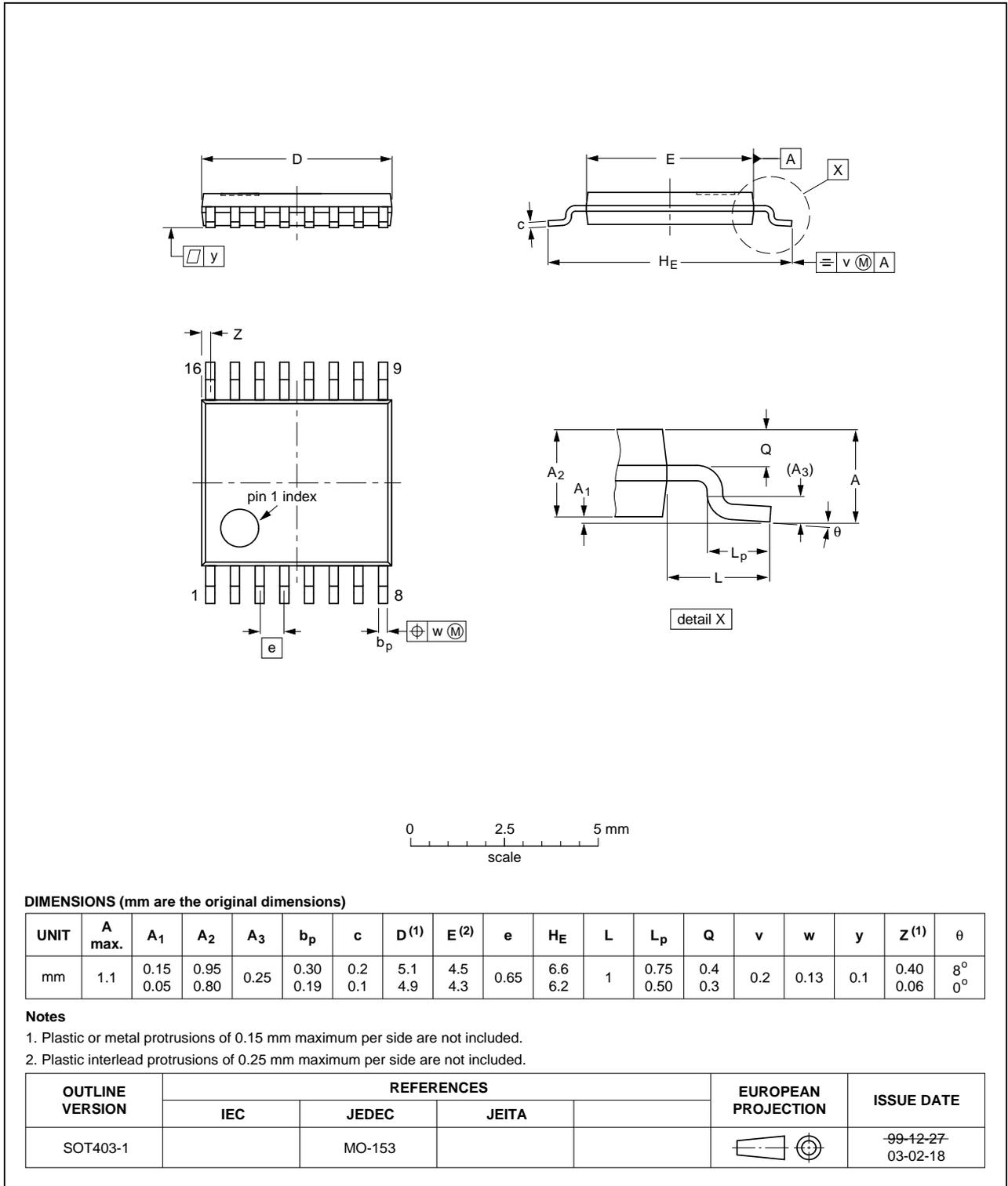


Fig 13. Package outline SOT403-1 (TSSOP16)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT259_Q100 v.1	20130722	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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