

DATA SHEET

74AHC573; 74AHCT573

Octal D-type transparent latch;
3-state

Product specification
Supersedes data of 1999 Sep 27

2003 Dec 08

Octal D-type transparent latch; 3-state

74AHC573; 74AHCT573

FEATURES

- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Common 3-state output enable input
- Functionally identical to the 74AHC/AHCT563 and 74AHC/AHCT373
- Inputs accepts voltages higher than V_{CC}
- For AHC only: operates with CMOS input levels
- For AHCT only: operates with TTL input levels
- Specified from -40 to $+85$ °C and -40 to $+125$ °C.

DESCRIPTION

The 74AHC/AHCT573 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74AHC/AHCT573 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A Latch Enable (LE) input and an Output Enable ($\overline{OE}$) input are common to all latches.

The 74AHC/AHCT573 consists of eight D-type transparent latches with 3-state true outputs. When pin LE is HIGH, data at the Dn inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When pin LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When pin $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When pin $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The 74AHC/AHCT573 is functionally identical to the 74AHC/AHCT533, 74AHC/AHCT563 and 74AHC/AHCT373, but the 74AHC/AHCT533 and 74AHC/AHCT563 have inverted outputs and the 74AHC/AHCT563 and 74AHC/AHCT373 have a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC	AHCT	
t_{PHL}/t_{PLH}	propagation delay Dn to Qn; LE to Qn	$C_L = 15$ pF; $V_{CC} = 5$ V	3.9	3.5	ns
C_I	input capacitance	$V_I = V_{CC}$ or GND	3.0	3.0	pF
C_O	output capacitance		4.0	4.0	pF
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; notes 1 and 2	12	18	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. The condition is $V_I = \text{GND to } V_{CC}$.

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FUNCTION TABLE

See note 1.

OPERATING MODE	INPUT			INTERNAL LATCH	OUTPUT
	$\overline{OE}$	LE	Dn		Q0 to Q7
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

Note

1. H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PACKAGE	MATERIAL	CODE
74AHC573D	20	SO20	plastic	SOT163-1
74AHCT573D	20	SO20	plastic	SOT163-1
74AHC573PW	20	TSSOP20	plastic	SOT360-1
74AHCT573PW	20	TSSOP20	plastic	SOT360-1

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PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2	D0	data input
3	D1	data input
4	D2	data input
5	D3	data input
6	D4	data input
7	D5	data input
8	D6	data input
9	D7	data input
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
12	Q7	3-state latch output
13	Q6	3-state latch output
14	Q5	3-state latch output
15	Q4	3-state latch output
16	Q3	3-state latch output
17	Q2	3-state latch output
18	Q1	3-state latch output
19	Q0	3-state latch output
20	V _{CC}	supply voltage

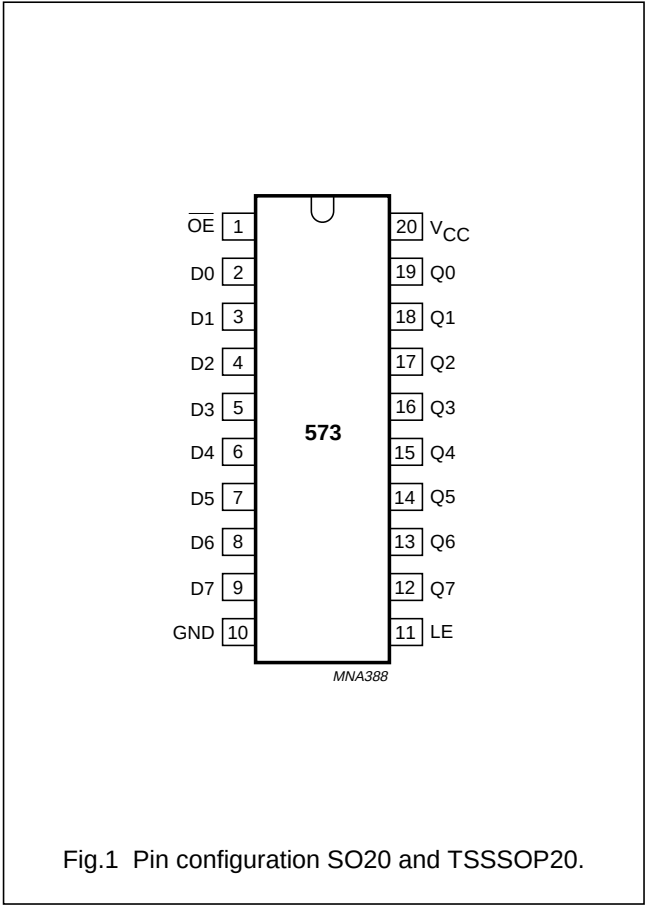


Fig.1 Pin configuration SO20 and TSSOP20.

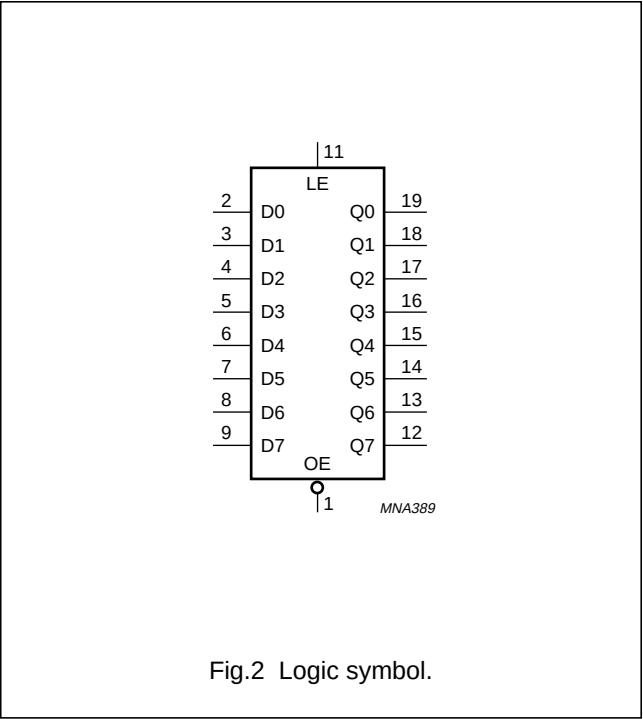


Fig.2 Logic symbol.

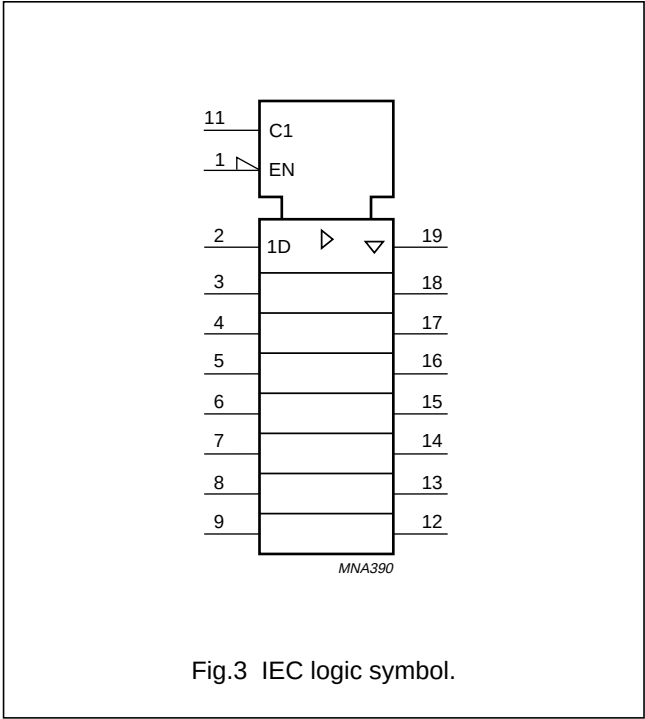


Fig.3 IEC logic symbol.

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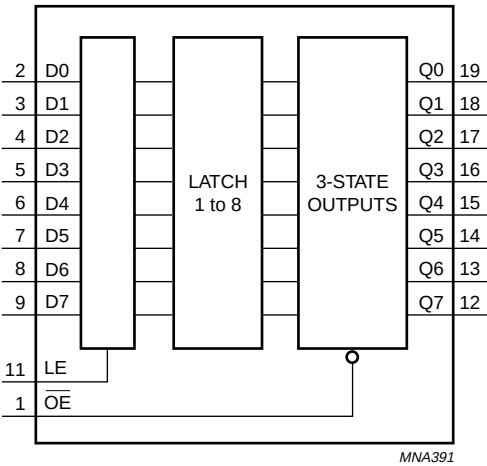


Fig.4 Functional diagram.

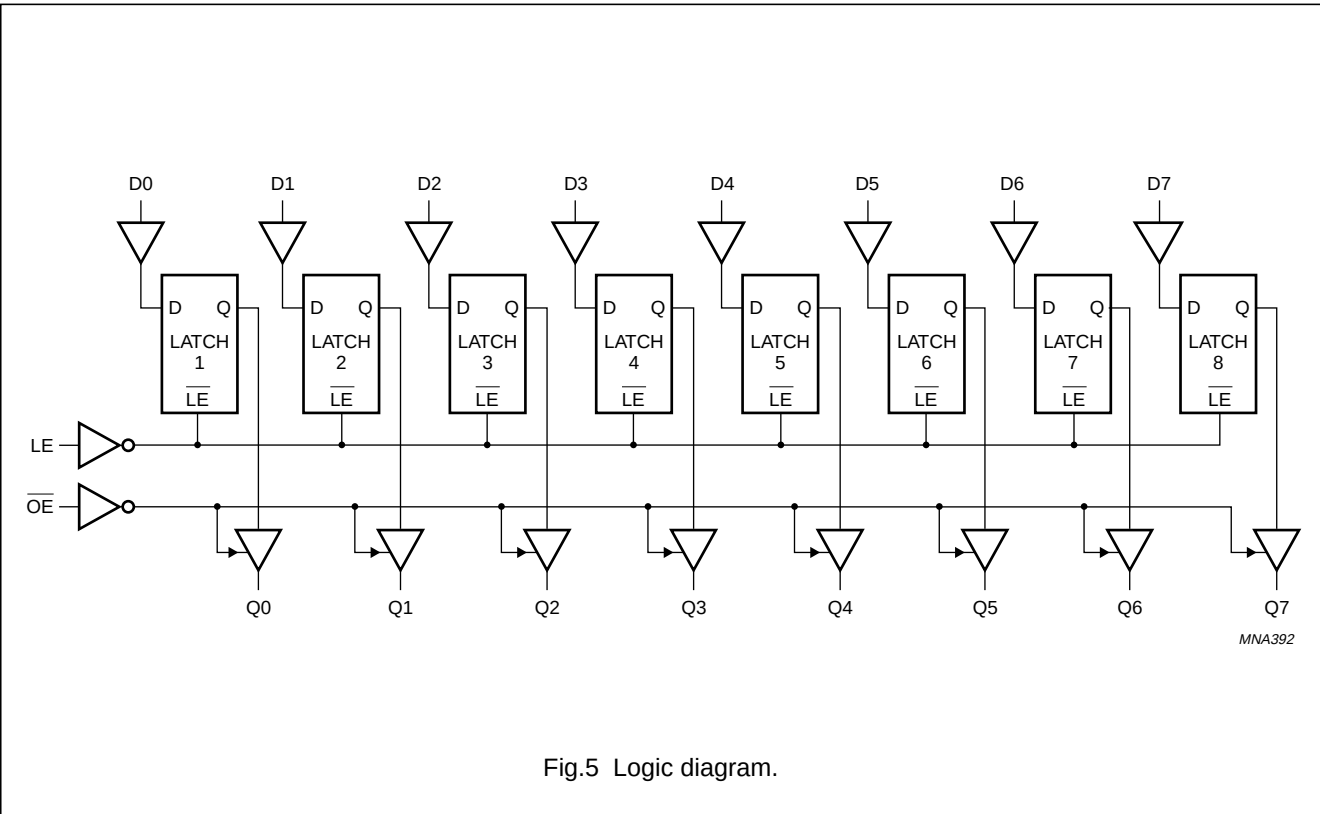


Fig.5 Logic diagram.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC			74AHCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall rates	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	–	–	100	–	–	–	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	–	–	20	–	–	20	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5 \text{ V}$; note 1	–	–20	mA
I_{OK}	output diode current	$V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$; note 1	–	± 20	mA
I_O	output source or sink current	$-0.5 \text{ V} < V_O < V_{CC} + 0.5 \text{ V}$	–	± 25	mA
I_{CC}	V_{CC} or GND current		–	± 75	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	$T_{amb} = -40 \text{ to } +125 \text{ °C}$; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO20 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For TSSOP20 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

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DC CHARACTERISTICS

74AHC type

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = 25 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = –50 μA I _O = –50 μA I _O = –50 μA I _O = –4.0 mA I _O = –8.0 mA					
			2.0	1.9	2.0	–	V
			3.0	2.9	3.0	–	V
			4.5	4.4	4.5	–	V
			3.0	2.58	–	–	V
			4.5	3.94	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 50 μA I _O = 50 μA I _O = 50 μA I _O = 4.0 mA I _O = 8.0 mA					
			2.0	–	0	0.1	V
			3.0	–	0	0.1	V
			4.5	–	0	0.1	V
			3.0	–	–	0.36	V
			4.5	–	–	0.36	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	0.1	μA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	5.5	–	–	±0.25	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	4.0	μA
C _I	input capacitance		–	–	3	10	pF

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +85 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = −50 μA I _O = −50 μA I _O = −50 μA I _O = −4.0 mA I _O = −8.0 mA	2.0	1.9	–	–	V
			3.0	2.9	–	–	V
			4.5	4.4	–	–	V
			3.0	2.48	–	–	V
			4.5	3.8	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 50 μA I _O = 50 μA I _O = 50 μA I _O = 4.0 mA I _O = 8.0 mA	2.0	–	–	0.1	V
			3.0	–	–	0.1	V
			4.5	–	–	0.1	V
			3.0	–	–	0.44	V
			4.5	–	–	0.44	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	1.0	μA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	5.5	–	–	±2.5	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	40	μA
C _I	input capacitance		–	–	–	10	pF

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +125 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = −50 μA I _O = −50 μA I _O = −50 μA I _O = −4.0 mA I _O = −8.0 mA	2.0	1.9	1.9	–	V
			3.0	2.9	2.9	–	V
			4.5	4.4	4.4	–	V
			3.0	2.48	2.48	–	V
			4.5	3.8	3.8	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 50 μA I _O = 50 μA I _O = 50 μA I _O = 4.0 mA I _O = 8.0 mA	2.0	–	–	–	V
			3.0	–	–	0.1	V
			4.5	–	–	0.1	V
			3.0	–	–	0.1	V
			4.5	–	–	0.44	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	2.0	μA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	5.5	–	–	±10.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	80	μA
C _I	input capacitance		–	–	–	10	pF

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74AHCT type

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = 25 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = –50 μA	4.5	4.4	4.5	–	V
		I _O = –8.0 mA	4.5	3.94	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 50 μA	4.5	–	0	0.1	V
		I _O = 8.0 mA	4.5	–	–	0.36	V
I _{LI}	input leakage current	V _I = V _{IH} or V _{IL}	5.5	–	–	0.1	μA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND per input pin; other inputs at V _{CC} or GND; I _O = 0	5.5	–	–	±0.25	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	4.0	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} – 2.1 V; other inputs at V _{CC} or GND; I _O = 0	4.5 to 5.5	–	–	1.35	mA
C _I	input capacitance		–	–	3	10	pF
T _{amb} = –40 to +85 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = –50 μA	4.5	4.4	–	–	V
		I _O = –8.0 mA	4.5	3.8	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 50 μA	4.5	–	–	0.1	V
		I _O = 8.0 mA	4.5	–	–	0.44	V
I _{LI}	input leakage current	V _I = V _{IH} or V _{IL}	5.5	–	–	1.0	μA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND per input pin; other inputs at V _{CC} or GND; I _O = 0	5.5	–	–	±2.5	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	40	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} – 2.1 V; other inputs at V _{CC} or GND; I _O = 0	4.5 to 5.5	–	–	1.5	mA
C _I	input capacitance		–	–	–	10	pF

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +125 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = −50 μA	4.5	4.4	–	–	V
		I _O = −8.0 mA	4.5	3.70	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 50 μA	4.5	–	–	0.1	V
		I _O = 8.0 mA	4.5	–	–	0.55	V
I _{LI}	input leakage current	V _I = V _{IH} or V _{IL}	5.5	–	–	2.0	μA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND per input pin; other inputs at V _{CC} or GND; I _O = 0	5.5	–	–	±10.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	80	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} − 2.1 V; other inputs at V _{CC} or GND; I _O = 0	4.5 to 5.5	–	–	1.5	mA
C _I	input capacitance		–	–	–	10	pF

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AC CHARACTERISTICS

74AHC573

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C _L (pF)				
V _{CC} = 3.0 to 3.6 V							
T _{amb} = 25 °C; note 1							
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	15	–	5.5	11.0	ns
	propagation delay LE to Qn	see Figs 7 and 10	15	–	5.8	11.9	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	–	5.8	11.5	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	–	6.8	11.0	ns
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	50	–	7.8	14.5	ns
	propagation delay LE to Qn	see Figs 7 and 10	50	–	8.3	15.4	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	–	8.3	15.0	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	–	9.7	14.5	ns
t _W	enable pulse width HIGH	see Figs 7 and 10	50	5.0	–	–	ns
t _{su}	set-up time Dn to LE	see Fig.8	50	3.5	–	–	ns
t _h	hold time Dn to LE	see Fig.8	50	1.5	–	–	ns
T _{amb} = –40 to +85 °C							
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	15	1.0	–	13.0	ns
	propagation delay LE to Qn	see Figs 7 and 10	15	1.0	–	14.0	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	1.0	–	13.5	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	1.0	–	13.0	ns
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	50	1.0	–	16.5	ns
	propagation delay LE to Qn	see Figs 7 and 10	50	1.0	–	17.5	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	1.0	–	17.0	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	1.0	–	16.5	ns
t _W	enable pulse width HIGH	see Figs 7 and 10	50	5.0	–	–	ns
t _{su}	set-up time Dn to LE	see Fig.8	50	3.5	–	–	ns
t _h	hold time Dn to LE	see Fig.8	50	1.5	–	–	ns

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C _L (pF)				
T _{amb} = −40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	15	1.0	–	14.0	ns
	propagation delay LE to Qn	see Figs 7 and 10	15	1.0	–	15.0	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	1.0	–	14.5	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	1.0	–	14.0	ns
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	50	1.0	–	18.5	ns
	propagation delay LE to Qn	see Figs 7 and 10	50	1.0	–	19.5	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	1.0	–	19.0	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	1.0	–	18.5	ns
t _W	enable pulse width HIGH	see Figs 7 and 10	50	5.0	–	–	ns
t _{su}	set-up time Dn to LE	see Fig.8	50	3.5	–	–	ns
t _h	hold time Dn to LE	see Fig.8	50	1.5	–	–	ns
V _{CC} = 4.5 to 5.5 V							
T _{amb} = 25 °C; note 2							
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	15	–	3.9	6.8	ns
	propagation delay LE to Qn	see Figs 7 and 10	15	–	4.2	7.7	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	–	4.4	7.7	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	–	4.6	7.7	ns
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	50	–	5.5	8.8	ns
	propagation delay LE to Qn	see Figs 7 and 10	50	–	5.9	9.7	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	–	6.3	9.7	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	–	7.4	9.7	ns
t _W	enable pulse width HIGH	see Figs 7 and 10	50	5.0	–	–	ns
t _{su}	set-up time Dn to LE	see Fig.8	50	3.5	–	–	ns
t _h	hold time Dn to LE	see Fig.8	50	1.5	–	–	ns
T _{amb} = −40 to +85 °C							
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	15	1.0	–	8.0	ns
	propagation delay LE to Qn	see Figs 7 and 10	15	1.0	–	9.0	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	1.0	–	9.0	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	1.0	–	9.0	ns
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	50	1.0	–	10.0	ns
	propagation delay LE to Qn	see Figs 7 and 10	50	1.0	–	11.0	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	1.0	–	11.0	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	1.0	–	11.0	ns
t _W	enable pulse width HIGH	see Figs 7 and 10	50	5.0	–	–	ns
t _{su}	set-up time Dn to LE	see Fig.8	50	3.5	–	–	ns
t _h	hold time Dn to LE	see Fig.8	50	1.5	–	–	ns

Octal D-type transparent latch; 3-state

74AHC573; 74AHCT573

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C _L (pF)				
T _{amb} = −40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	15	1.0	–	8.5	ns
	propagation delay LE to Qn	see Figs 7 and 10	15	1.0	–	10.0	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	1.0	–	10.0	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	1.0	–	10.0	ns
t _{PHL} /t _{PLH}	propagation delay Dn to Qn2	see Figs 6 and 10	50	1.0	–	11.0	ns
	propagation delay LE to Qn	see Figs 7 and 10	50	1.0	–	12.5	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	1.0	–	12.5	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	1.0	–	12.5	ns
t _W	enable pulse width HIGH	see Figs 7 and 10	50	5.0	–	–	ns
t _{su}	set-up time Dn to LE	see Fig.8	50	3.5	–	–	ns
t _h	hold time Dn to LE	see Fig.8	50	1.5	–	–	ns

Notes

1. Typical values at V_{CC} = 3.3 V.
2. Typical values at V_{CC} = 5.0 V.

Octal D-type transparent latch; 3-state

74AHC573; 74AHCT573

74AHCT573GND = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C _L (pF)				
V _{CC} = 4.5 to 5.5 V; note 1							
T _{amb} = 25 °C							
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	15	–	3.5	5.5	ns
	propagation delay LE to Qn	see Figs 7 and 10	15	–	3.9	6.0	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	–	4.1	6.5	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	–	4.5	6.5	ns
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	50	–	4.9	7.5	ns
	propagation delay LE to Qn	see Figs 7 and 10	50	–	5.5	8.5	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	–	5.9	8.5	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	–	6.4	9.0	ns
t _W	enable pulse width HIGH	see Figs 7 and 9	50	5.0	–	–	ns
t _{su}	set-up time Dn to LE	see Fig.8	50	3.5	–	–	ns
t _h	hold time Dn to LE	see Fig.8	50	1.5	–	–	ns
T _{amb} = –40 to +85 °C							
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	15	1	–	6.5	ns
	propagation delay LE to Qn	see Figs 7 and 10	15	1	–	7.0	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	1	–	7.5	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	1	–	7.5	ns
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	50	1	–	8.5	ns
	propagation delay LE to Qn	see Figs 7 and 10	50	1	–	9.5	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	1	–	10.0	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	1	–	10.0	ns
t _W	enable pulse width HIGH	see Figs 7 and 9	50	5.0	–	–	ns
t _{su}	set-up time Dn to LE	see Fig.8	50	3.5	–	–	ns
t _h	hold time Dn to LE	see Fig.8	50	1.5	–	–	ns

Octal D-type transparent latch; 3-state

74AHC573; 74AHCT573

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C _L (pF)				
T _{amb} = −40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 6 and 10	15	1	–	7.0	ns
	propagation delay LE to Qn	see Figs 7 and 10	15	1	–	7.5	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	1	–	8.5	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	15	1	–	8.5	ns
t _{PHL} /t _{PLH}	propagation delay Don to Qn	see Figs 6 and 10	50	1	–	9.5	ns
	propagation delay LE to Qn	see Figs 7 and 10	50	1	–	11.0	ns
t _{PZH} /t _{PZL}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	1	–	11.0	ns
t _{PHZ} /t _{PLZ}	propagation delay $\overline{OE}$ to Qn	see Figs 9 and 10	50	1	–	11.5	ns
t _W	enable pulse width HIGH	see Figs 7 and 9	50	5.0	–	–	ns
t _{su}	set-up time Dn to LE	see Fig.8	50	3.5	–	–	ns
t _h	hold time Dn to LE	see Fig.8	50	1.5	–	–	ns

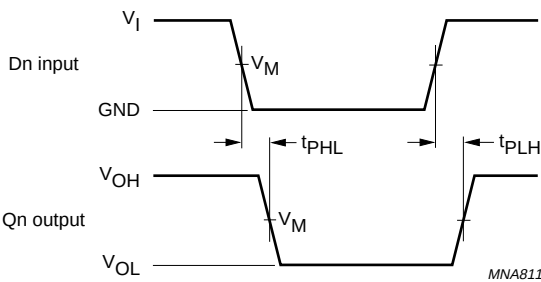
Note

1. Typical values at V_{CC} = 5.0 V.

Octal D-type transparent latch; 3-state

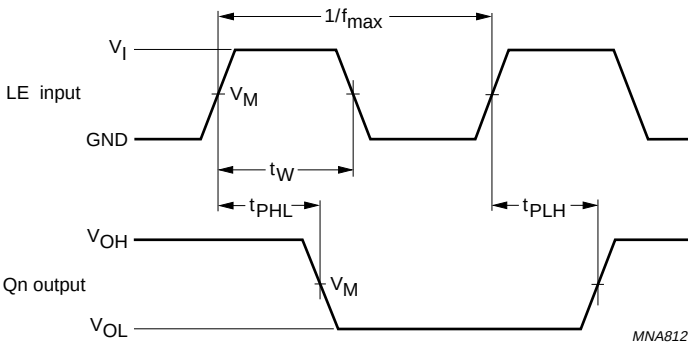
74AHC573; 74AHCT573

AC WAVEFORMS



FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
AHC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT	GND to 3.0 V	1.5 V	50% V_{CC}

Fig.6 The data input (Dn) to output (Qn) propagation delays.

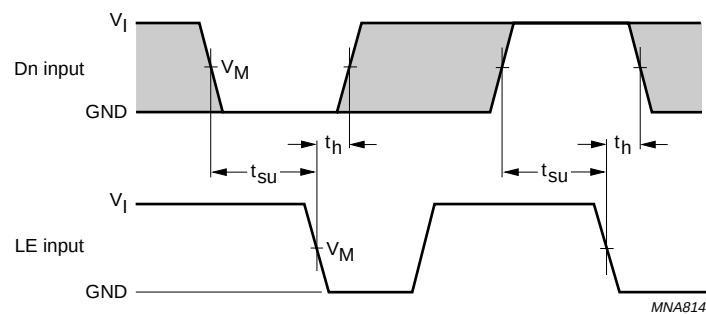


FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
AHC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT	GND to 3.0 V	1.5 V	50% V_{CC}

Fig.7 The latch enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays.

Octal D-type transparent latch; 3-state

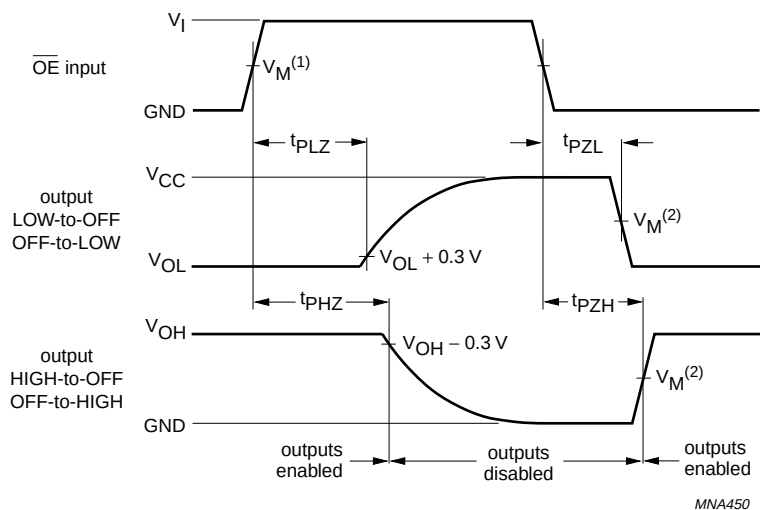
74AHC573; 74AHCT573



FAMILY	V _I INPUT REQUIREMENTS	V _M INPUT
AHC	GND to V _{CC}	50% V _{CC}
AHCT	GND to 3.0 V	1.5 V

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.8 Data set-up and hold times for the Dn input to the LE input.

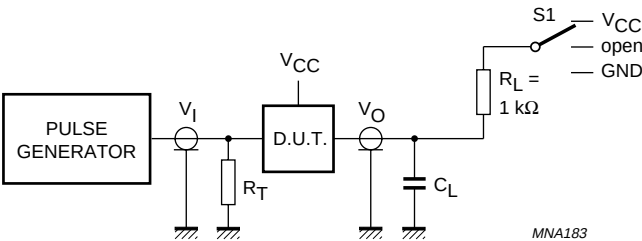


FAMILY	V _I INPUT REQUIREMENTS	V _M (¹) INPUT	V _M (²) OUTPUT
AHC	GND to V _{CC}	50% V _{CC}	50% V _{CC}
AHCT	GND to 3.0 V	1.5 V	50% V _{CC}

Fig.9 The 3-state enable and disable times.

Octal D-type transparent latch; 3-state

74AHC573; 74AHCT573



TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
 R_L = Load resistor.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.10 Load circuitry for switching times.

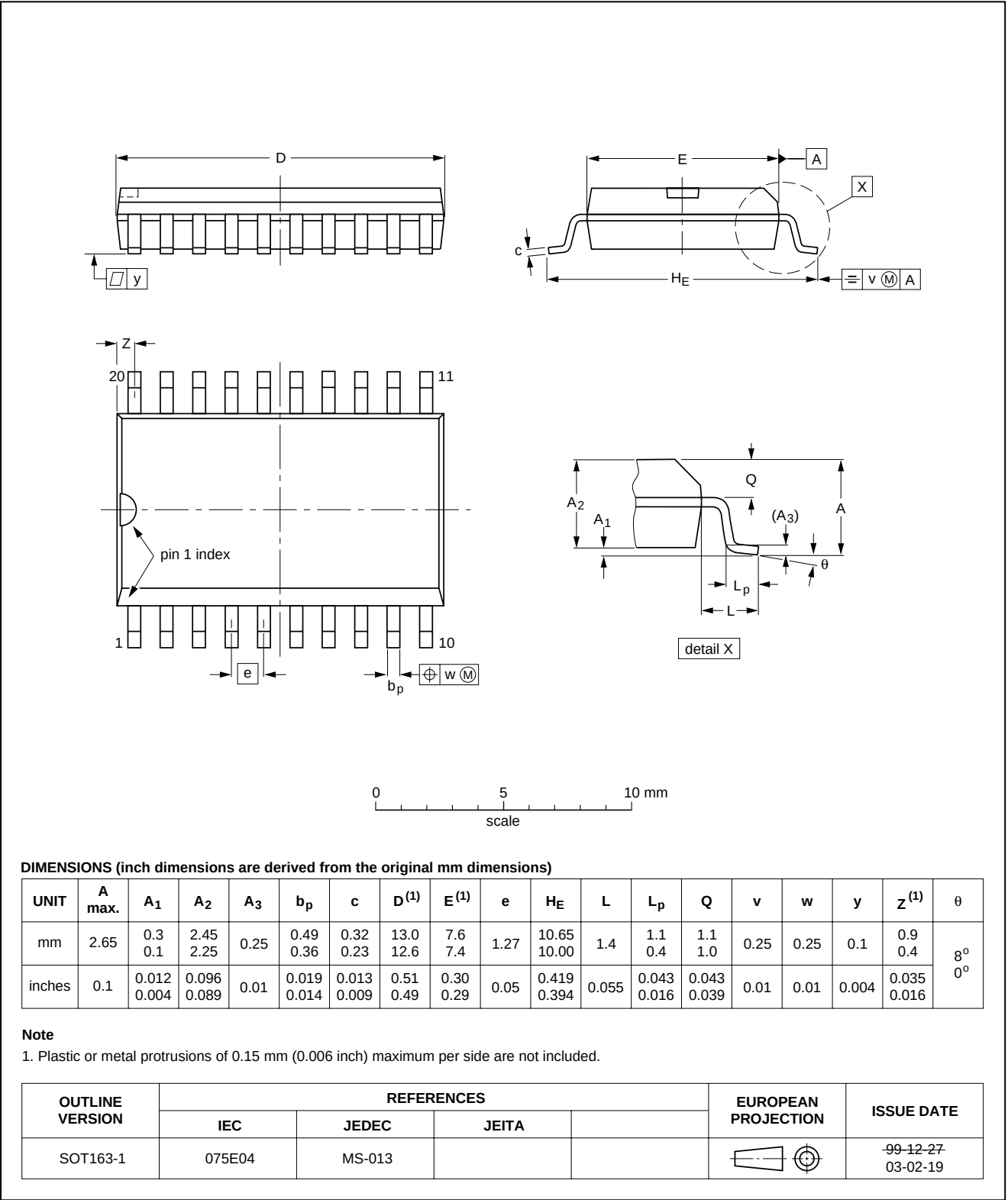
Octal D-type transparent latch; 3-state

74AHC573; 74AHCT573

PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

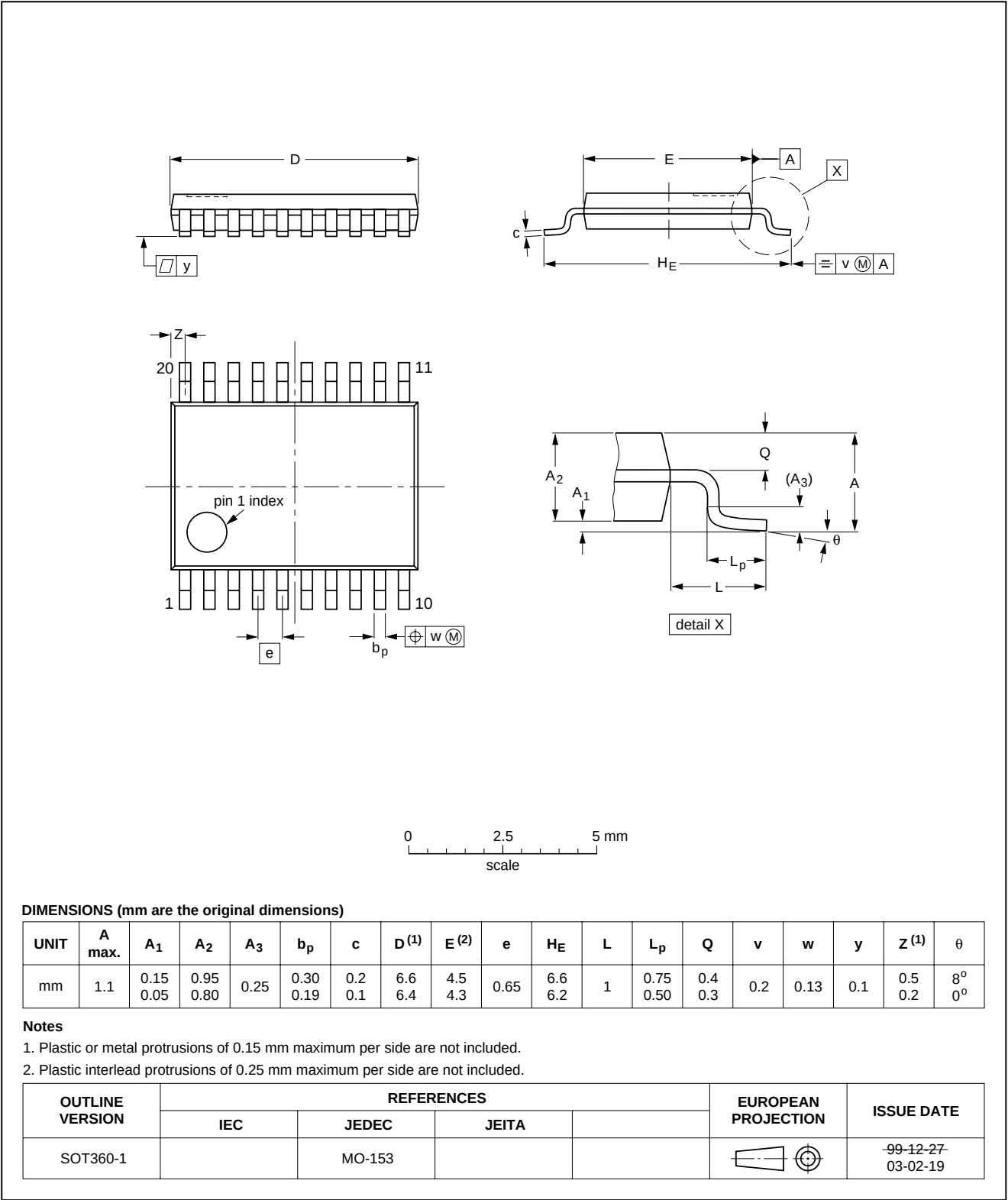


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74AHC573; 74AHCT573

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
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