

# 74AHC74; 74AHCT74

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 7 — 21 April 2015

Product data sheet

## 1. General description

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The 74AHC74; 74AHCT74 is a high-speed Si-gate CMOS device and is pin compatible with Low-Power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC74; 74AHCT74 is a dual positive-edge triggered, D-type flip-flop with individual data inputs (D), clock inputs (CP), set inputs ( $\overline{SD}$ ) and reset inputs ( $\overline{RD}$ ). It also has complementary outputs (Q and  $\overline{Q}$ ).

The set and reset are asynchronous active LOW inputs that operate independent of the clock input. Information on the data input is transferred to the Q output on the LOW to HIGH transition of the clock pulse. The data inputs must be stable one set-up time prior to the LOW to HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

## 2. Features and benefits

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- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than  $V_{CC}$
- Input levels:
  - ◆ For 74AHC74: CMOS level
  - ◆ For 74AHCT74: TTL level
- ESD protection:
  - ◆ HBM EIA/JESD22-A114E exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V
  - ◆ CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<b>74AHC74</b>				
74AHC74D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHC74PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHC74BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
<b>74AHCT74</b>				
74AHCT74D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCT74PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCT74BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

### 4. Functional diagram

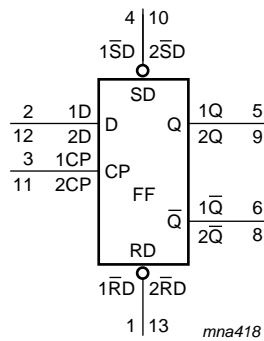


Fig 1. Functional diagram

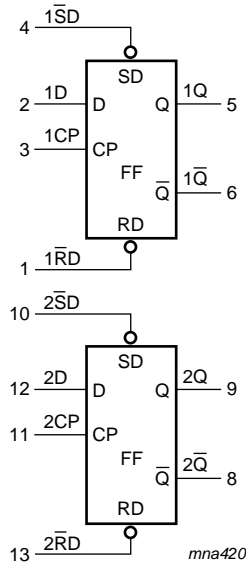


Fig 2. Logic symbol

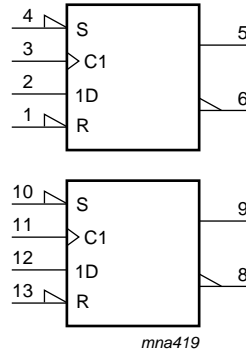


Fig 3. IEC logic symbol

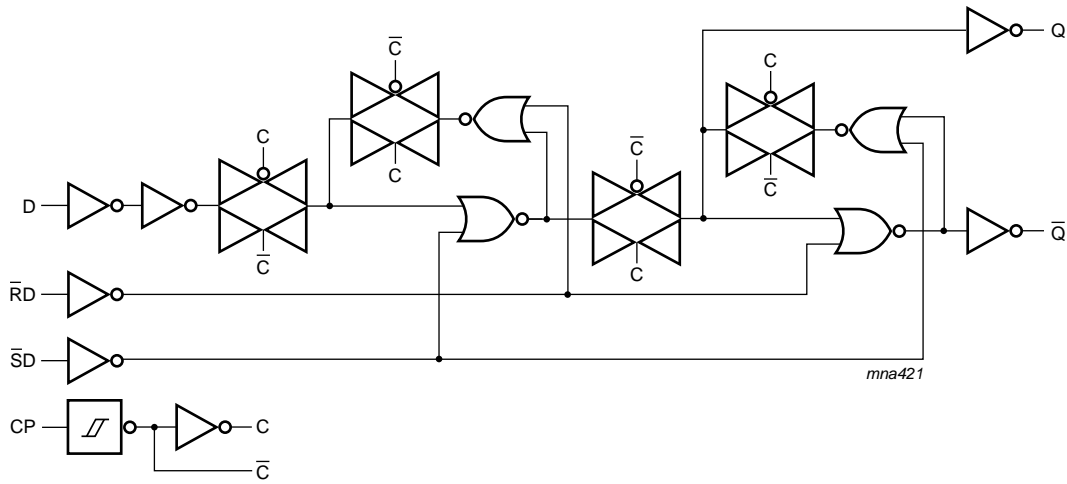
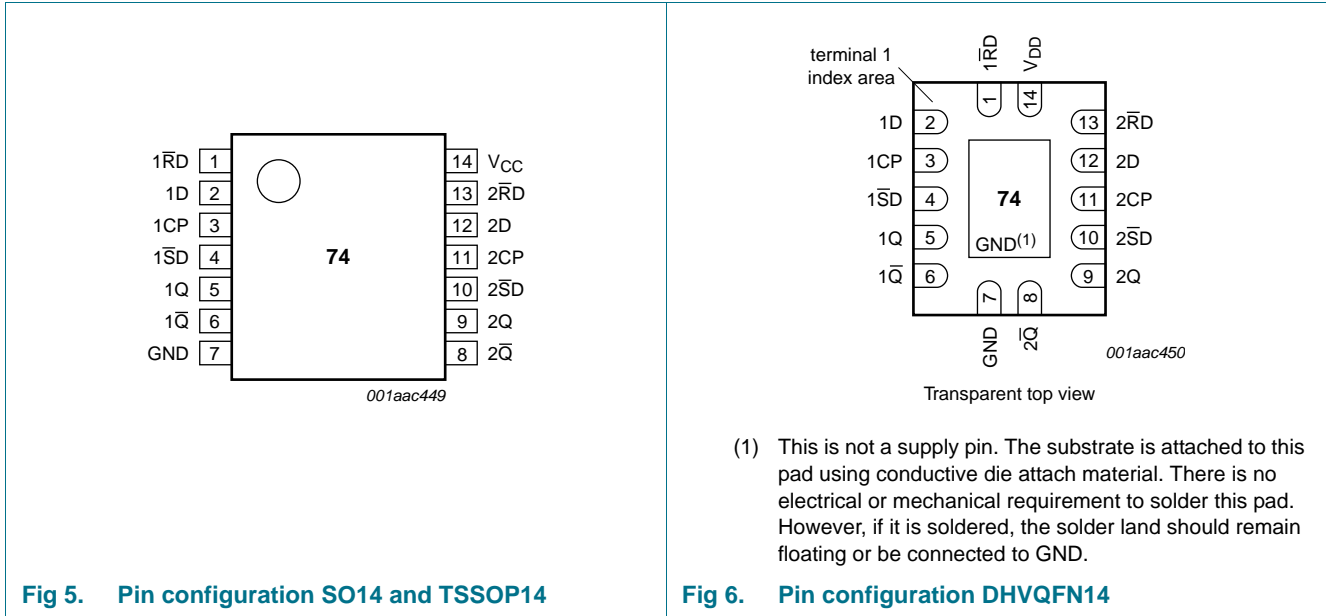


Fig 4. Logic diagram (one flip-flop)

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1 $\overline{\text{RD}}$	1	asynchronous reset direct input (active LOW)
1D	2	data input
1CP	3	clock input (LOW to HIGH, edge-triggered)
1 $\overline{\text{SD}}$	4	asynchronous set direct input (active LOW)
1Q	5	true flip-flop output
1 $\overline{\text{Q}}$	6	complement flip-flop output
GND	7	ground (0 V)
2 $\overline{\text{Q}}$	8	complement flip-flop output
2Q	9	true flip-flop output
2 $\overline{\text{SD}}$	10	asynchronous set direct input (active LOW)
2CP	11	clock input (LOW to HIGH, edge-triggered)
2D	12	data input
2 $\overline{\text{RD}}$	13	asynchronous reset direct input (active LOW)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Control			Input	Output			
nSD	nRD	nCP	nD	nQ	nQ̄	nQ <sub>n+1</sub>	nQ̄ <sub>n+1</sub>
L	H	X	X	H	L	-	-
H	L	X	X	L	H	-	-
L	L	X	X	H	H	-	-
H	H	↑	L	-	-	L	H
H	H	↑	H	-	-	H	L

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 ↑ = LOW to HIGH transition;  
 Q<sub>n+1</sub> = state after the next LOW to HIGH CP transition;  
 X = don't care.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	[1] -20	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	[1] -20	+20	mA
I <sub>O</sub>	output current	V <sub>O</sub> = -0.5 V to (V <sub>CC</sub> + 0.5 V)	-25	+25	mA
I <sub>CC</sub>	supply current		-	+75	mA
I <sub>GND</sub>	ground current		-75	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[2] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] For SO14 packages: above 70 °C the value of P<sub>tot</sub> derates linearly at 8 mW/K.  
 For TSSOP14 packages: above 60 °C the value of P<sub>tot</sub> derates linearly at 5.5 mW/K.  
 For DHVQFN14 packages: above 60 °C the value of P<sub>tot</sub> derates linearly at 4.5 mW/K.

## 8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>74AHC74</b>						
$V_{CC}$	supply voltage		2.0	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	100	ns/V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	20	ns/V
<b>74AHCT74</b>						
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	20	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC74</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	-	-	1.5	-	1.5	-	V
		$V_{CC} = 3.0\text{ V}$	2.1	-	-	2.1	-	2.1	-	V
		$V_{CC} = 5.5\text{ V}$	3.85	-	-	3.85	-	3.85	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	-	0.5	-	0.5	-	0.5	V
		$V_{CC} = 3.0\text{ V}$	-	-	0.9	-	0.9	-	0.9	V
		$V_{CC} = 5.5\text{ V}$	-	-	1.65	-	1.65	-	1.65	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -50\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50\ \mu\text{A}; V_{CC} = 3.0\text{ V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0\text{ mA}; V_{CC} = 3.0\text{ V}$	2.58	-	-	2.48	-	2.40	-	V
	$I_O = -8.0\text{ mA}; V_{CC} = 4.5\text{ V}$	3.94	-	-	3.80	-	3.70	-	V	
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 50\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50\ \mu\text{A}; V_{CC} = 3.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.36	-	0.44	-	0.55	V
	$I_O = 8.0\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.36	-	0.44	-	0.55	V	

**Table 6.** Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	$\mu\text{A}$
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
<b>74AHCT74</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = -50 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = 50 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; other pins at $V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF

## 10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 9](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
<b>74AHC74</b>										
t <sub>pd</sub>	propagation delay	nCP to nQ, n $\bar{Q}$ ; see <a href="#">Figure 7</a> <sup>[2]</sup>								
		V <sub>CC</sub> = 3.0 V to 3.6 V								
		C <sub>L</sub> = 15 pF	-	5.2	11.9	1.0	14.0	1.0	15.0	ns
		C <sub>L</sub> = 50 pF	-	7.4	15.4	1.0	17.5	1.0	19.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	3.7	7.3	1.0	8.5	1.0	9.5	ns
		C <sub>L</sub> = 50 pF	-	5.2	9.3	1.0	10.5	1.0	12.0	ns
		n $\bar{S}D$ , n $\bar{R}D$ to nQ, n $\bar{Q}$ ; see <a href="#">Figure 8</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V								
		C <sub>L</sub> = 15 pF	-	5.4	12.3	1.0	14.5	1.0	15.5	ns
		C <sub>L</sub> = 50 pF	-	7.7	15.8	1.0	18.0	1.0	20.0	ns
		f <sub>max</sub>	maximum frequency	see <a href="#">Figure 7</a>						
V <sub>CC</sub> = 3.0 V to 3.6 V										
C <sub>L</sub> = 15 pF	80			125	-	70	-	70	-	MHz
C <sub>L</sub> = 50 pF	50			75	-	45	-	45	-	MHz
V <sub>CC</sub> = 4.5 V to 5.5 V										
C <sub>L</sub> = 15 pF	130			170	-	110	-	110	-	MHz
t <sub>w</sub>	pulse width	CP HIGH or LOW; n $\bar{S}D$ , n $\bar{R}D$ LOW; see <a href="#">Figure 7</a> and <a href="#">8</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	6.0	-	-	7.0	-	7.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
t <sub>su</sub>	set-up time	nD to nCP; see <a href="#">Figure 7</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	6.0	-	-	7.0	-	7.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
t <sub>h</sub>	hold time	nD to nCP; see <a href="#">Figure 7</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	-	-	0.5	-	0.5	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	-	-	0.5	-	0.5	-	ns
t <sub>rec</sub>	recovery time	nRD to nCP; see <a href="#">Figure 8</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	3.0	-	-	3.0	-	3.0	-	ns



**Table 7. Dynamic characteristics ...continued**Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 9](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[3]</sup>	-	12	-	-	-	-	-	pF
<b>74AHCT74; V<sub>CC</sub> = 4.5 V to 5.5 V</b>										
t <sub>pd</sub>	propagation delay	nCP to nQ, nQ̄; see <a href="#">Figure 7</a> <sup>[2]</sup>								
		C <sub>L</sub> = 15 pF	-	3.3	7.8	1.0	9.0	1.0	10.0	ns
		C <sub>L</sub> = 50 pF	-	4.8	8.8	1.0	10.0	1.0	11.0	ns
		nSD, nRD to nQ, nQ̄; see <a href="#">Figure 7</a>								
		C <sub>L</sub> = 15 pF	-	3.7	10.4	1.0	12.0	1.0	13.0	ns
		C <sub>L</sub> = 50 pF	-	5.3	11.4	1.0	13.0	1.0	14.5	ns
f <sub>max</sub>	maximum frequency	see <a href="#">Figure 7</a>								
		C <sub>L</sub> = 15 pF	100	160	-	80	-	80	-	MHz
		C <sub>L</sub> = 50 pF	80	140	-	65	-	65	-	MHz
t <sub>W</sub>	pulse width	CP HIGH or LOW; nSD, nRD LOW; see <a href="#">Figure 7</a> and <a href="#">8</a>	5.0	-	-	5.0	-	5.0	-	ns
t <sub>su</sub>	set-up time	nD to nCP; see <a href="#">Figure 7</a>	5.0	-	-	5.0	-	5.0	-	ns
t <sub>h</sub>	hold time	nD to nCP; see <a href="#">Figure 7</a>	0	-	-	0	-	0	-	ns
t <sub>rec</sub>	recovery time	nRD to nCP; see <a href="#">Figure 8</a>	3.5	-	-	3.5	-	3.5	-	ns
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[3]</sup>	-	16	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V and V<sub>CC</sub> = 5.0 V).

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

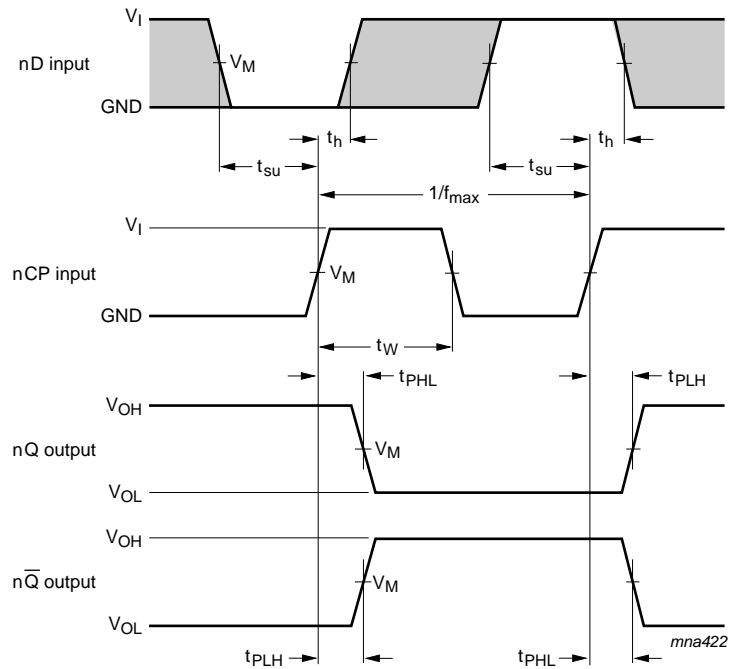
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

## 11. Waveforms

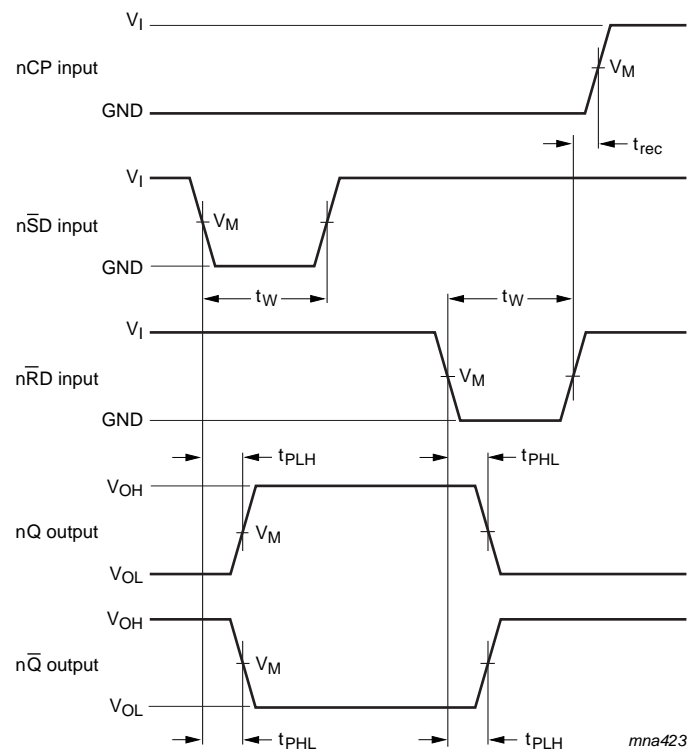


Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Clock pulse width, maximum frequency, set-up times, hold times and input to output propagation delays**



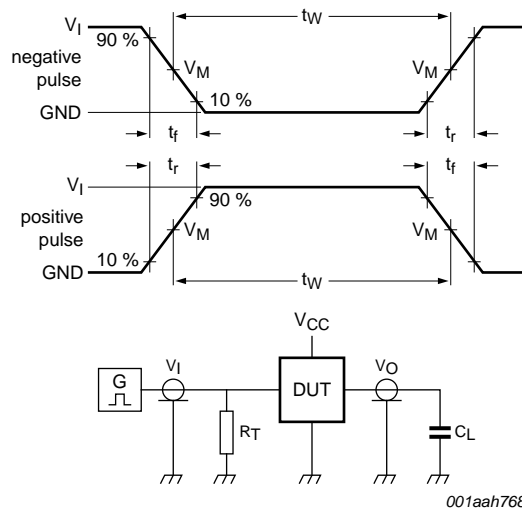
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 8. Set and reset pulse widths, recovery time and input to output propagation delays**

**Table 8. Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74AHC74	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT74	1.5 V	$0.5 \times V_{CC}$



For test data, see [Table 9](#).

Definitions for test circuit:

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

**Fig 9. Load circuitry for switching times**

**Table 9. Test data**

Type	Input		Load	Test
	$V_I$	$t_r, t_f$	$C_L$	
74AHC74	$V_{CC}$	$\leq 3.0$ ns	50 pF, 15 pF	$t_{PLH}, t_{PHL}$
74AHCT74	3.0 V	$\leq 3.0$ ns	50 pF, 15 pF	$t_{PLH}, t_{PHL}$

## 12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

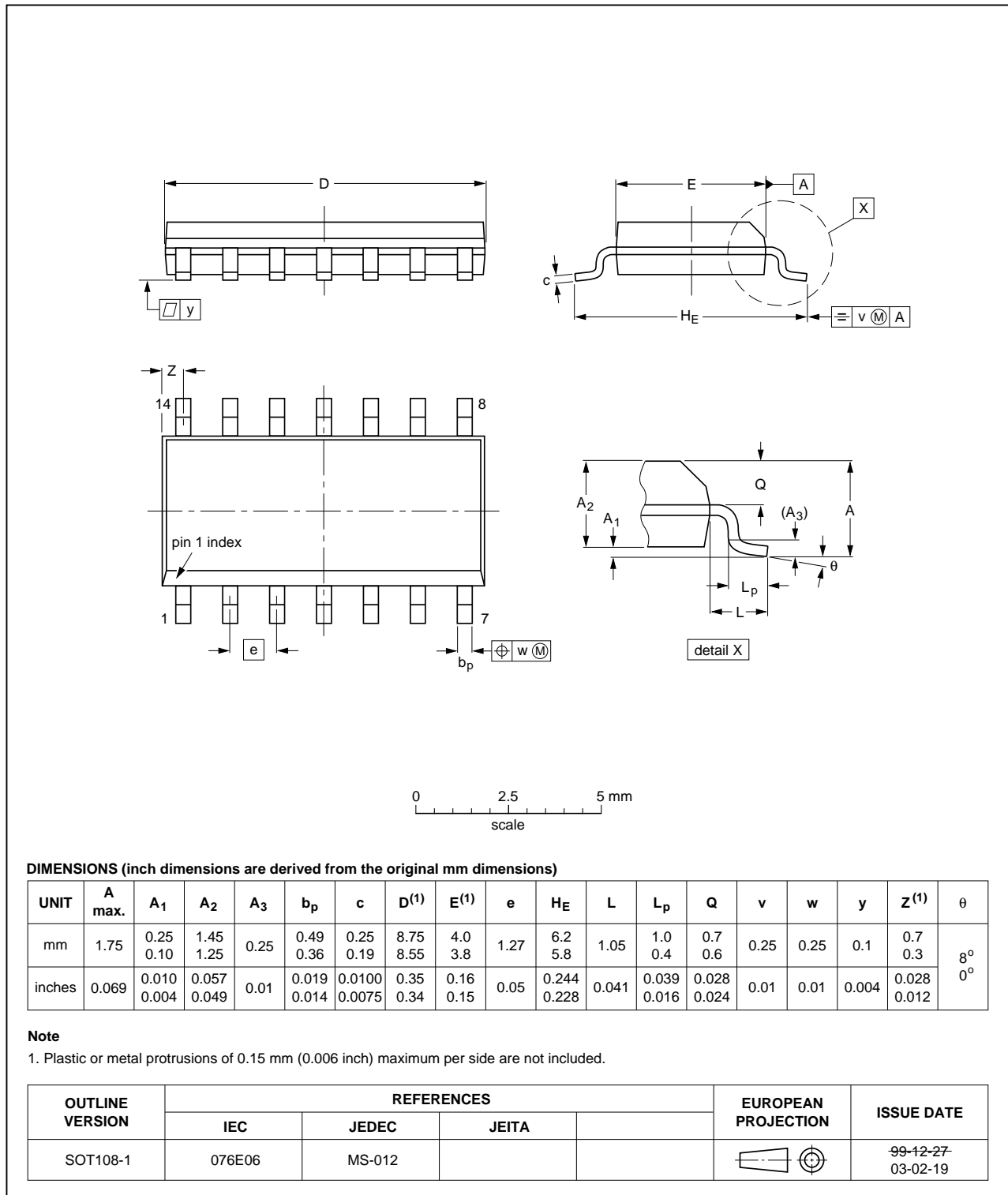


Fig 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

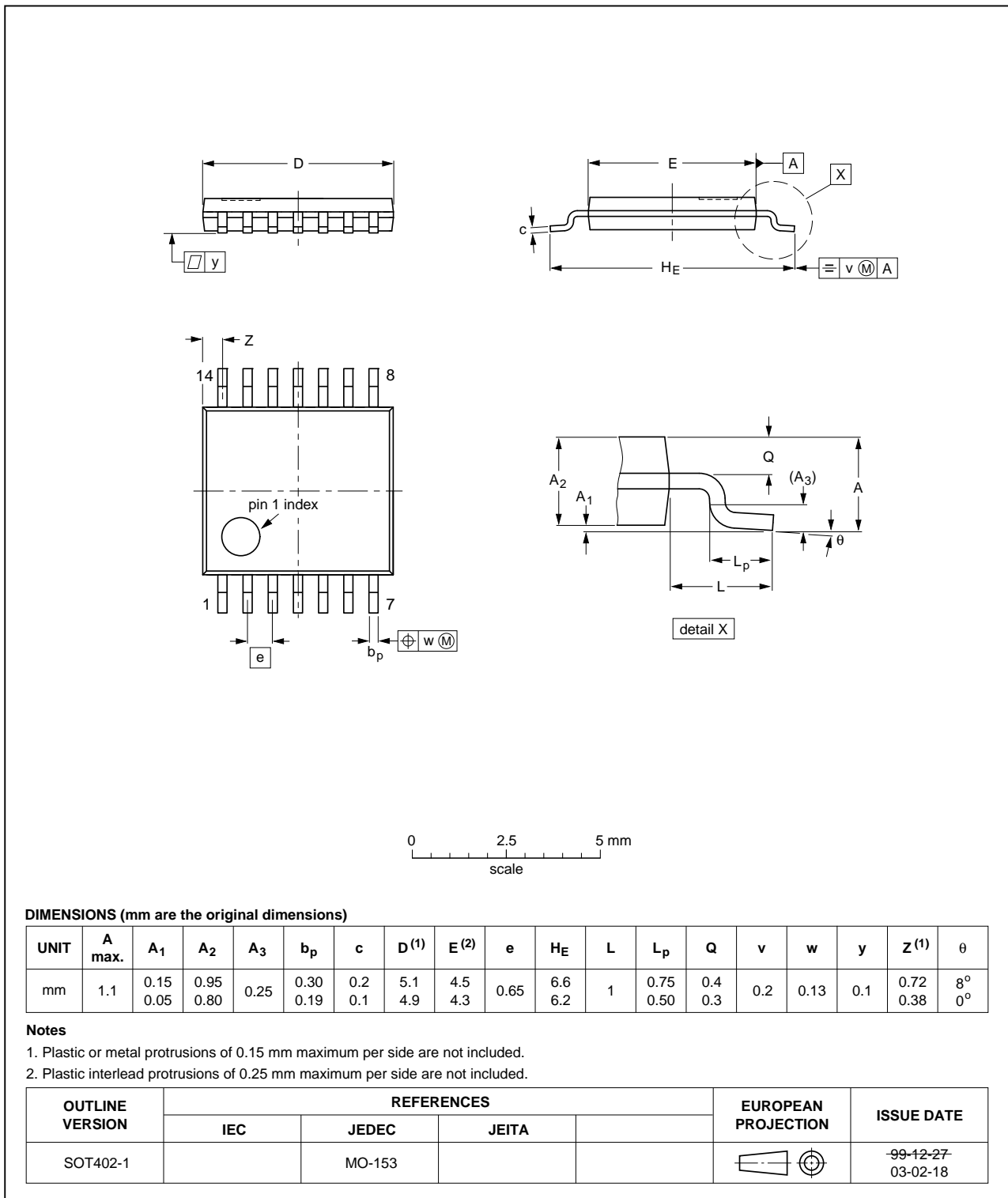


Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

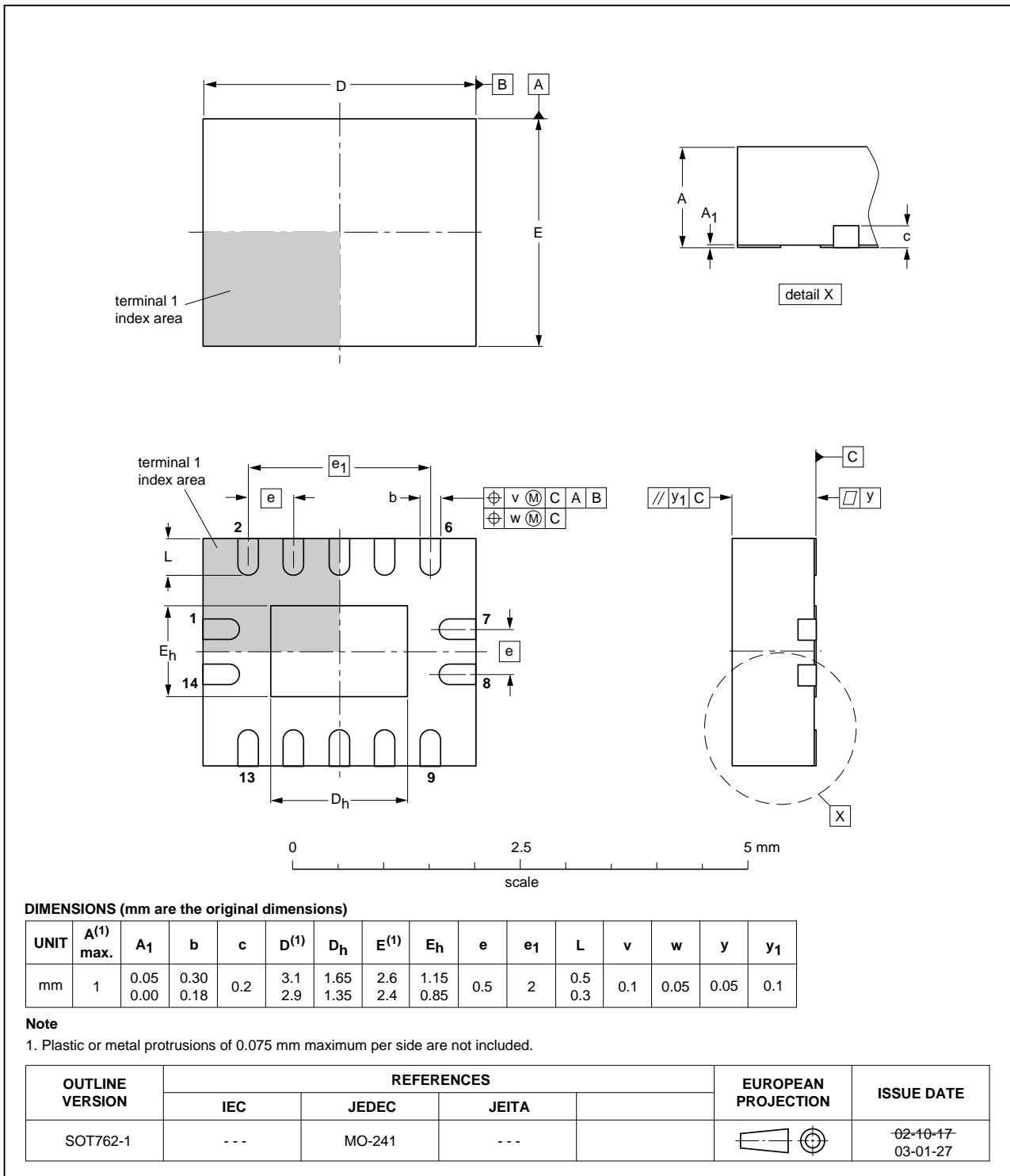


Fig 12. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT74 v.7	20150421	Product data sheet	-	74AHC_AHCT74 v.6
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 7</a>: minimum <math>f_{max}</math> values at 3.0 V to 3.6 V for 74AHC74 corrected (errata).</li> </ul>			
74AHC_AHCT74 v.6	20141020	Product data sheet	-	74AHC_AHCT74 v.5
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 3</a> corrected (errata).</li> </ul>			
74AHC_AHCT74 v.5	20080609	Product data sheet	-	74AHC_AHCT74 v.4
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Table 6: the conditions for input leakage current have been changed.</li> </ul>			
74AHC_AHCT74 v.4	20050207	Product data sheet	-	74AHC_AHCT74 v.3
74AHC_AHCT74 v.3	20040429	Product specification	-	74AHC_AHCT74 v.2
74AHC_AHCT74 v.2	19990923	Product specification	-	74AHC_AHCT74 v.1
74AHC_AHCT74 v.1	19990805	Product specification	-	-



## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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