

# 74AHCU04

Hex unbuffered inverter

Rev. 4 — 7 December 2015

Product data sheet

## 1. General description

The 74AHCU04 is high-speed Si-gate CMOS devices and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHCU04 is a general purpose hex unbuffered inverter. Each of the six inverters is a single stage.

## 2. Features and benefits

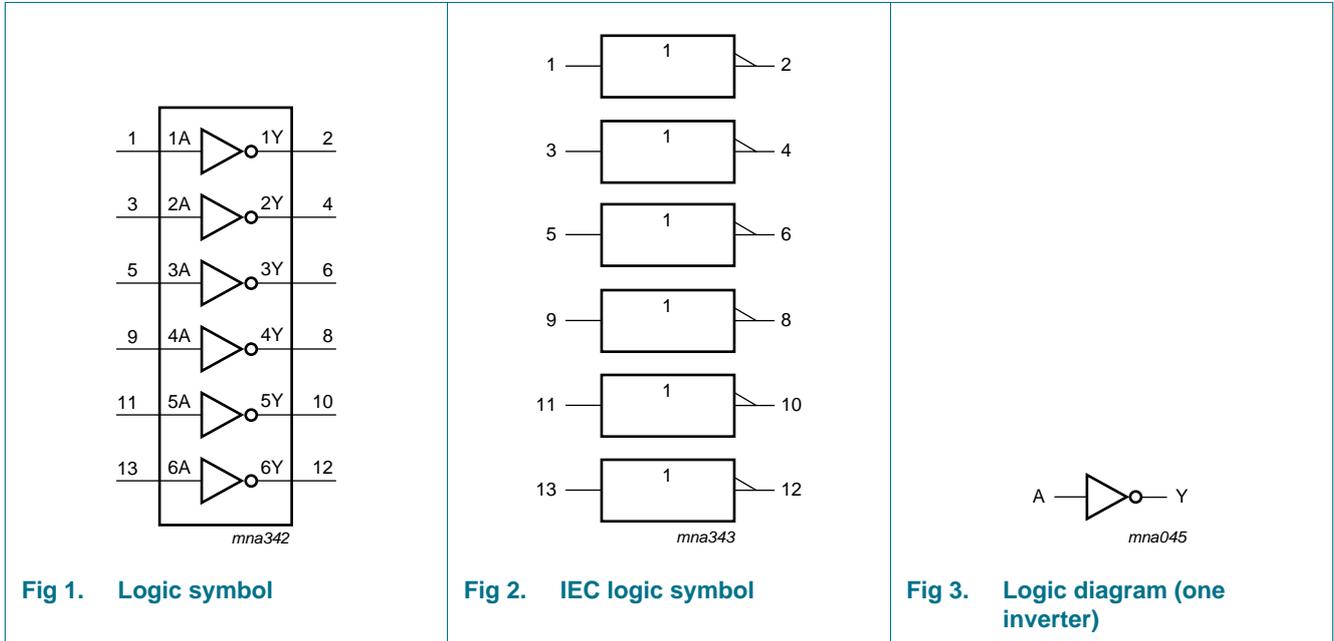
- Low power dissipation
- Balanced propagation delays
- Inputs accepts voltages higher than  $V_{CC}$
- ESD protection:
  - ◆ HBM JESD22-A114F: exceeds 2000 V
  - ◆ MM JESD22-A115-A: exceeds 200 V
  - ◆ CDM JESD22-C101C: exceeds 1000 V
- Multiple package options
- Specified from  $-40\text{ °C}$  to  $+125\text{ °C}$

## 3. Ordering information

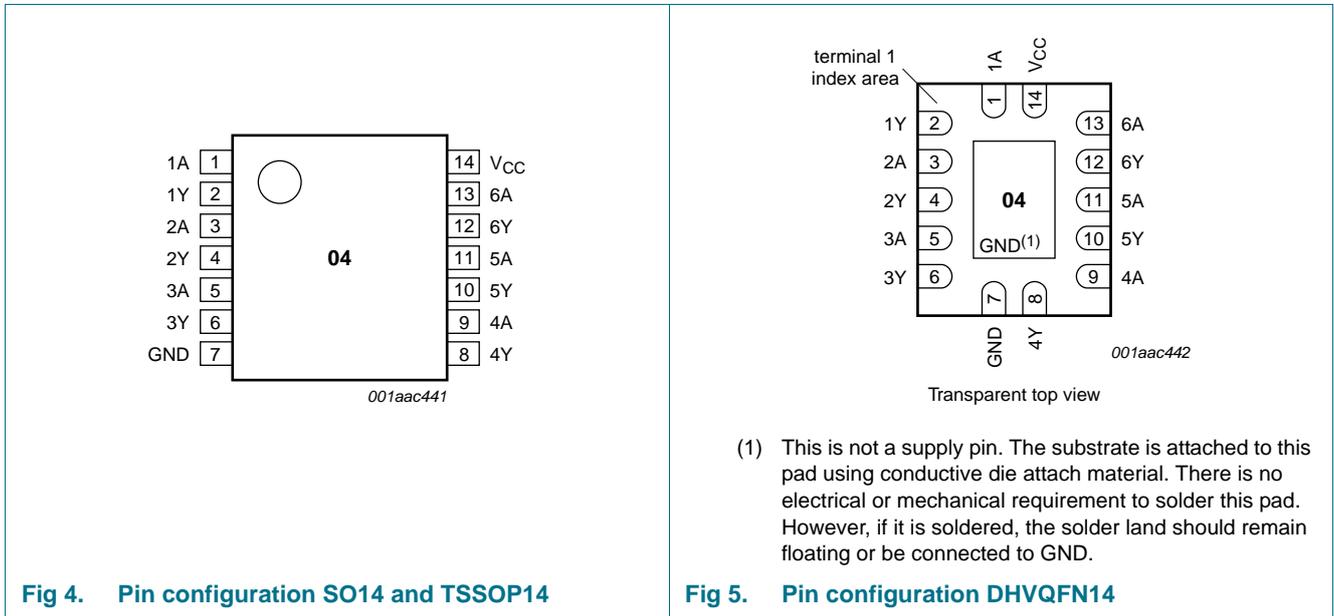
Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AHCU04D	$-40\text{ °C}$ to $+125\text{ °C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCU04PW	$-40\text{ °C}$ to $+125\text{ °C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCU04BQ	$-40\text{ °C}$ to $+125\text{ °C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1

4. Functional diagram



5. Pinning information



## 5.1 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
nA	nY
L	H
H	L

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	-20	-	mA
V <sub>I</sub>	input voltage		[1] -0.5	+7.0	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	-	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	75	mA
I <sub>GND</sub>	ground current		-75	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[2] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] For SO14 packages: above 70 °C the value of P<sub>tot</sub> derates linearly with 8 mW/K.  
 For TSSOP14 packages: above 60 °C the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.  
 For DHVQFN14 packages: above 60 °C the value of P<sub>tot</sub> derates linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	-	-	100	ns/V
		$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0 \text{ V}$	1.7	-	-	1.7	-	1.7	-	V
		$V_{CC} = 3.0 \text{ V}$	2.4	-	-	2.4	-	2.4	-	V
		$V_{CC} = 5.5 \text{ V}$	4.4	-	-	4.4	-	4.4	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0 \text{ V}$	-	-	0.3	-	0.3	-	0.3	V
		$V_{CC} = 3.0 \text{ V}$	-	-	0.6	-	0.6	-	0.6	V
		$V_{CC} = 5.5 \text{ V}$	-	-	1.1	-	1.1	-	1.1	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -50 \mu\text{A}$ ; $V_{CC} = 2.0 \text{ V}$	1.8	2.0	-	1.8	-	1.8	-	V
		$I_O = -50 \mu\text{A}$ ; $V_{CC} = 3.0 \text{ V}$	2.7	3.0	-	2.7	-	2.7	-	V
		$I_O = -50 \mu\text{A}$ ; $V_{CC} = 4.5 \text{ V}$	4.0	4.5	-	4.0	-	4.0	-	V
		$I_O = -4.0 \text{ mA}$ ; $V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.4	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 50 \mu\text{A}$ ; $V_{CC} = 2.0 \text{ V}$	-	0	0.2	-	0.2	-	0.2	V
		$I_O = 50 \mu\text{A}$ ; $V_{CC} = 3.0 \text{ V}$	-	0	0.3	-	0.3	-	0.3	V
		$I_O = 50 \mu\text{A}$ ; $V_{CC} = 4.5 \text{ V}$	-	0	0.5	-	0.5	-	0.5	V
		$I_O = 4.0 \text{ mA}$ ; $V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to $5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
		$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	$\mu\text{A}$
$C_I$	input capacitance		-	3	10	-	10	-	10	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
*GND = 0 V; For test circuit see Figure 7.*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA to nY; see Figure 6 [1]								
		V <sub>CC</sub> = 3.0 V to 3.6 V [2]								
		C <sub>L</sub> = 15 pF	-	3.0	7.1	1.0	8.5	1.0	9.0	ns
		C <sub>L</sub> = 50 pF	-	3.4	10.6	1.0	12.0	1.0	13.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [3]								
		C <sub>L</sub> = 15 pF	-	2.4	5.5	1.0	6.5	1.0	7.0	ns
		C <sub>L</sub> = 50 pF	-	3.5	7.0	1.0	8.0	1.0	9.0	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [4]	-	9.1	-	-	-	-	-	pF

- [1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [2] Typical values are measured at V<sub>CC</sub> = 3.3 V.
- [3] Typical values are measured at V<sub>CC</sub> = 5.0 V.
- [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V;  
 N = number of inputs switching;  
 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## 11. Waveforms

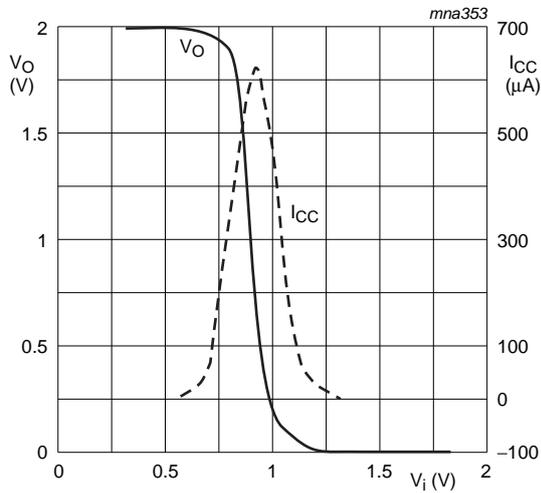
$V_M = 0.5 \times V_{CC}; V_I = \text{GND to } V_{CC}.$

**Fig 6. The input (nA) to output (nY) propagation delay times**

Test data is given in [Table 7](#).  
 Definitions for test circuit:  
 C<sub>L</sub> = Load capacitance including jig and probe capacitance.  
 R<sub>T</sub> = Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator.

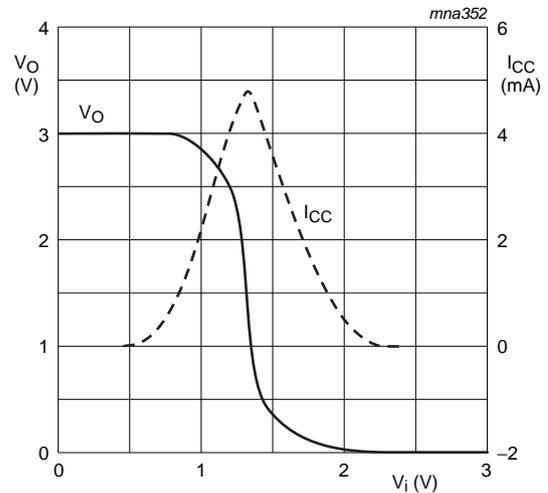
**Fig 7. Load circuit for switching times**

## 12. Typical transfer characteristics



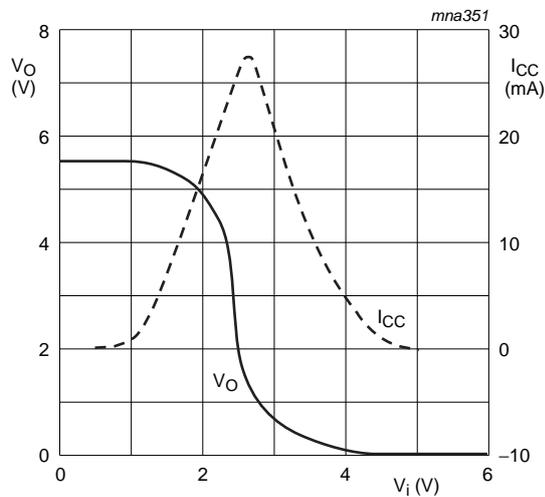
T<sub>amb</sub> = 25 °C.

Fig 8. V<sub>CC</sub> = 2.0 V; I<sub>O</sub> = 0 A



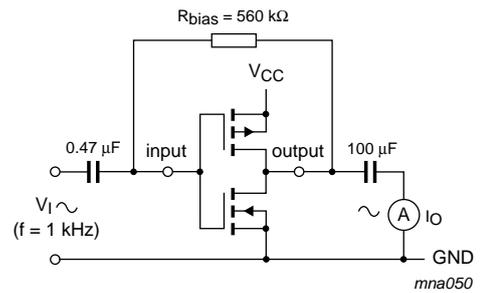
T<sub>amb</sub> = 25 °C.

Fig 9. V<sub>CC</sub> = 3.0 V; I<sub>O</sub> = 0 A



T<sub>amb</sub> = 25 °C.

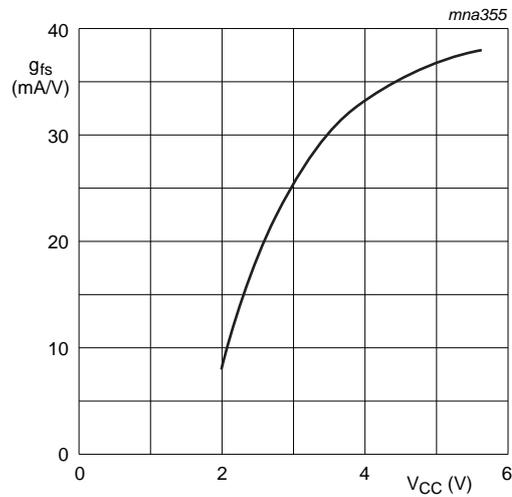
Fig 10. V<sub>CC</sub> = 5.5 V; I<sub>O</sub> = 0 A



$$g_{fs} = \frac{\Delta I_o}{\Delta V_i}$$

f<sub>i</sub> = 1 kHz at V<sub>O</sub> is constant

Fig 11. Test set-up for measuring forward transconductance



T<sub>amb</sub> = 25 °C.

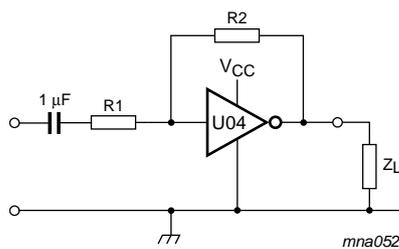
Fig 12. Typical forward transconductance as a function of the supply voltage

### 13. Application information

Some applications are:

- Linear amplifier (see [Figure 13](#))
- In crystal oscillator design (see [Figure 14](#))

**Remark:** All values given are typical unless otherwise specified.



Maximum V<sub>o(p-p)</sub> = V<sub>CC</sub> - 1.5 V centered at 0.5 × V<sub>CC</sub>.

$$G_v = -\frac{G_{ol}}{1 + \frac{R1}{R2}(1 + G_{ol})}$$

G<sub>ol</sub> = open loop gain

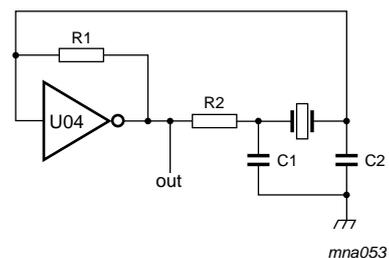
G<sub>v</sub> = voltage gain

R1 ≥ 3 kΩ, R2 ≤ 1 MΩ

Z<sub>L</sub> > 10 kΩ; G<sub>ol</sub> = 12 (typical)

Typical unity gain bandwidth product is 5 MHz.

Fig 13. Used as a linear amplifier



C1 = 47 pF (typical)

C2 = 33 pF (typical)

R1 = 1 MΩ to 10 MΩ (typical)

R2 optimum value depends on the frequency and required stability against changes in V<sub>CC</sub> or average minimum I<sub>CC</sub> (I<sub>CC</sub> is typically 5 mA at V<sub>CC</sub> = 5 V and f<sub>i</sub> = 10 MHz).

Fig 14. Crystal oscillator configuration

**Table 8. External components for resonator (f < 1 MHz)***All values given are typical and must be used as an initial set-up.*

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	22 M $\Omega$	220 k $\Omega$	56 pF	20 pF
16 kHz to 24.9 kHz	22 M $\Omega$	220 k $\Omega$	56 pF	10 pF
25 kHz to 54.9 kHz	22 M $\Omega$	100 k $\Omega$	56 pF	10 pF
55 kHz to 129.9 kHz	22 M $\Omega$	100 k $\Omega$	47 pF	5 pF
130 kHz to 199.9 kHz	22 M $\Omega$	47 k $\Omega$	47 pF	5 pF
200 kHz to 349.9 kHz	10 M $\Omega$	47 k $\Omega$	47 pF	5 pF
350 kHz to 600 kHz	10 M $\Omega$	47 k $\Omega$	47 pF	5 pF

**Table 9. Optimum value for R2**

Frequency	R2	Optimum for
3 kHz	2.0 k $\Omega$	minimum required I <sub>CC</sub>
	8.0 k $\Omega$	minimum influence due to change in V <sub>CC</sub>
6 kHz	1.0 k $\Omega$	minimum required I <sub>CC</sub>
	4.7 k $\Omega$	minimum influence by V <sub>CC</sub>
10 kHz	0.5 k $\Omega$	minimum required I <sub>CC</sub>
	2.0 k $\Omega$	minimum influence by V <sub>CC</sub>
14 kHz	0.5 k $\Omega$	minimum required I <sub>CC</sub>
	1.0 k $\Omega$	minimum influence by V <sub>CC</sub>
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF

14. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

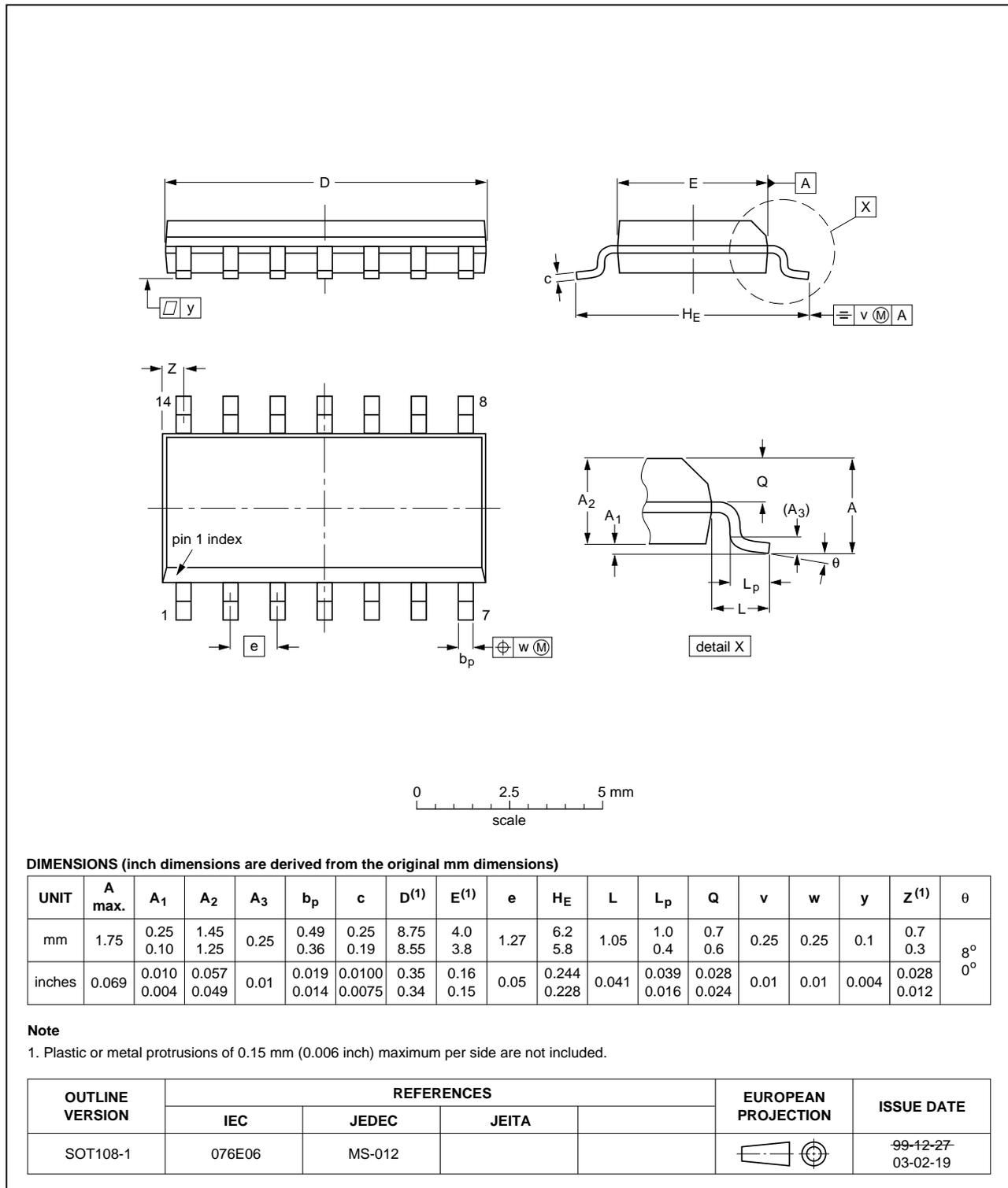


Fig 15. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

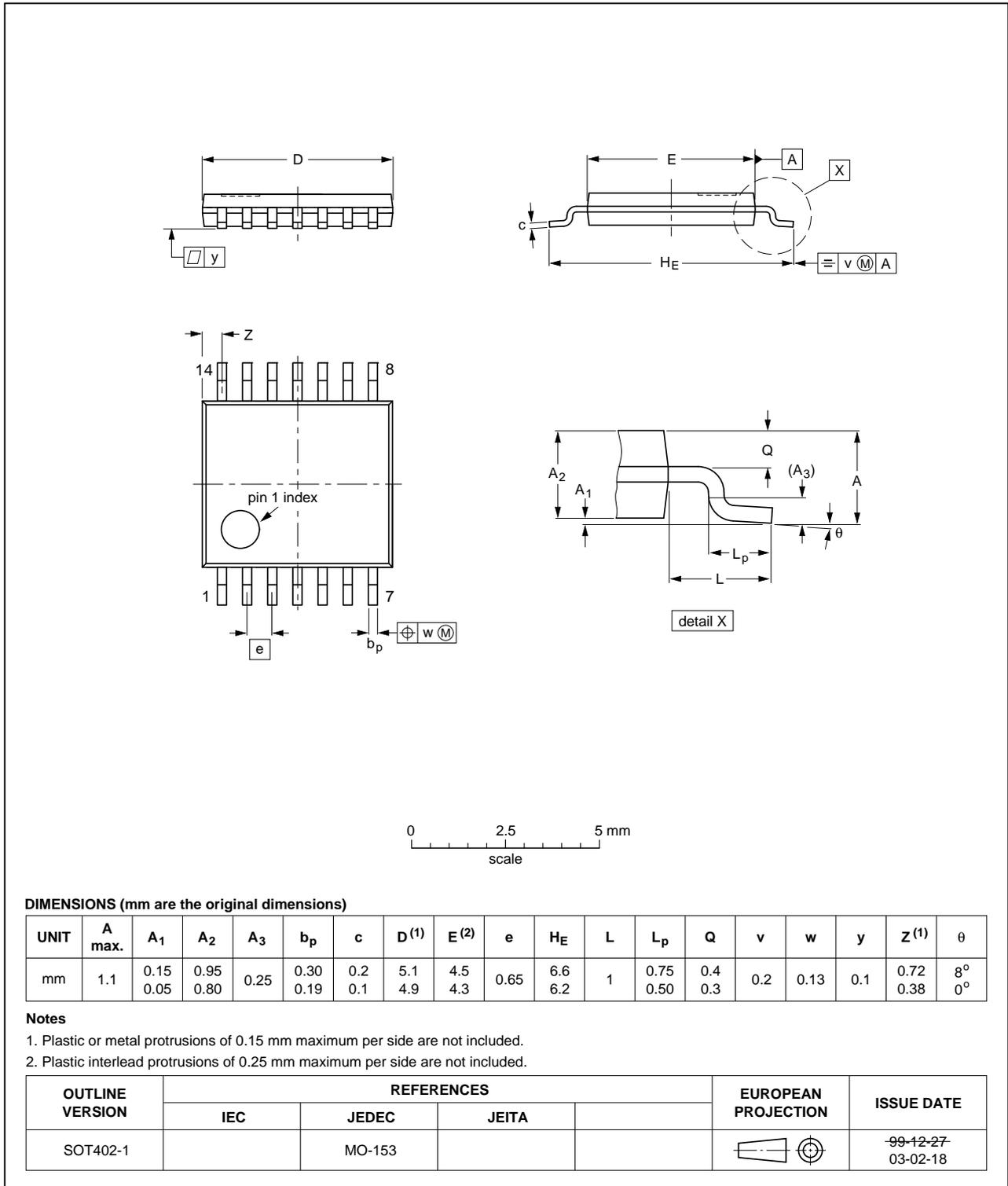


Fig 16. Package outline SOT402-1 (TSSOP14)



## 15. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge Device Model
TTL	Transistor-Transistor Logic

## 16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHCU04 v.4	20151207	Product data sheet	-	74AHCU04 v.3
Modifications:	<ul style="list-style-type: none"> <li>• Descriptive title updated. Added "unbuffered" (errata).</li> </ul>			
74AHCU04 v.3	20071114	Product data sheet	-	74AHCU04 v.2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Section 3</a>: DHVQFN14 package added.</li> <li>• <a href="#">Section 8</a>: derating values added for DHVQFN14 package.</li> <li>• <a href="#">Section 14</a>: outline drawing added for DHVQFN14 package.</li> </ul>			
74AHCU04 v.2	19990927	Product specification	-	74AHCU04 v.1
74AHCU04 v.1	19990226	Product specification	-	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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