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Kind regards,

Team Nexperia

74ALVT16827

20-bit buffer/line driver; non-inverting; 3-state

Rev. 03 — 2 June 2005

Product data sheet

1. General description

The 74ALVT16827 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive. It is designed for V_{CC} operation at 2.5 V or 3.3 V with I/O compatibility to 5 V.

The 74ALVT16827 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($\overline{nOE1}$ and $\overline{nOE2}$) for maximum control flexibility.

2. Features

- Multiple V_{CC} and GND pins minimize switching noise
- 5 V I/O compatible
- Live insertion and extraction permitted
- 3-state output buffers
- Power-up 3-state
- Output capability: +64 mA and –32 mA
- Latch-up protection:
 - ◆ JESD 78 exceeds 500 mA
- ElectroStatic Discharge (ESD) protection:
 - ◆ MIL STD 883 Method 3015: exceeds 2000 V
 - ◆ Machine model: exceeds 200 V
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs

3. Quick reference data

Table 1: Quick reference data

$GND = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay nAx to nYx	$C_L = 50\text{ pF}$; $V_{CC} = 2.5\text{ V}$	1.0	2.0	2.9	ns
		$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	0.7	1.5	2.2	ns
t_{PHL}	propagation delay nAx to nYx	$C_L = 50\text{ pF}$; $V_{CC} = 2.5\text{ V}$	1.0	2.0	3.0	ns
		$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	0.8	1.6	2.3	ns
C_I	input capacitance on DIR, $\overline{OE}$	$V_I = 0\text{ V}$ or V_{CC}	-	3	-	pF

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Table 1: Quick reference data ...continued
GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _O	output capacitance	V _{IO} = 0 V or V _{CC}	-	9	-	pF
I _{CC}	total supply current	outputs disabled; V _{CC} = 2.5 V	-	40	-	μA
		outputs disabled; V _{CC} = 3.3 V	-	70	-	μA

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVT16827DL	−40 °C to +85 °C	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1
74ALVT16827DGG	−40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

5. Functional diagram

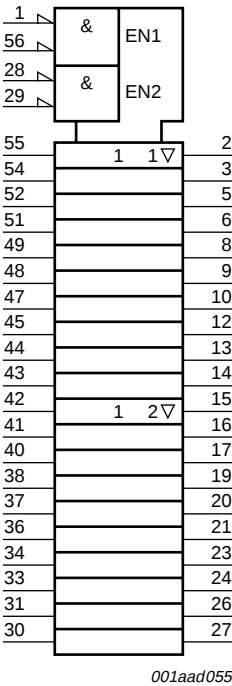


Fig 1. Logic symbol

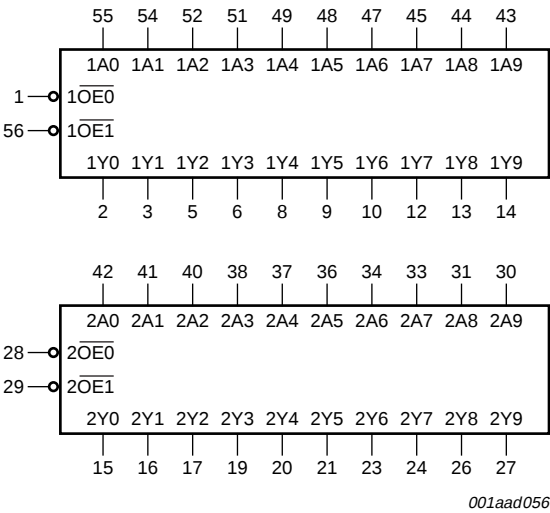


Fig 2. IEC logic symbol

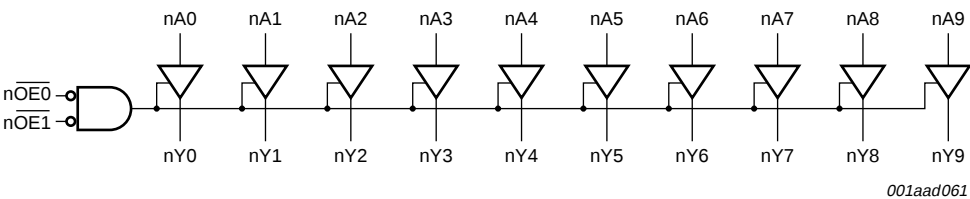


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

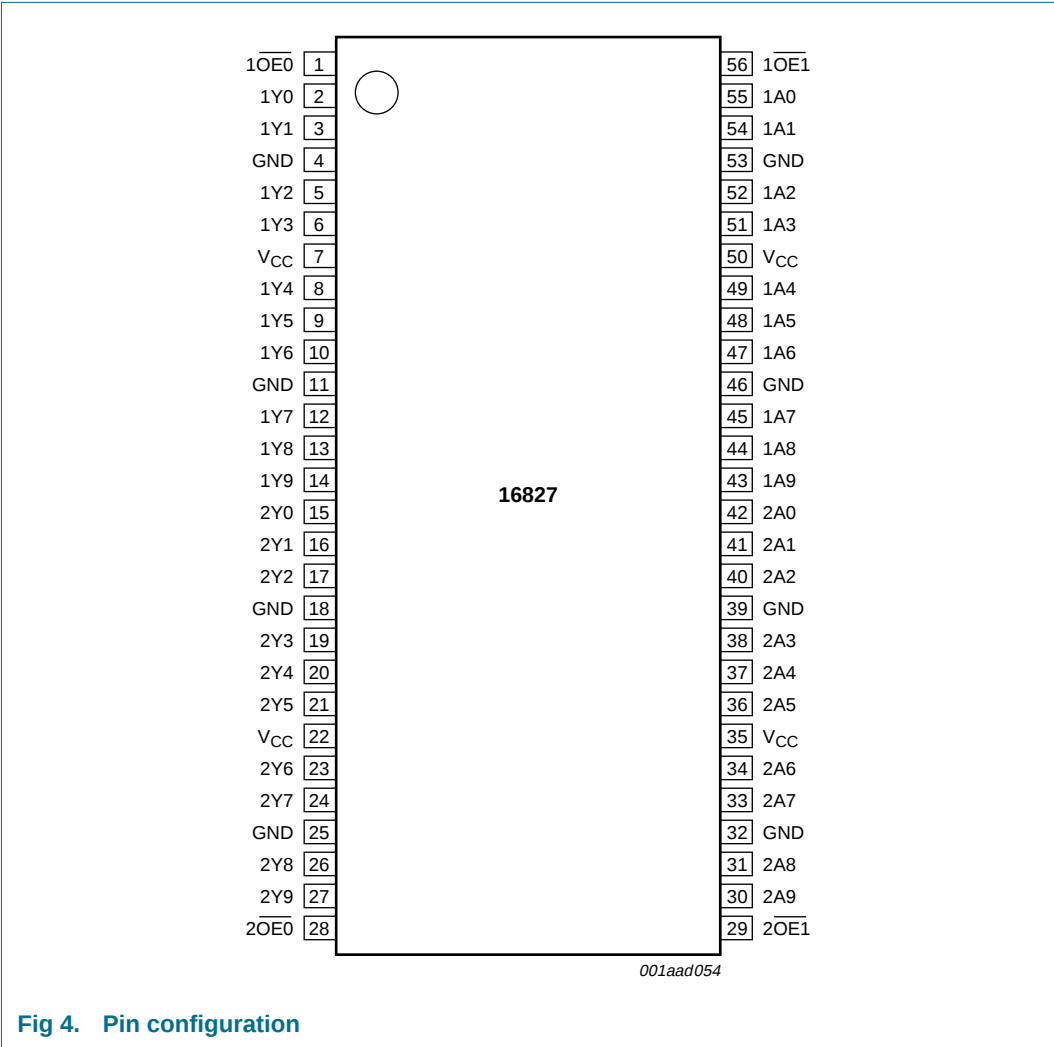


Fig 4. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
$\overline{1OE0}$	1	output enable input (active-LOW)
1Y0	2	data output
1Y1	3	data output
GND	4	ground (0 V)
1Y2	5	data output
1Y3	6	data output
V _{CC}	7	positive voltage supply
1Y4	8	data output
1Y5	9	data output
1Y6	10	data output
GND	11	ground (0 V)
1Y7	12	data output
1Y8	13	data output
1Y9	14	data output
2Y0	15	data output
2Y1	16	data output
2Y2	17	data output
GND	18	ground (0 V)
2Y3	19	data output
2Y4	20	data output
2Y5	21	data output
V _{CC}	22	positive voltage supply
2Y6	23	data output
2Y7	24	data output
GND	25	ground (0 V)
2Y8	26	data output
2Y9	27	data output
$\overline{2OE0}$	28	output enable input (active-LOW)
$\overline{2OE1}$	29	output enable input (active-LOW)
2A9	30	data input
2A8	31	data input
GND	32	ground (0 V)
2A7	33	data input
2A6	34	data input
V _{CC}	35	positive voltage supply
2A5	36	data input
2A4	37	data input
2A3	38	data input
GND	39	ground (0 V)

Table 3: Pin description ...continued

Symbol	Pin	Description
2A2	40	data input
2A1	41	data input
2A0	42	data input
1A9	43	data input
1A8	44	data input
1A7	45	data input
GND	46	ground (0 V)
1A6	47	data input
1A5	48	data input
1A4	49	data input
V _{CC}	50	positive voltage supply
1A3	51	data input
1A2	52	data input
GND	53	ground (0 V)
1A1	54	data input
1A0	55	data input
1 $\overline{\text{OE}}$ 1	56	output enable input (active-LOW)

7. Functional description

7.1 Function table

Table 4: Function table [1]

Input		Output	Operating mode
nOEx	nAx	nYx	
L	L	L	transparent
L	H	H	transparent
H	X	Z	High-impedance

- [1] X = don't care;
 Z = High-impedance OFF-state;
 H = HIGH voltage level;
 L = LOW voltage level.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [2] Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input diode current	V _I < 0 V	-18	-	mA
V _I	input voltage		[2] -1.2	+7.0	V
I _{OK}	output diode current	V _O < 0 V	-50	-	mA

Table 5: Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). ^[1] Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _O	output voltage	output in OFF or HIGH-state	^[2] -0.5	+5.5	V
I _O	output current	output in LOW-state	-	128	mA
T _j	junction temperature		-	150	°C
T _{stg}	storage temperature		-65	+150	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. Exceed 150 °C.

[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC} = 3.3 V ± 0.3 V						
V _{CC}	supply voltage		3.0	-	3.6	V
V _I	input voltage		0	-	5.5	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	input voltage		-	-	0.8	V
I _{OH}	HIGH-level output current		-	-	-32	mA
I _{OL}	LOW-level output current		-	-	32	mA
		current duty cycle ≤ 50 %; f ≥ 1 kHz	-	-	64	mA
Δt/Δv	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
T _{amb}	ambient temperature		-40	-	+85	°C
V_{CC} = 2.5 V ± 0.2 V						
V _{CC}	supply voltage		2.3	-	2.7	V
V _I	input voltage		0	-	5.5	V
V _{IH}	HIGH-level input voltage		1.7	-	-	V
V _{IL}	input voltage		-	-	0.7	V
I _{OH}	HIGH-level output current		-	-	-8	mA
I _{OL}	LOW-level output current		-	-	8	mA
		current duty cycle ≤ 50 %; f ≥ 1 kHz	-	-	24	mA
Δt/Δv	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
T _{amb}	ambient temperature		-40	-	+85	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referred to GND (ground = 0 V). $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ [4]						
V_{IK}	input clamp voltage	$V_{CC} = 3.0\text{ V}$; $I_{IK} = -18\text{ mA}$	-	-0.85	-1.2	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 3.0\text{ V}$ to 3.6 V ; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	V_{CC}	-	V
		$V_{CC} = 3.0\text{ V}$; $I_{OH} = -32\text{ mA}$	2.0	2.3	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 3.0\text{ V}$				
		$I_{OL} = 100\text{ }\mu\text{A}$	[2] -	0.07	0.2	V
		$I_{OL} = 16\text{ mA}$	[2] -	0.25	0.4	V
		$I_{OL} = 32\text{ mA}$	[2] -	0.3	0.5	V
I_{LI}	input leakage current	$I_{OL} = 64\text{ mA}$	[2] -	0.4	0.55	V
		control pins				
		$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND	-	0.1	± 1	μA
		$V_{CC} = 0\text{ V}$ or 3.6 V ; $V_I = 5.5\text{ V}$	-	0.1	10	μA
	I/O data pins	$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$	[2] -	0.5	1	μA
		$V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V}$	[2] -	+0.1	-5	μA
I_{OFF}	off current	$V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V}$ to 4.5 V	-	0.1	± 100	μA
I_{HOLD}	bus hold current data inputs	$V_{CC} = 3\text{ V}$; $V_I = 0.8\text{ V}$	[3] 75	130	-	μA
		$V_{CC} = 3\text{ V}$; $V_I = 2.0\text{ V}$	[3] -75	-140	-	μA
		$V_{CC} = 0\text{ V}$ to 3.6 V ; $V_{CC} = 3.6\text{ V}$	[3] ± 500	-	-	μA
I_{EX}	current into an output in the HIGH-state when $V_O > V_{CC}$	$V_O = 5.5\text{ V}$; $V_{CC} = 3.0\text{ V}$	-	10	125	μA
I_{PU}, I_{PD}	power-up/down 3-state output current	$V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; $\overline{\text{OE}} = \text{don't care}$	[4] -	1	± 100	μA
I_{OZ}	3-state output current	$V_{CC} = 3.6\text{ V}$; $V_I = V_{IL}$ or V_{IH}				
		output HIGH; $V_O = 3.0\text{ V}$	-	0.5	5	μA
		output LOW; $V_O = 0.5\text{ V}$	-	+0.5	-5	μA
I_{CC}	quiescent supply current	$V_{CC} = 3.6\text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$				
		outputs HIGH	-	0.07	0.1	mA
		outputs LOW	-	4.2	6	mA
		outputs disabled	[5] -	0.07	0.1	mA
ΔI_{CC}	additional supply current per input pin	$V_{CC} = 3\text{ V}$ to 3.6 V ; one input at $V_{CC} - 0.6\text{ V}$, other inputs at V_{CC} or GND	[6] -	0.04	0.4	mA
C_I	input capacitance	$V_I = 0\text{ V}$ or V_{CC}	-	3	-	pF
C_O	output capacitance	$V_{IO} = 0\text{ V}$ or V_{CC}	-	9	-	pF

Table 7: Static characteristics ...continuedAt recommended operating conditions; voltages are referred to GND (ground = 0 V). $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ [1]						
V_{IK}	input clamp voltage	$V_{CC} = 2.3\text{ V}$; $I_{IK} = -18\text{ mA}$	-	-0.85	-1.2	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 2.3\text{ V}$ to 2.7 V ; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	V_{CC}	-	V
		$V_{CC} = 2.3\text{ V}$; $I_{OH} = -8\text{ mA}$	1.8	2.1	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 2.3\text{ V}$				
		$I_{OL} = 100\text{ }\mu\text{A}$	-	0.07	0.2	V
		$I_{OL} = 24\text{ mA}$	-	0.3	0.5	V
		$I_{OL} = 100\text{ }\mu\text{A}$	-	0.07	0.2	V
I_{LI}	input leakage current	$V_{CC} = 2.3\text{ V}$; $I_{OL} = 24\text{ mA}$	-	0.3	0.5	V
	control pins	$V_{CC} = 2.7\text{ V}$; $V_I = V_{CC}$ or GND	-	0.1	± 1	μA
	I/O data pins	$V_{CC} = 0\text{ V}$ or 2.7 V ; $V_I = 5.5\text{ V}$	[2] -	0.1	10	μA
		$V_{CC} = 2.7\text{ V}$; $V_I = V_{CC}$	[2] -	0.1	1	μA
		$V_{CC} = 2.7\text{ V}$; $V_I = 0\text{ V}$	[2] -	+0.1	-5	μA
I_{OFF}	off current	$V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V}$ to 4.5 V	-	0.1	± 100	μA
I_{HOLD}	bus hold current data inputs	$V_{CC} = 2.5\text{ V}$; $V_I = 0.8\text{ V}$	[3] -	115	-	μA
		$V_{CC} = 2.5\text{ V}$; $V_I = 2.0\text{ V}$	[3] -	-10	-	μA
I_{EX}	current into an output in the HIGH-state when $V_O > V_{CC}$	$V_O = 5.5\text{ V}$; $V_{CC} = 2.3\text{ V}$	-	10	125	μA
I_{PU}, I_{PD}	power-up/down 3-state output current	$V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; $n\text{OE}x = \text{don't care}$	[4] -	1	100	μA
I_{OZ}	3-state output current	$V_{CC} = 2.7\text{ V}$; $V_O = 2.3\text{ V}$; $V_I = V_{IL}$ or V_{IH}				
		output HIGH; $V_O = 2.3\text{ V}$	-	0.5	5	μA
		output LOW; $V_O = 0.5\text{ V}$	-	+0.5	-5	μA
I_{CC}	quiescent supply current	$V_{CC} = 2.7\text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$				
		outputs HIGH	-	0.04	0.1	mA
		outputs LOW	-	3.6	5.0	mA
		outputs disabled	[5] -	0.04	0.1	mA
ΔI_{CC}	additional supply current per input pin	$V_{CC} = 2.3\text{ V}$ to 2.7 V ; one input at $V_{CC} - 0.6\text{ V}$, other inputs at V_{CC} or GND	[6] -	0.04	0.4	mA

[1] All typical values are at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25^{\circ}\text{C}$.[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ a transition time of 100 μs is permitted. This parameter is valid for $T_{amb} = 25^{\circ}\text{C}$ only.[5] I_{CC} is measured with outputs pulled up to V_{CC} or pulled down to ground.[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.[7] All typical values are at $V_{CC} = 2.5\text{ V}$ and $T_{amb} = 25^{\circ}\text{C}$.

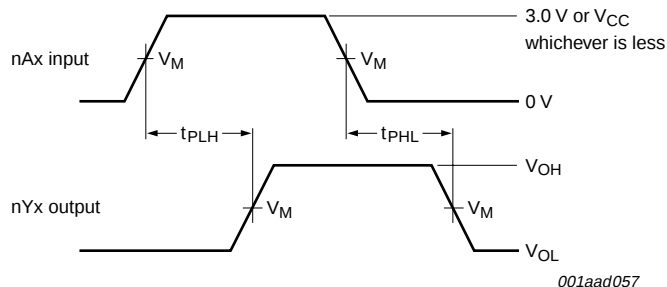
11. Dynamic characteristics

Table 8: Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f = 2.5\text{ ns}$; $C_L = 50\text{ pF}$; $R_L = 500\text{ }\Omega$; $T_{amb} = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$						
t_{PLH}	propagation delay nAx to nYx	see Figure 5	0.7	1.5	2.2	ns
t_{PHL}	propagation delay nAx to nYx	see Figure 5	0.8	1.6	2.3	ns
t_{PZH}	output enable time to HIGH-level	see Figure 6	1.6	2.6	3.8	ns
t_{PZL}	output enable time to LOW-level	see Figure 6	1.4	2.3	3.2	ns
t_{PHZ}	output disable time from HIGH-level	see Figure 6	2.3	3.2	4.8	ns
t_{PLZ}	output disable time from LOW-level	see Figure 6	1.5	2.5	3.8	ns
$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$						
t_{PLH}	propagation delay nAx to nYx	see Figure 5	1.0	2.0	2.9	ns
t_{PHL}	propagation delay nAx to nYx	see Figure 5	1.0	2.0	3.0	ns
t_{PZH}	output enable time to HIGH-level	see Figure 6	2.0	3.2	5.5	ns
t_{PZL}	output enable time to LOW-level	see Figure 6	1.7	2.9	4.3	ns
t_{PHZ}	output disable time from HIGH-level	see Figure 6	1.8	2.8	5.1	ns
t_{PLZ}	output disable time from LOW-level	see Figure 6	1.4	2.3	3.9	ns

12. AC waveforms



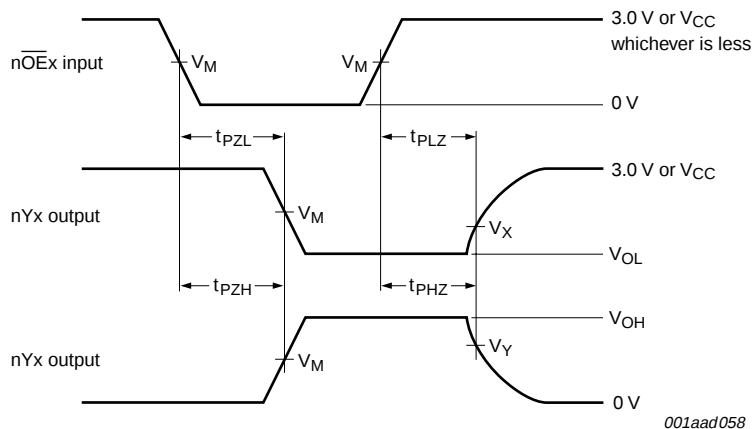
$V_M = 1.5 \text{ V}$ for $V_{CC} \geq 3.0 \text{ V}$; $V_M = V_{CC}/2$ for $V_{CC} \leq 2.7 \text{ V}$.

$V_X = V_{OL} + 0.3 \text{ V}$ for $V_{CC} \geq 3.0 \text{ V}$; $V_X = V_{OL} + 0.15 \text{ V}$ for $V_{CC} \leq 2.7 \text{ V}$.

$V_Y = V_{OH} - 0.3 \text{ V}$ for $V_{CC} \geq 3.0 \text{ V}$; $V_Y = V_{OH} - 0.15 \text{ V}$ for $V_{CC} \leq 2.7 \text{ V}$.

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Fig 5. The input (nAx) to output (nYx) propagation delays



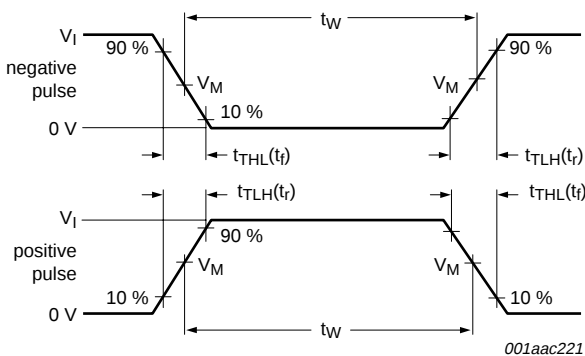
$V_M = 1.5 \text{ V}$ for $V_{CC} \geq 3.0 \text{ V}$; $V_M = V_{CC}/2$ for $V_{CC} \leq 2.7 \text{ V}$.

$V_X = V_{OL} + 0.3 \text{ V}$ for $V_{CC} \geq 3.0 \text{ V}$; $V_X = V_{OL} + 0.15 \text{ V}$ for $V_{CC} \leq 2.7 \text{ V}$.

$V_Y = V_{OH} - 0.3 \text{ V}$ for $V_{CC} \geq 3.0 \text{ V}$; $V_Y = V_{OH} - 0.15 \text{ V}$ for $V_{CC} \leq 2.7 \text{ V}$.

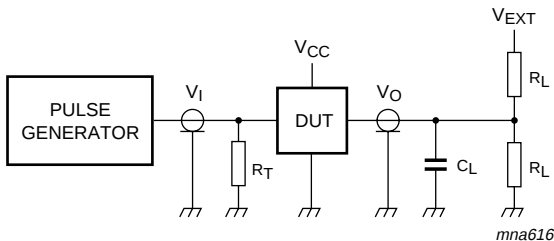
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Fig 6. The 3-state output enable and disable times



$V_M = 1.5\text{ V}$.

a. Input pulse definition



Test data is given in [Table 9](#).
Definitions test circuit:
 R_L = Load resistor.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = Test voltage for switching times.

b. Test circuit

Fig 7. Load circuitry for switching times

Table 9: Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V or V_{CC} whichever is less	$\leq 10\text{ MHz}$	500 ns	$\leq 2.5\text{ ns}$	50 pF	500 Ω	6 V or $V_{CC} \times 2$	open	GND

13. Package outline

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

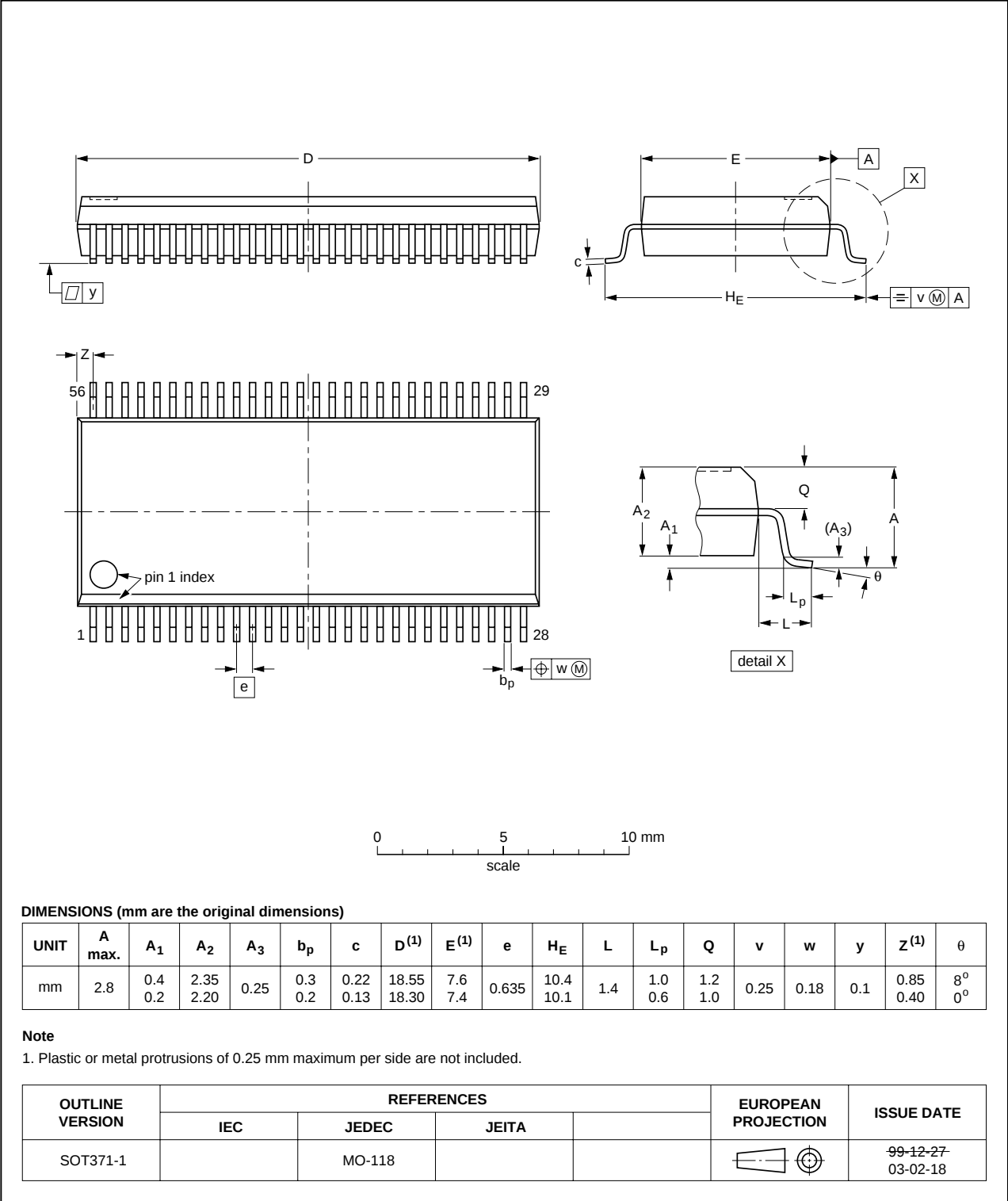


Fig 8. Package outline SOT371-1 (SSOP56)

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

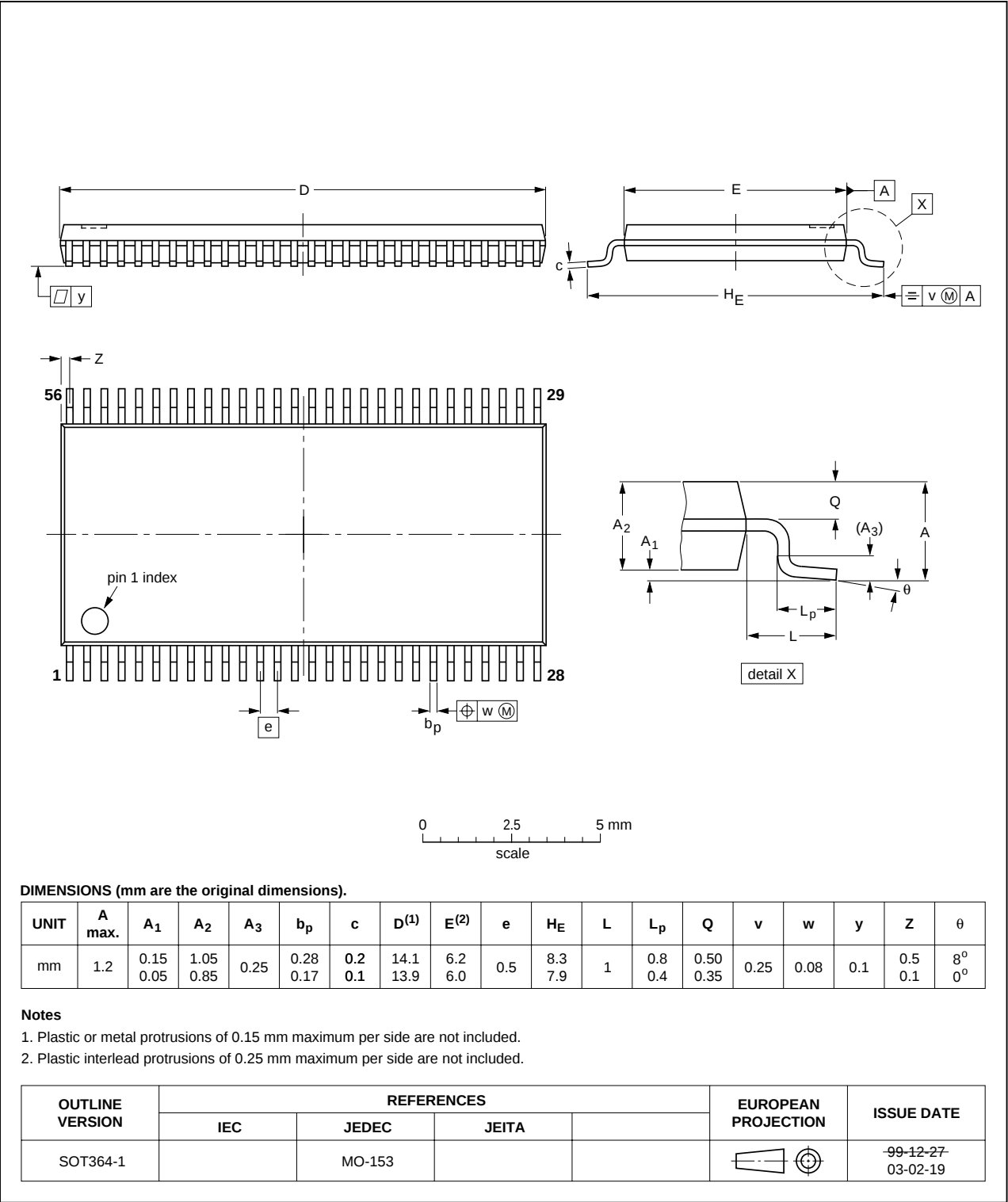


Fig 9. Package outline SOT364-1 (TSSOP56)

14. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74ALVT16827_3	20050602	Product data sheet	-	9397 750 15122	74ALVT16827_2
Modifications:					
- The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Section 2 “Features”: modified ‘JEDEC Std 17’ into ‘JESD78’. Section 11 “Dynamic characteristics”: changed values in column ‘min’					

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