

74AUP1G57

TinyLogic® Low Power Universal Configurable Two-Input Logic Gate

Features

- 0.8V to 3.6V V_{CC} Supply Operation
- 3.6V Over-Voltage Tolerant I/Os at V_{CC} from 0.8V to 3.6V
- High Speed t_{PD}
 - 2.9ns: Typical at 3.3V
- Power-Off High-Impedance Inputs and Outputs
- Low Static Power Consumption
 - I_{CC} =0.9 μ A Maximum
- Low Dynamic Power Consumption
 - C_{PD} =2.9pF Typical at 3.3V
- Ultra-Small MicroPak™ Packages

Description

The 74AUP1G57 is a universal configurable 2-input logic gate that provides a high performance and low power solution ideal for battery-powered portable applications. This product is designed for a wide low voltage operating range (0.8V to 3.6V) and guarantees very low static and dynamic power consumption across the entire voltage range. All inputs are implemented with hysteresis to allow for slower transition input signals and better switching noise immunity.

The 74AUP1G57 provides for multiple functions as determined by various configurations of the three inputs. The potential logic functions provided are AND, NAND, OR, NOR, and XNOR, inverter and buffer. Refer to Figures 2 to 8.

Ordering Information

Part Number	Top Mark	Package	Packing Method
74AUP1G57L6X	AB	6-Lead Micropak™, 1.0mm Wide	5000 Units on Tape & Reel
74AUP1G57FHX	AB	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel

Pin Configurations

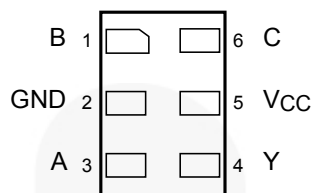


Figure 1. MicroPak™ (Top Through View)

Pin Definitions

Pin #	Name	Description
1	B	Data Input
2	GND	Ground
3	A	Data Input
4	Y	Output
5	V _{CC}	Supply Voltage
6	C	Data Input

Function Table

Inputs			74AUP1G57
C	B	A	Y=Output
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

H = HIGH Logic Level

L = LOW Logic Level

Function Selection Table

2-Input Logic Function	Connection Configuration
2-Input AND	Figure 2
2-Input AND with Both Inputs Inverted	Figure 5
2-Input NAND with Inverted Input	Figure 3, Figure 4
2-Input OR with Inverted Input	Figure 3, Figure 4
2-Input NOR	Figure 5
2-Input NOR with Both Inputs Inverted	Figure 2
2-Input XNOR	Figure 6
Inverter	Figure 7
Buffer	Figure 8

74AUP1G57 Logic Configurations

Figure 2 through Figure 8 show the logical functions that can be implemented using the 74AUP1G57. The diagrams show the DeMorgan's equivalent logic duals for a given two-input function. The logical

implementation is next to the board-level physical implementation of how the pins of the function should be connected.

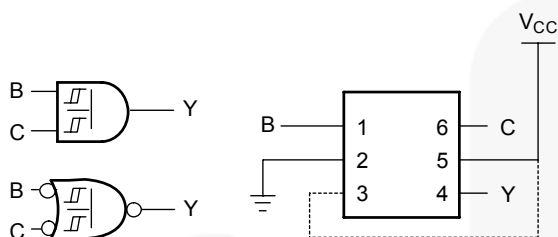


Figure 2. 2-Input AND Gate or 2-Input NOR Gate with Both Inputs Inverted

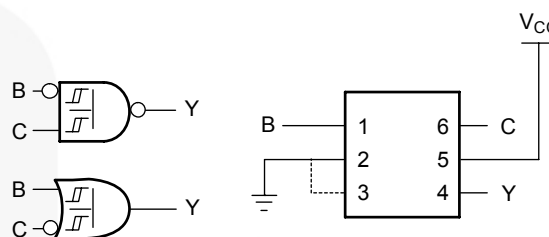


Figure 3. 2-Input NAND with Inverted B Input or 2-Input OR Gate with Inverted C Input

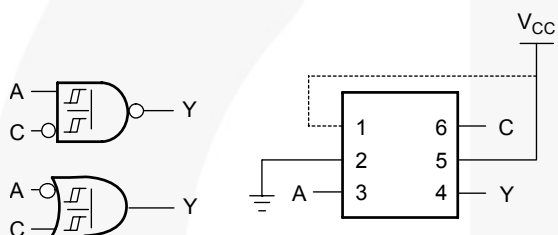


Figure 4. 2-Input NAND with Inverted C Input or 2-Input OR Gate with Inverted A Input

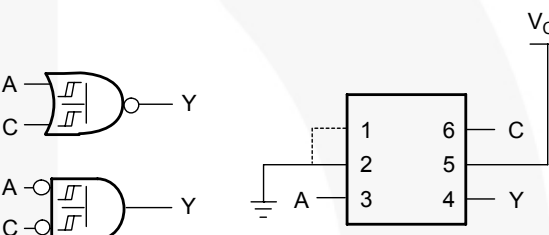


Figure 5. 2-Input NOR Gate or 2-Input AND Gate with Both Inputs Inverted

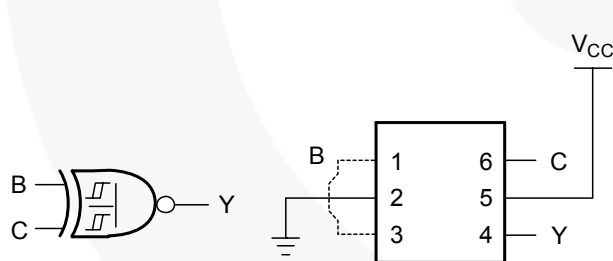


Figure 6. 2-Input XNOR Gate

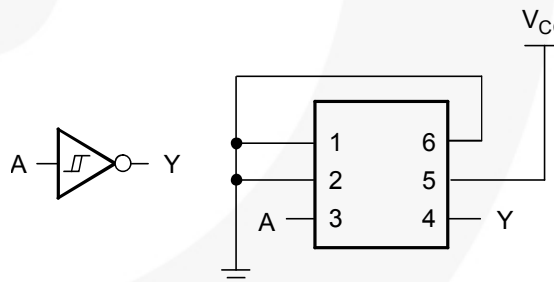


Figure 7. Inverter

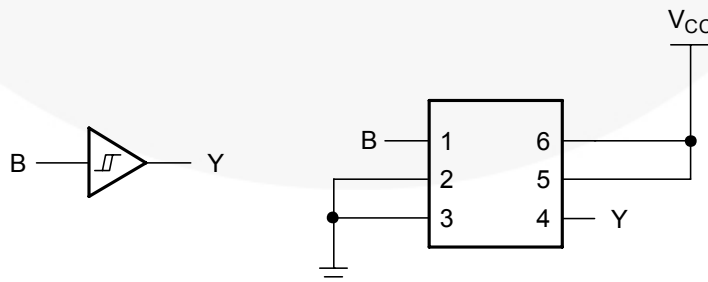


Figure 8. Non-Inverter Buffer

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	4.6	V
V_{IN}	DC Input Voltage	-0.5	4.6	V
V_{OUT}	DC Output Voltage	HIGH or LOW State ⁽¹⁾	$V_{CC} + 0.5$	V
		$V_{CC}=0V$	4.6	
I_{IK}	DC Input Diode Current	$V_{IN} < 0V$	-50	mA
I_{OK}	DC Output Diode Current	$V_{OUT} < 0V$	-50	mA
		$V_{OUT} > V_{CC}$	+50	
I_{OH} / I_{OL}	DC Output Source / Sink Current		±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin		±50	mA
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Junction Temperature Under Bias		+150	°C
T_L	Junction Lead Temperature, Soldering 10s		+260	°C
P_D	Power Dissipation at +85°C	MicroPak-6	130	mW
		MicroPak2-6	120	
ESD	Human Body Model, JEDEC:JESD22-A114		5000+	V
	Charged Device Model, JEDEC:JESD22-C101		2000	

Note:

1. I_O absolute maximum rating must be observed.

Recommended Operating Conditions⁽²⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage		0.8	3.6	V
V_{IN}	Input Voltage		0	3.6	V
V_{OUT}	Output Voltage	$V_{CC}=0V$	0	3.6	V
		HIGH or LOW State	0	V_{CC}	
I_{OH}/I_{OL}	Output Current	$V_{CC}=3.0V$ to $3.6V$		±4.0	mA
		$V_{CC}=2.3V$ to $2.7V$		±3.1	
		$V_{CC}=1.65V$ to $1.95V$		±1.9	
		$V_{CC}=1.4V$ to $1.6V$		±1.7	
		$V_{CC}=1.1V$ to $1.3V$		±1.1	
		$V_{CC}=0.8V$		±20.0	µA
T_A	Operating Temperature, Free Air		-40	+85	°C
θ_{JA}	Thermal Resistance	MicroPak-6		500	°C/W
		MicroPak2-6		560	

Note:

2. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC}	Conditions	T _A =+25°C		T _A =-40 to +85°C		Units
				Min.	Max.	Min.	Max.	
V _P	Positive Threshold Voltage	0.80		0.30	0.60	0.30	0.60	V
		1.10		0.53	0.90	0.53	0.90	
		1.40		0.74	1.11	0.74	1.11	
		1.65		0.91	1.29	0.91	1.29	
		2.30		1.37	1.77	1.37	1.77	
		3.00		1.88	2.29	1.88	2.29	
V _N	Negative Threshold Voltage	0.80		0.10	0.60	0.10	0.60	V
		1.10		0.26	0.65	0.26	0.65	
		1.40		0.39	0.75	0.39	0.75	
		1.65		0.47	0.84	0.47	0.84	
		2.30		0.69	1.04	0.69	1.04	
		3.00		0.88	1.24	0.88	1.24	
V _H	Hysteresis Voltage	0.80		0.07	0.50	0.07	0.50	V
		1.10		0.08	0.46	0.08	0.46	
		1.40		0.18	0.56	0.18	0.56	
		1.65		0.27	0.66	0.27	0.66	
		2.30		0.53	0.92	0.53	0.92	
		3.00		0.79	1.31	0.79	1.31	
V _{OH}	HIGH Level Output Voltage	0.80 ≤ V _{CC} ≤ 3.60	I _{OH} =-20μA	V _{CC} -0.1		V _{CC} -0.1		V
		1.10 ≤ V _{CC} ≤ 1.30	I _{OH} =-1.1mA	0.75 x V _{CC}		0.70 x V _{CC}		
		1.40 ≤ V _{CC} ≤ 1.60	I _{OH} =-1.7mA	1.11		1.03		
		1.65 ≤ V _{CC} ≤ 1.95	I _{OH} =-1.9mA	1.32		1.30		
		2.30 ≤ V _{CC} ≤ 2.70	I _{OH} =-2.3mA	2.05		1.97		
			I _{OH} =-3.1mA	1.90		1.85		
		3.00 ≤ V _{CC} ≤ 3.60	I _{OH} =-2.7mA	2.72		2.67		
			I _{OH} =-4.0mA	2.60		2.55		
V _{OL}	LOW Level Output Voltage	0.80 ≤ V _{CC} ≤ 3.60	I _{OL} =20μA		0.10		0.10	V

AC Electrical Characteristics

Symbol	Parameter	V _{CC}	Conditions	T _A =+25°C			T _A =-40 to +85°C		Units	Figure
				Min.	Typ.	Max	Min.	Max.		
t _{PHL} , t _{PLH}	Propagation Delay	0.80	C _L =5pF, R _L =1MΩ		22.1				ns	Figure 9 Figure 10
		1.10 ≤ V _{CC} ≤ 1.30		2.5	6.5	12.6	2.5	13.0		
		1.40 ≤ V _{CC} ≤ 1.60		2.2	4.6	7.6	2.2	8.2		
		1.65 ≤ V _{CC} ≤ 1.95		2.0	3.9	6.2	2.0	6.8		
		2.30 ≤ V _{CC} ≤ 2.70		1.7	3.1	4.5	1.7	5.1		
		3.00 ≤ V _{CC} ≤ 3.60		1.3	2.9	3.9	1.3	4.1		
		0.80	C _L =10pF, R _L =1MΩ		27.1					
		1.10 ≤ V _{CC} ≤ 1.30		3.2	7.6	14.4	2.8	14.9		
		1.40 ≤ V _{CC} ≤ 1.60		2.6	5.3	8.7	2.8	9.3		
		1.65 ≤ V _{CC} ≤ 1.95		2.2	4.6	7.0	2.2	7.8		
		2.30 ≤ V _{CC} ≤ 2.70		1.9	3.7	5.2	1.9	5.9		
		3.00 ≤ V _{CC} ≤ 3.60		1.3	2.8	4.6	1.3	4.9		
		0.80	C _L =15pF, R _L =1MΩ		32.6					
		1.10 ≤ V _{CC} ≤ 1.30		3.4	8.3	15.7	3.1	16.7		
		1.40 ≤ V _{CC} ≤ 1.60		2.8	5.8	9.4	3.1	10.4		
		1.65 ≤ V _{CC} ≤ 1.95		2.5	5.1	7.9	2.5	8.7		
		2.30 ≤ V _{CC} ≤ 2.70		2.1	4.0	6.1	2.1	6.9		
		3.00 ≤ V _{CC} ≤ 3.60		1.3	3.2	5.0	1.3	5.5		
		0.80	C _L =30pF, R _L =1MΩ		25.4					
		1.10 ≤ V _{CC} ≤ 1.30		3.4	8.6	18.5	3.4	19.0		
		1.40 ≤ V _{CC} ≤ 1.60		3.1	5.5	10.5	3.1	11.0		
		1.65 ≤ V _{CC} ≤ 1.95		2.1	4.5	8.7	2.1	9.5		
		2.30 ≤ V _{CC} ≤ 2.70								

AC Loadings and Waveforms

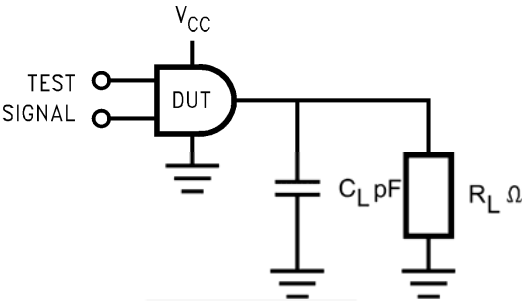


Figure 9. AC Test Circuit

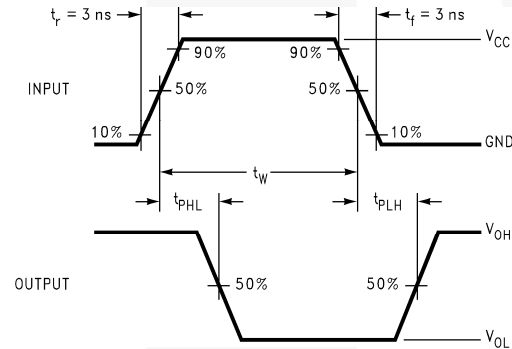
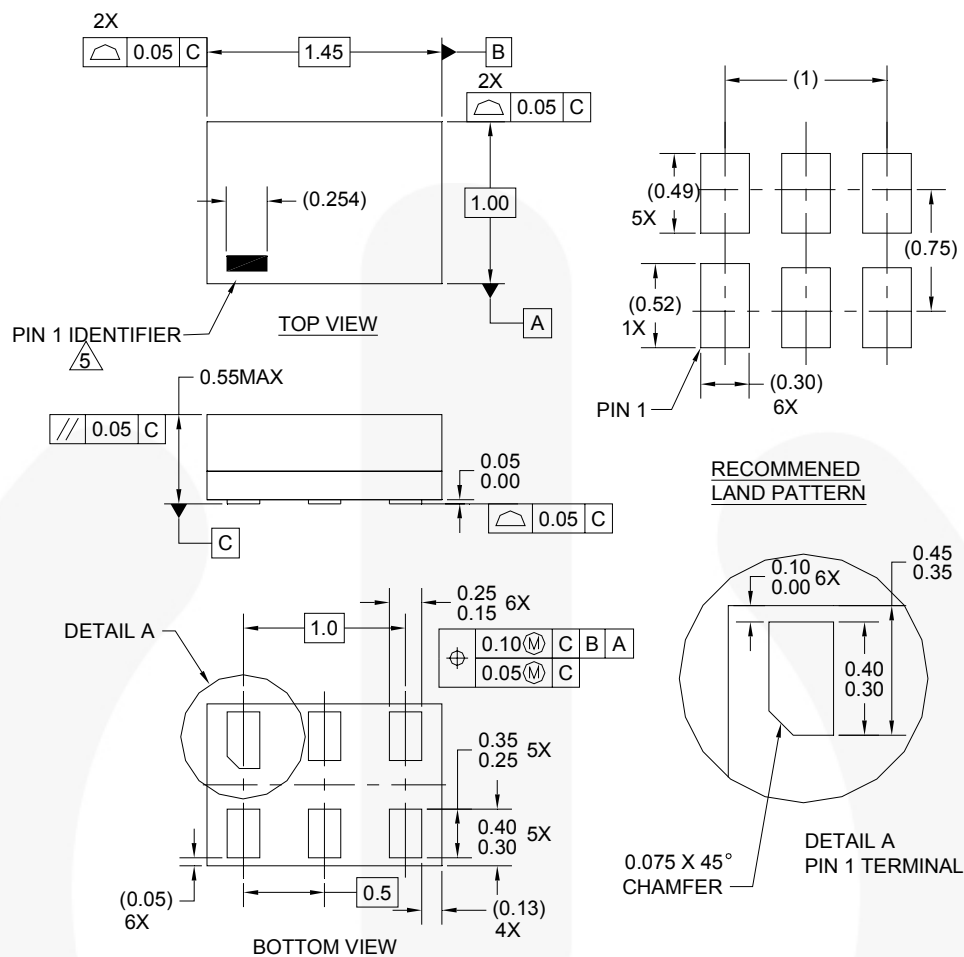


Figure 10. AC Waveforms

Symbol	V _{CC}					
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V	1.5V ± 0.10V	1.2V ± 0.10V	0.8V
V _{mi}	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V _{mo}	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2

Physical Dimensions



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

Figure 11. 6-Lead, MicroPak™, 1.0mm Wide

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions

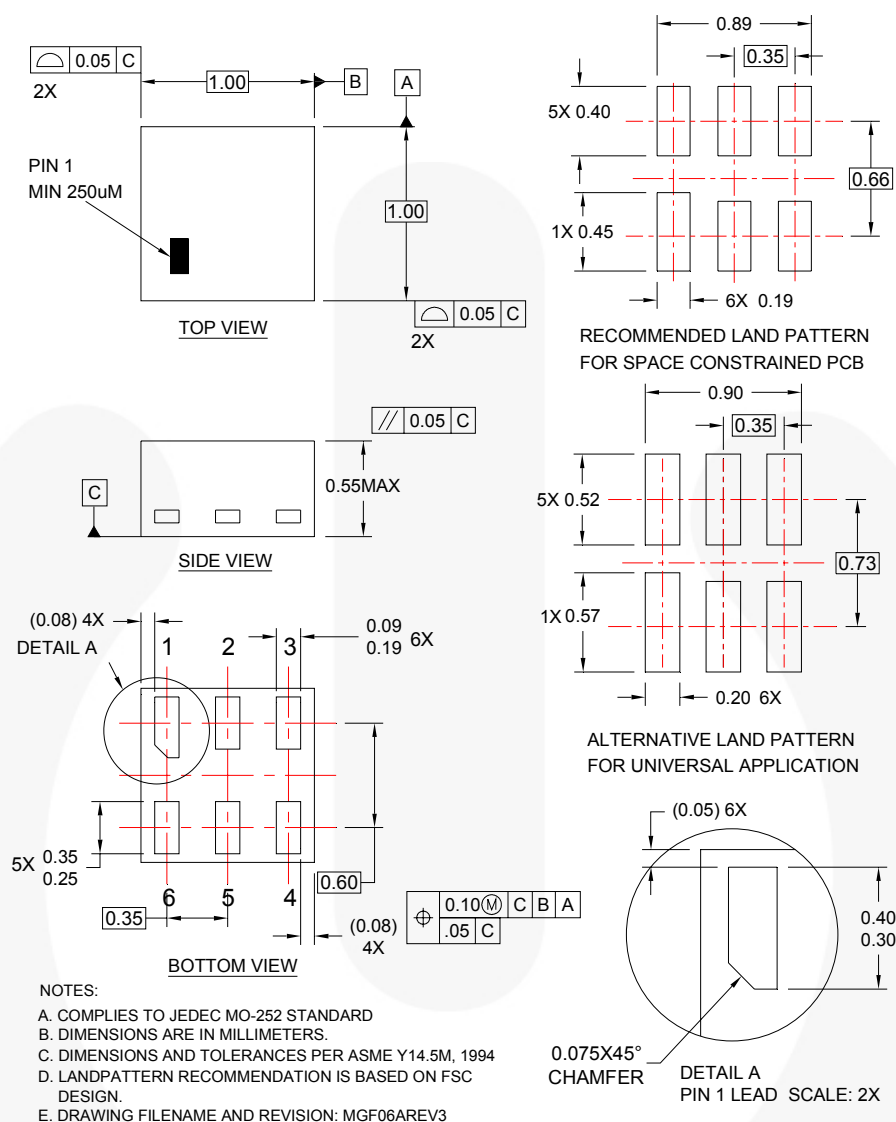


Figure 12. 6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



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