

74CBTLV3257

Quad 1-of-2 multiplexer/demultiplexer

Rev. 5 — 11 November 2016

Product data sheet

1. General description

The 74CBTLV3257 provides a quad 1-of-2 high-speed multiplexer/demultiplexer with common select (S) and output enable ($\overline{OE}$) inputs. The low ON resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. When pin $\overline{OE}$ = LOW, one of the two switches is selected (low-impedance ON-state) with pin S. When pin $\overline{OE}$ = HIGH, all switches are in the high-impedance OFF-state, independent of pin S.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 2.3 V to 3.6 V.

To ensure the high-impedance OFF-state during power-up or power-down, $\overline{OE}$ should be tied to the V_{CC} through a pull-up resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM AEC-Q100-011 revision B exceeds 1000 V
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$



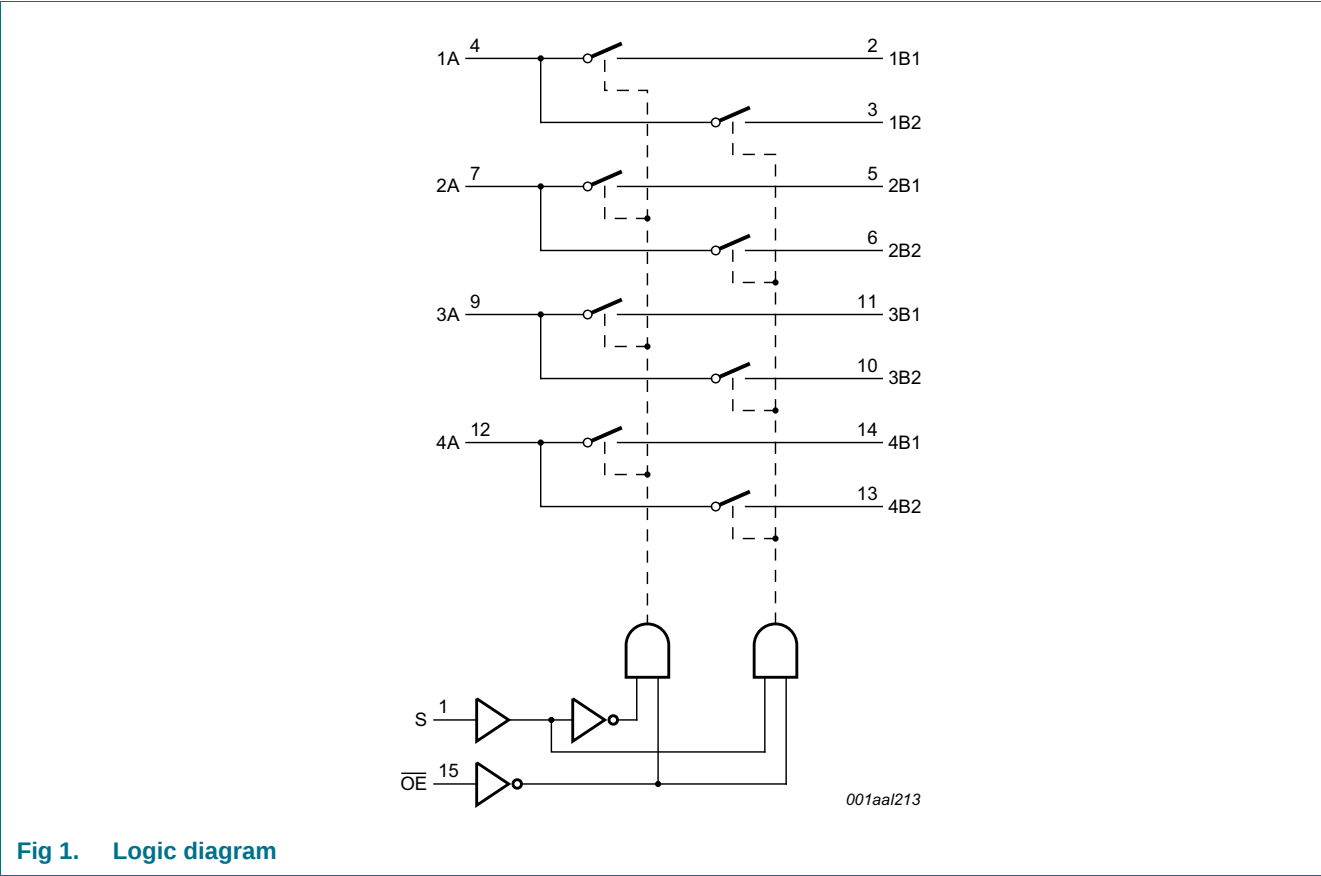
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74CBTLV3257D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74CBTLV3257DS	−40 °C to +125 °C	SSOP16 ^[1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
74CBTLV3257PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74CBTLV3257BQ	−40 °C to +125 °C	DHVQFN16	plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

[1] Also known as QSOP16.

4. Functional diagram



5. Pinning information

5.1 Pinning

74CBTLV3257

Pin 1: S, Pin 2: 1B1, Pin 3: 1B2, Pin 4: 1A, Pin 5: 2B1, Pin 6: 2B2, Pin 7: 2A, Pin 8: GND, Pin 9: 3A, Pin 10: 3B2, Pin 11: 3B1, Pin 12: 4A, Pin 13: 4B2, Pin 14: 4B1, Pin 15: OE, Pin 16: VCC

001aal214

74CBTLV3257

Pin 1: S, Pin 2: 1B1, Pin 3: 1B2, Pin 4: 1A, Pin 5: 2B1, Pin 6: 2B2, Pin 7: 2A, Pin 8: GND, Pin 9: 3A, Pin 10: 3B2, Pin 11: 3B1, Pin 12: 4A, Pin 13: 4B2, Pin 14: 4B1, Pin 15: OE, Pin 16: VCC

001aal215

74CBTLV3257

terminal 1 index area

Pin 1: S, Pin 2: 1B1, Pin 3: 1B2, Pin 4: 1A, Pin 5: 2B1, Pin 6: 2B2, Pin 7: 2A, Pin 8: GND, Pin 9: 3A, Pin 10: 3B2, Pin 11: 3B1, Pin 12: 4A, Pin 13: 4B2, Pin 14: 4B1, Pin 15: OE, Pin 16: VCC

GND(1)

001aal216

Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 2. Pin configuration SOT109-1 (SO16) and SOT519-1 (SSOP16)

Fig 3. Pin configuration SOT403-1 (TSSOP16)

Fig 4. Pin configuration SOT763-1 (DHVQFN16)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	select input
1B1 to 4B1	2, 5, 11, 14	B1 input/output
1B2 to 4B2	3, 6, 10, 13	B2 input/output
1A to 4A	4, 7, 9, 12	A input/output
GND	8	ground (0 V)
OE	15	output enable input (active LOW)
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table^[1]

Inputs		Function switch
OE	S	
L	L	nA = nB1
L	H	nA = nB2
H	X	disconnect nA and nBn

[1] H = HIGH voltage level; L = LOW voltage level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	control inputs ^[1]	-0.5	+4.6	V
V _{SW}	switch voltage	enable and disable mode ^[2]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < -0.5 V	-50	-	mA
I _{SK}	switch clamping current	V _I < -0.5 V	-50	-	mA
I _{SW}	switch current	V _{SW} = 0 V to V _{CC}	-	±128	mA
I _{CC}	supply current		-	+100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C ^[3]	-	500	mW

[1] The minimum input voltage rating may be exceeded if the input clamping current ratings are observed.

[2] The switch voltage ratings may be exceeded if switch clamping current ratings are observed

[3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN16 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		2.3	3.6	V
V _I	input voltage		0	3.6	V
V _{SW}	switch voltage	enable and disable mode	0	V _{CC}	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.3 V to 3.6 V ^[1]	0	200	ns/V

[1] Applies to control signal levels.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = −40 °C to +85 °C			T _{amb} = −40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
I _I	input leakage current	pin $\overline{\text{OE}}$, S; V _I = GND to V _{CC} ; V _{CC} = 3.6 V	-	-	±1	-	±20	μA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 3.6 V; see Figure 5	-	-	±1	-	±20	μA
I _{S(ON)}	ON-state leakage current	V _{CC} = 3.6 V; see Figure 6	-	-	±1	-	±20	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±10	-	±50	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V	-	-	10	-	50	μA
ΔI _{CC}	additional supply current	pin $\overline{\text{OE}}$, S; V _I = V _{CC} − 0.6 V; [2] V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V	-	-	300	-	2000	μA
C _I	input capacitance	pin $\overline{\text{OE}}$, S; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	0.9	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	5.2	-	-	-	pF
C _{S(ON)}	ON-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	14.3	-	-	-	pF

[1] All typical values are measured at $T_{\text{amb}} = 25^\circ\text{C}$.

[2] One input at 3 V, other inputs at V_{CC} or GND.

9.1 Test circuits

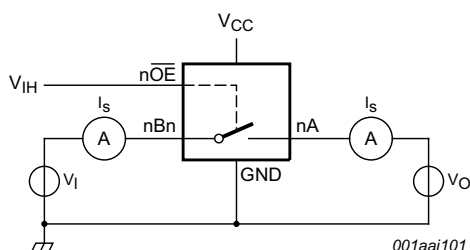
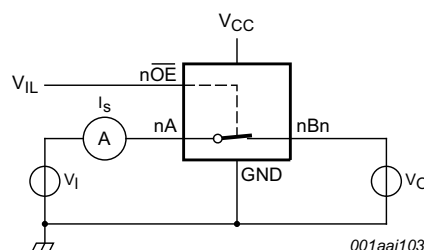

$$V_I = V_{CC} \text{ or GND and } V_O = \text{GND or } V_{CC}.$$

Fig 5. Test circuit for measuring OFF-state leakage current (one switch)



$V_I = V_{CC}$ or GND and $V_O =$ open circuit.

Fig 6. Test circuit for measuring ON-state leakage current (one switch)

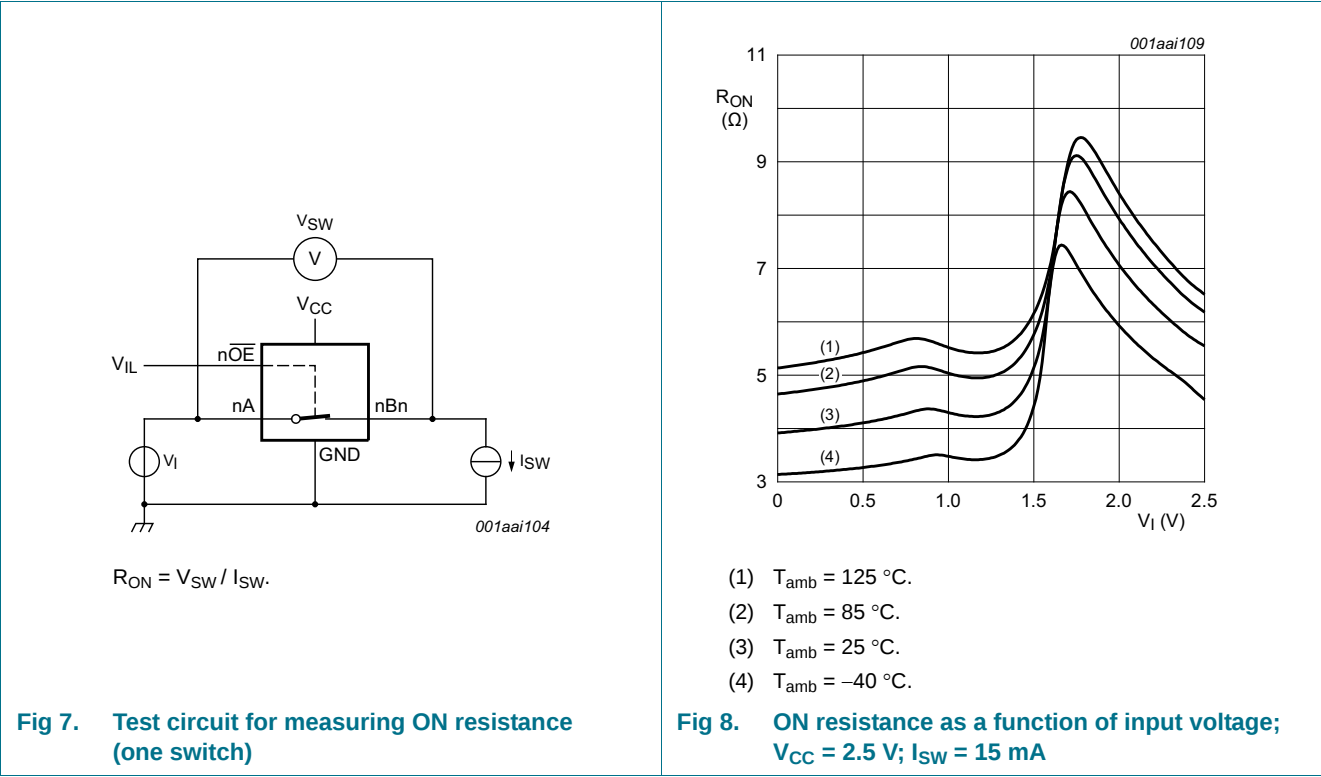
9.2 ON resistance

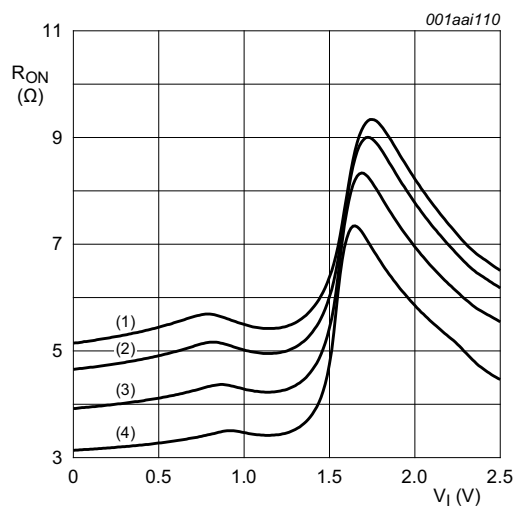
Table 7. Resistance R_{ON}
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$			$T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$		Unit
			Min	Typ ^[1]	Max	Min	Max	
R_{ON}	ON resistance	$V_{CC} = 2.3\text{ V to }2.7\text{ V};$ see Figure 8 to Figure 10 ^[2]						
		$I_{SW} = 64\text{ mA}; V_I = 0\text{ V}$	-	4.2	8.0	-	15.0	Ω
		$I_{SW} = 24\text{ mA}; V_I = 0\text{ V}$	-	4.2	8.0	-	15.0	Ω
		$I_{SW} = 15\text{ mA}; V_I = 1.7\text{ V}$	-	8.4	40.0	-	60.0	Ω
		$V_{CC} = 3.0\text{ V to }3.6\text{ V};$ see Figure 11 to Figure 13						
		$I_{SW} = 64\text{ mA}; V_I = 0\text{ V}$	-	4.0	7.0	-	11.0	Ω
		$I_{SW} = 24\text{ mA}; V_I = 0\text{ V}$	-	4.0	7.0	-	11.0	Ω
		$I_{SW} = 15\text{ mA}; V_I = 2.4\text{ V}$	-	6.2	15.0	-	25.5	Ω

- [1] Typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$ and nominal V_{CC} .
- [2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

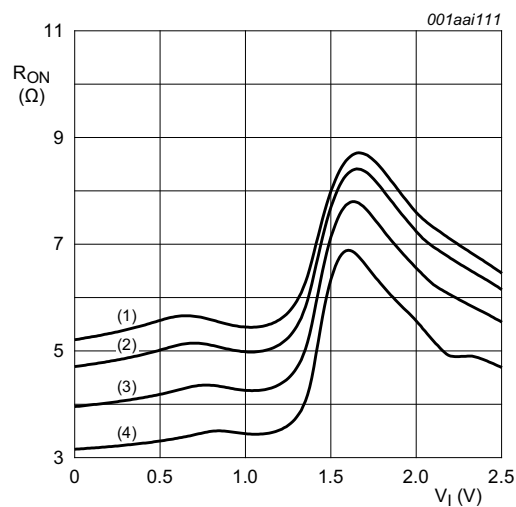
9.3 ON resistance test circuit and graphs





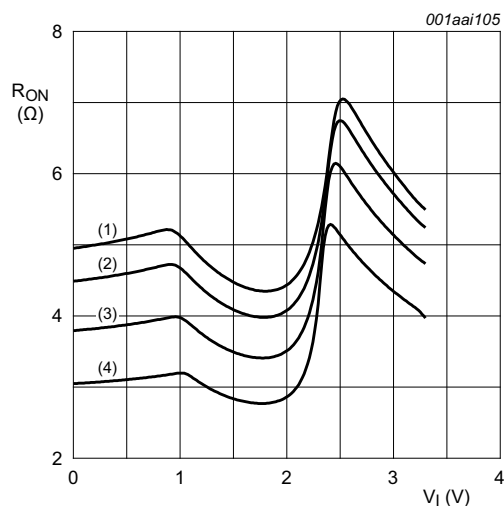
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 9. ON resistance as a function of input voltage;
 $V_{CC} = 2.5\text{ V}; I_{SW} = 24\text{ mA}$



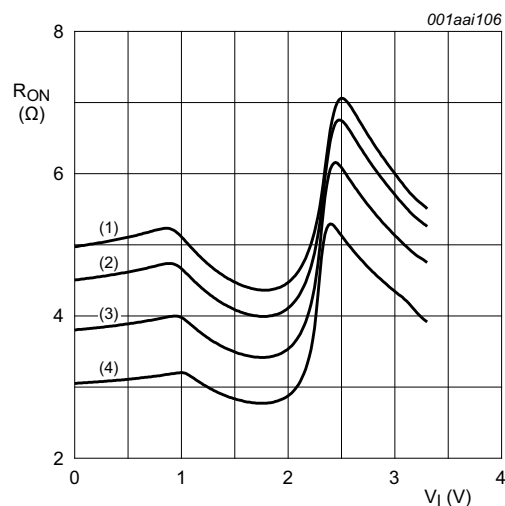
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 10. ON resistance as a function of input voltage;
 $V_{CC} = 2.5\text{ V}; I_{SW} = 64\text{ mA}$



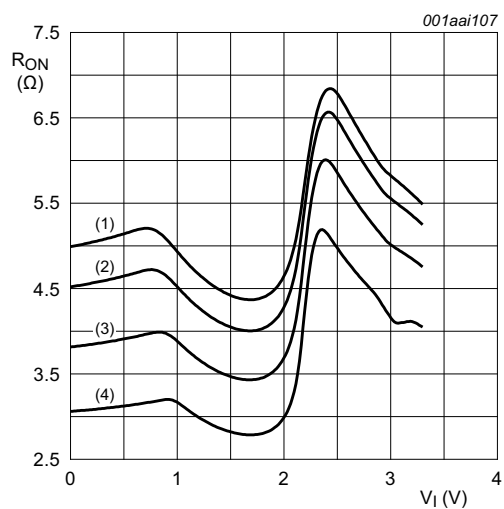
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 11. ON resistance as a function of input voltage;
 $V_{CC} = 3.3\text{ V}; I_{SW} = 15\text{ mA}$



- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 12. ON resistance as a function of input voltage;
 $V_{CC} = 3.3\text{ V}; I_{SW} = 24\text{ mA}$



- (1) $T_{amb} = 125^\circ\text{C}$.
- (2) $T_{amb} = 85^\circ\text{C}$.
- (3) $T_{amb} = 25^\circ\text{C}$.
- (4) $T_{amb} = -40^\circ\text{C}$.

Fig 13. ON resistance as a function of input voltage; $V_{CC} = 3.3\text{ V}$; $I_{SW} = 64\text{ mA}$

10. Dynamic characteristics

Table 8. Dynamic characteristics

$GND = 0\text{ V}$; for test circuit see [Figure 16](#)

Symbol	Parameter	Conditions	$T_{\text{amb}} = -40\text{ °C to }+85\text{ °C}$			$T_{\text{amb}} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nBn or nBn to nA; see Figure 14 ^{[2][3]}						
		$V_{\text{CC}} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.15	-	0.25	ns
		$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	-	-	0.15	-	0.25	ns
		S to nA; see Figure 14 ^[3]						
		$V_{\text{CC}} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.8	6.1	1.0	6.7	ns
		$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.2	5.3	1.0	5.8	ns
t_{en}	enable time	$\overline{\text{OE}}$ to nA or nBn; see Figure 15 ^[4]						
		$V_{\text{CC}} = 2.3\text{ V to }2.7\text{ V}$	1.0	2.2	5.6	1.0	6.2	ns
		$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	1.0	2.0	5.0	1.0	5.5	ns
		S to nBn; see Figure 15						
		$V_{\text{CC}} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.5	6.1	1.0	6.7	ns
		$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.0	5.3	1.0	5.8	ns
t_{dis}	disable time	$\overline{\text{OE}}$ to nA or nBn; see Figure 15 ^[5]						
		$V_{\text{CC}} = 2.3\text{ V to }2.7\text{ V}$	1.0	2.6	5.5	1.0	6.1	ns
		$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.1	5.5	1.0	6.1	ns
		S to nBn; see Figure 15						
		$V_{\text{CC}} = 2.3\text{ V to }2.7\text{ V}$	1.0	2.6	4.8	1.0	5.3	ns
		$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.2	4.5	1.0	5.0	ns

[1] All typical values are measured at $T_{\text{amb}} = 25\text{ °C}$ and at nominal V_{CC} .

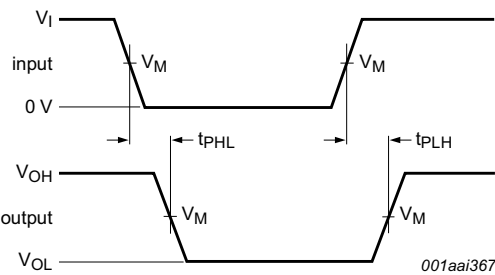
[2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).

[3] t_{pd} is the same as t_{PLH} and t_{PHL} .

[4] t_{en} is the same as t_{PZH} and t_{PZL} .

[5] t_{dis} is the same as t_{PHZ} and t_{PLZ} .

11. Waveforms

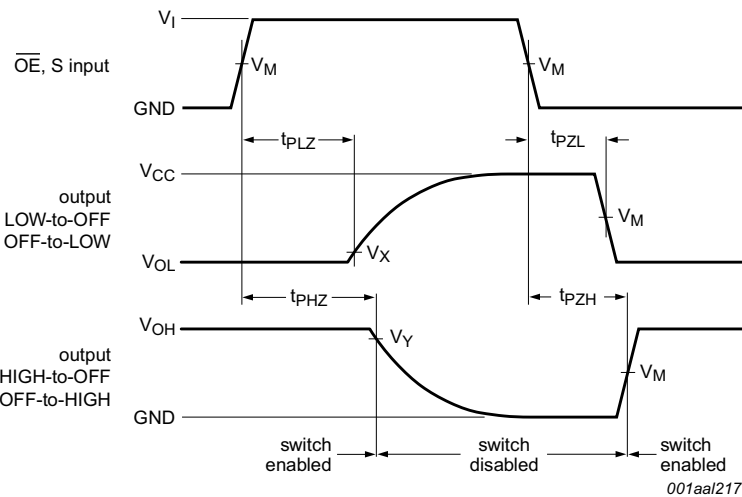


Measurement points are given in [Table 9](#).
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 14. The data input (nA or nBn) to output (nBn or nA) propagation delays

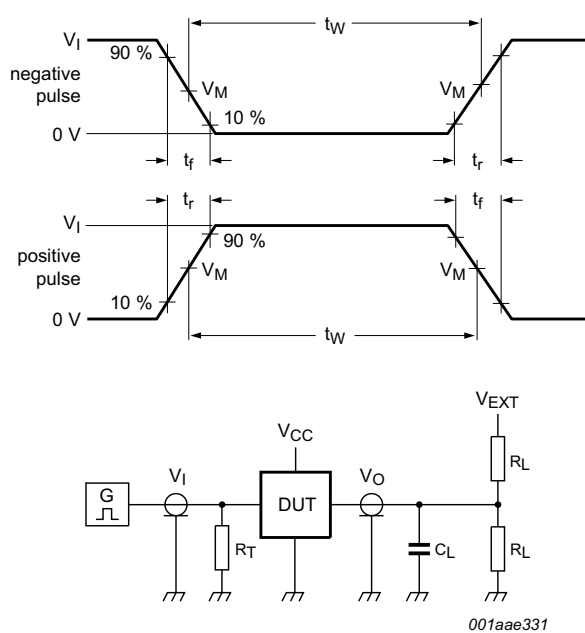
Table 9. Measurement points

Supply voltage	Input			Output		
V_{CC}	V_M	V_I	$t_r = t_f$	V_M	V_X	V_Y
2.3 V to 2.7 V	$0.5V_{CC}$	V_{CC}	≤ 2.0 ns	$0.5V_{CC}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
3.0 V to 3.6 V	$0.5V_{CC}$	V_{CC}	≤ 2.0 ns	$0.5V_{CC}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V



Measurement points are given in [Table 9](#).
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 15. Enable and disable times



Test data is given in [Table 10](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 16. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.3 V to 2.7 V	30 pF	500 Ω	open	GND	$2V_{CC}$
3.0 V to 3.6 V	50 pF	500 Ω	open	GND	$2V_{CC}$

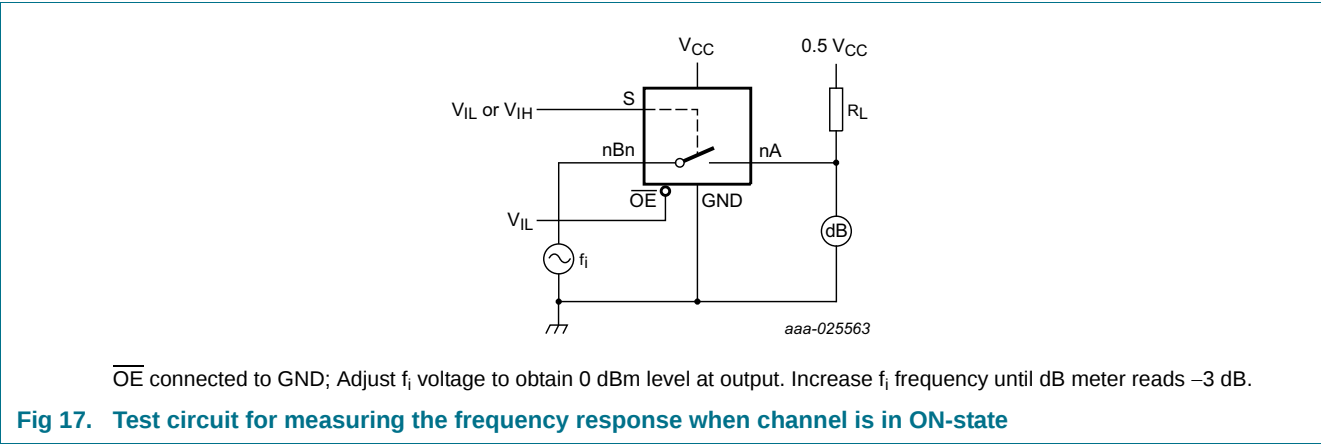
11.1 Additional dynamic characteristics

Table 11. Additional dynamic characteristics
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = \text{GND or } V_{CC}$ (unless otherwise specified); $t_r = t_f \leq 2.5 \text{ ns}$.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			Unit
			Min	Typ	Max	
f _(-3dB)	−3 dB frequency response	V _{CC} = 3.3 V; R _L = 50 Ω; see Figure 17 [1]	-	398	-	MHz

[1] f_i is biased at 0.5V_{CC}.

11.2 Test circuits



12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1

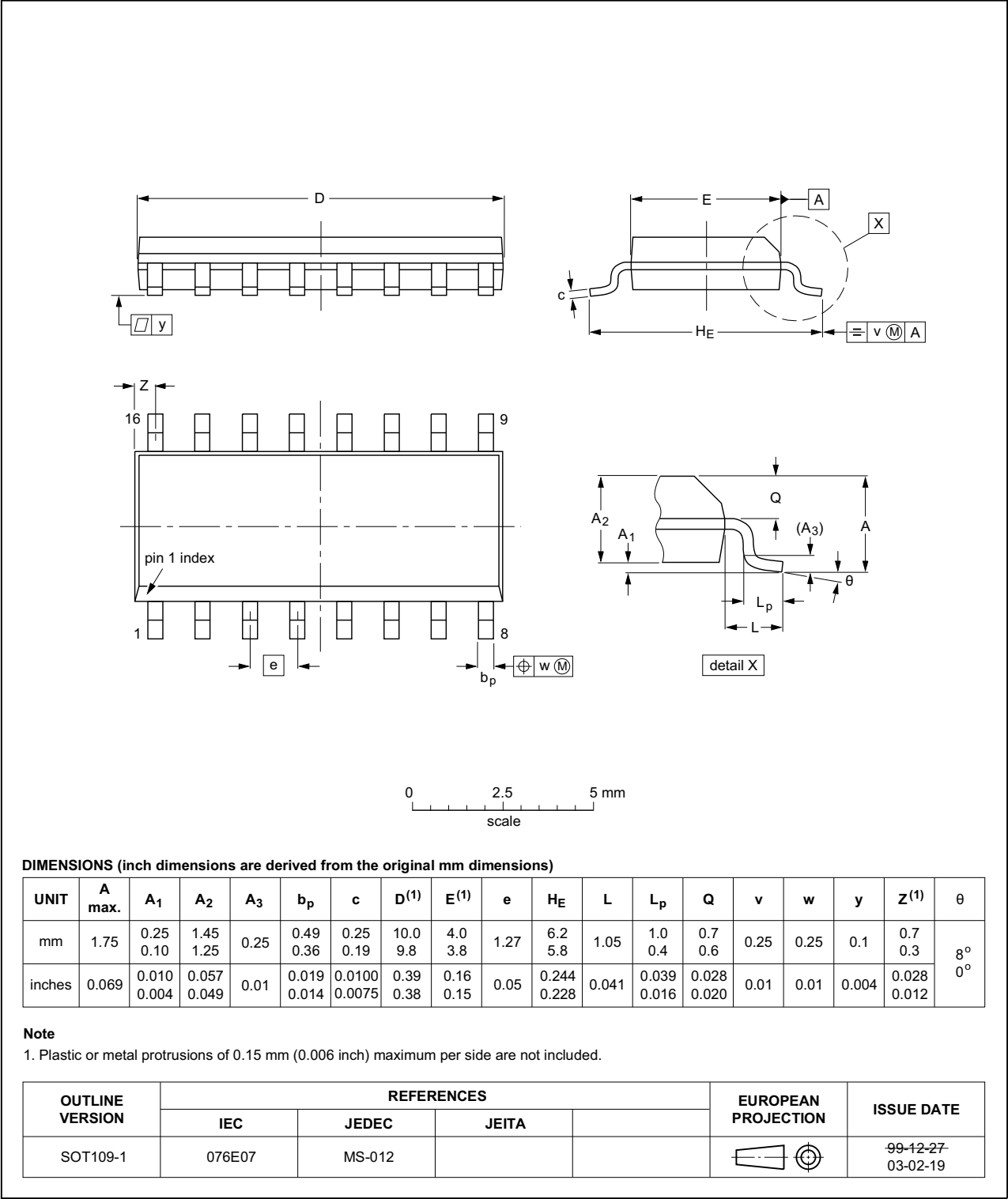


Fig 18. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1

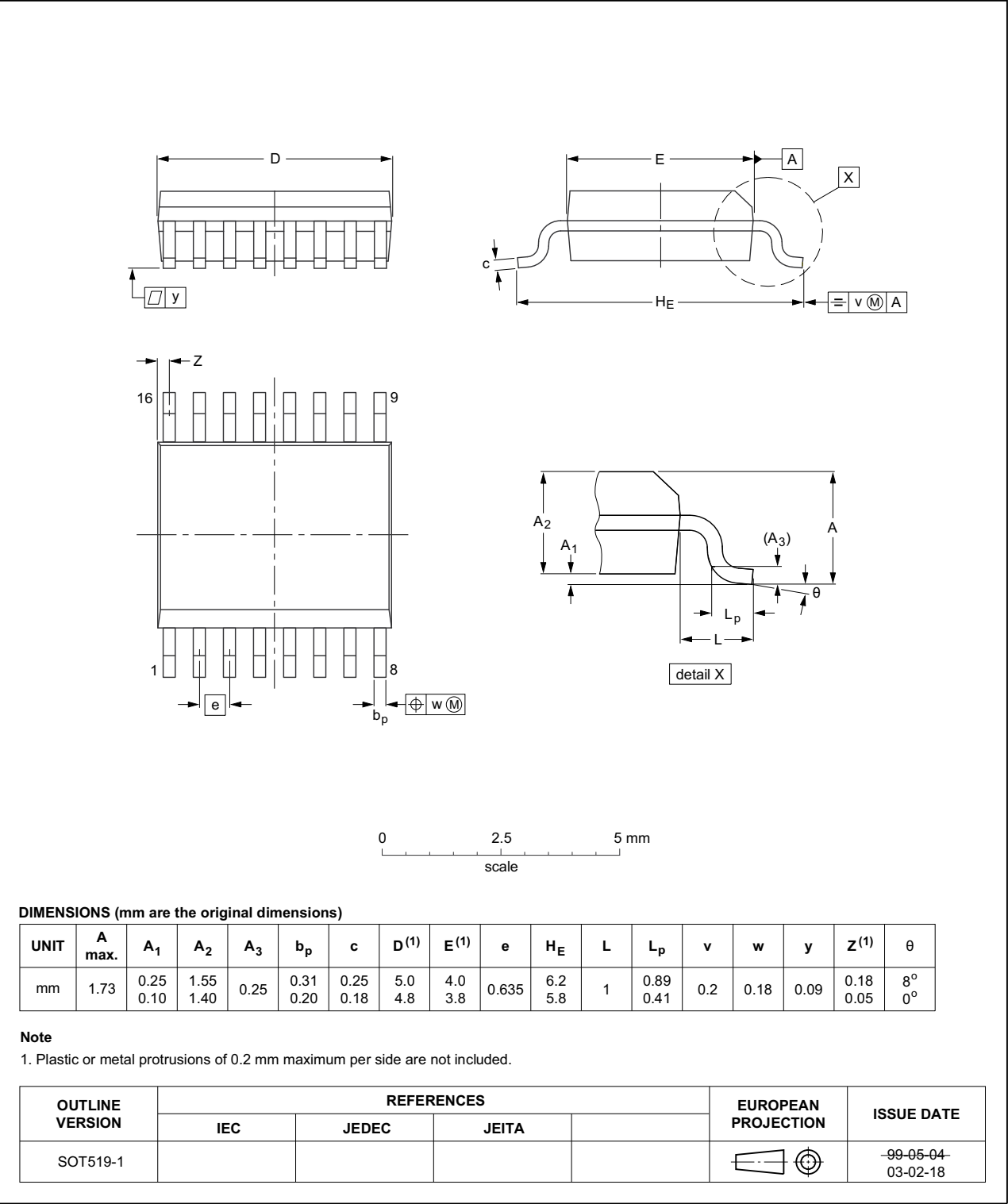
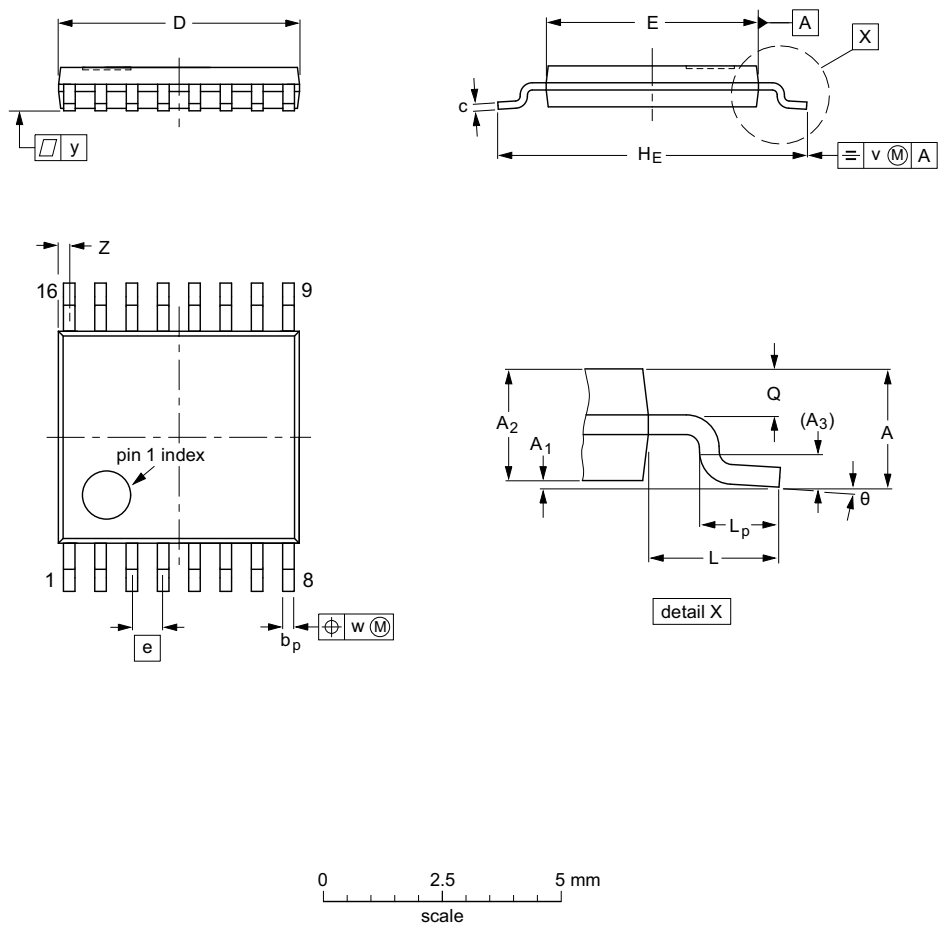


Fig 19. Package outline SOT519-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

- Notes
- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 - 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				-99-12-27 03-02-18

Fig 20. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

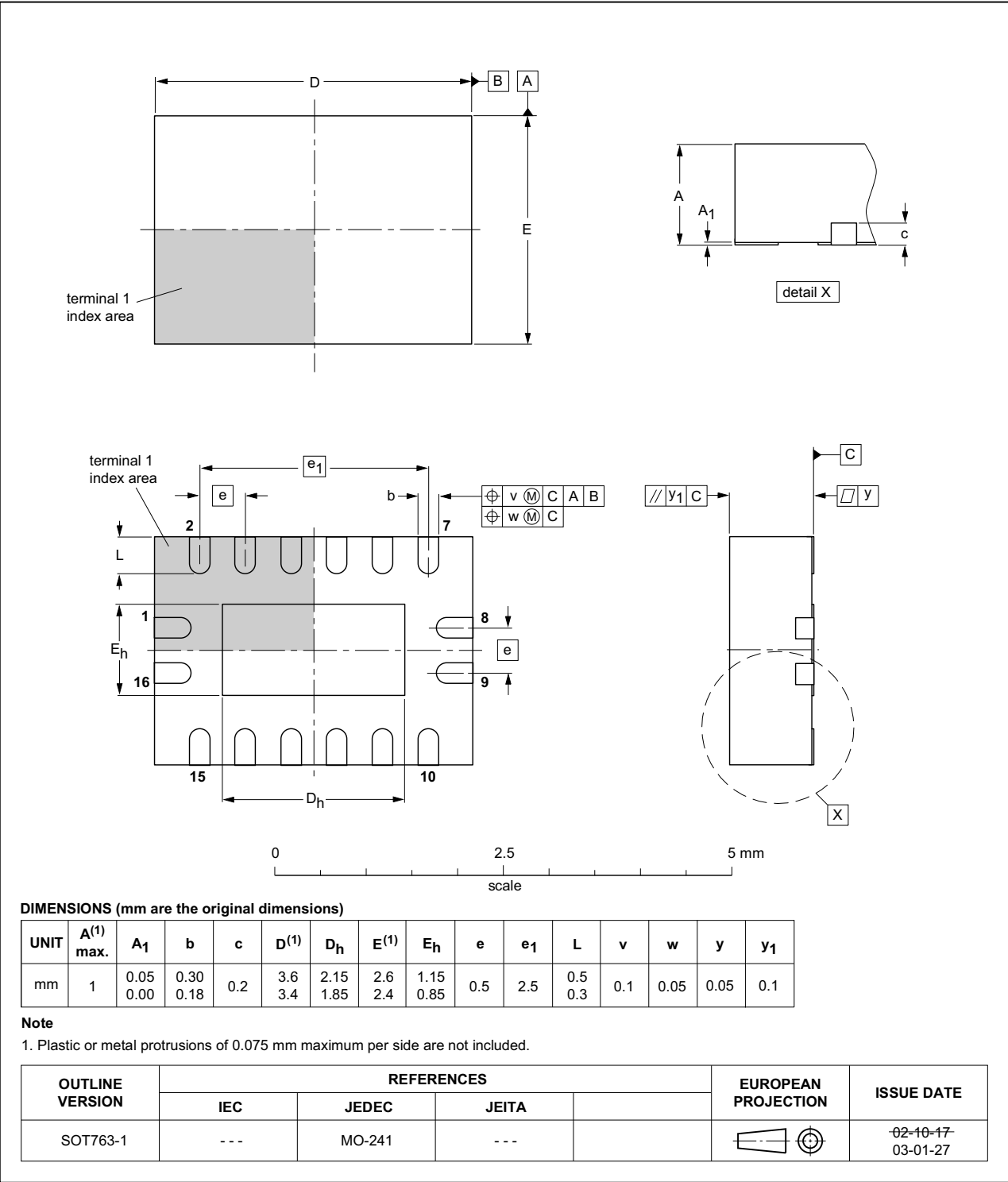


Fig 21. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLV3257 v.5	20161111	Product data sheet	-	74CBTLV3257 v.4
Modifications:	• Section 11.1 and Section 11.2 added.			
74CBTLV3257 v.4	20111216	Product data sheet	-	74CBTLV3257 v.3
Modifications:	• Legal pages updated.			
74CBTLV3257 v.3	20110106	Product data sheet	-	74CBTLV3257 v.2
74CBTLV3257 v.2	20101126	Product data sheet	-	74CBTLV3257 v.1
74CBTLV3257 v.1	20100112	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	4
7	Limiting values	4
8	Recommended operating conditions	4
9	Static characteristics	5
9.1	Test circuits	5
9.2	ON resistance	6
9.3	ON resistance test circuit and graphs	6
10	Dynamic characteristics	9
11	Waveforms	10
11.1	Additional dynamic characteristics	12
11.2	Test circuits	12
12	Package outline	13
13	Abbreviations	17
14	Revision history	17
15	Legal information	18
15.1	Data sheet status	18
15.2	Definitions	18
15.3	Disclaimers	18
15.4	Trademarks	19
16	Contact information	19
17	Contents	20

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2016.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 11 November 2016

Document identifier: 74CBTLV3257

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

[74CBTLV3257BQ,115](#) [74CBTLV3257D,118](#) [74CBTLV3257DS,118](#) [74CBTLV3257PW,118](#)