

May 1988 Revised August 1999

74F382

4-Bit Arithmetic Logic Unit

General Description

The 74F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. An Overflow output is provided for convenience in twos complement arithmetic. A Carry output is provided for ripple expansion. For high-speed expansion using a Carry Lookahead Generator, refer to the 74F381 data sheet.

Features

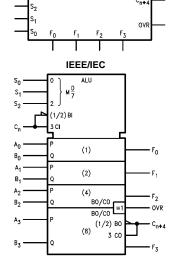
- Performs six arithmetic and logic functions
- Selectable LOW (clear) and HIGH (preset) functions
- LOW input loading minimizes drive requirements
- Carry output for ripple expansion
- Overflow output for twos complement arithmetic

Ordering Code:

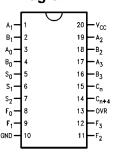
Order Number	Package Number	Package Description
74F382SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F382SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F382PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



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DS009529

Unit Loading/Fan Out

Din Names	Description	U.L.	Input I _{IH} /I _{IL}	
Pin Names	Description	HIGH/LOW	Output I _{OH} /I _{OL}	
A ₀ -A ₃	A Operand Inputs	1.0/4.0	20 μA/–2.4 mA	
B ₀ –B ₃	B Operand Inputs	1.0/4.0	20 μA/–2.4 mA	
S ₀ -S ₂	Function Select Inputs	1.0/1.0	20 μA/-0.6 mA	
C _n	Carry Input	1.0/5.0	20 μA/-3.0 mA	
C _{n + 4}	Carry Output	50/33.3	−1 mA/20 mA	
OVR	Overflow Output	50/33.3	−1 mA/20 mA	
F ₀ -F ₃	Function Outputs	50/33.3	−1 mA/20 mA	

Functional Description

Function Select Table

	Select					
S ₀	S ₁	S ₂	Operation			
L	L	L	Clear			
Н	L	L	B Minus A			
L	Н	L	A Minus B			
Н	Н	L	A Plus B			
L	L	Н	A ⊕ B			
Н	L	Н	A + B			
L	Н	Н	AB			
Н	Н	Н	Preset			

H = HIGH Voltage Level L = LOW Voltage Level

Path Segment	Toward	Output
5. g	F	C _{n+4} , OVR
A_1 or B_1 to C_{n+4}	6.5 ns	6.5 ns
C _n to C _{n+4}	6.3 ns	6.3 ns
C _n to C _{n+4}	6.3 ns	6.3 ns
C _n to F	8.1 ns	_
C_n to C_{n+4} , OVR	_	8.0 ns
Total Delay	27.2 ns	27.1 ns

FIGURE 1. 16-Bit Delay Tabulation

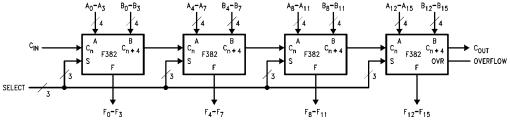


FIGURE 2. 16-Bit Ripply Carry ALU Expansion

Truth Table

				uts			Outputs					
Function	S ₀	S ₁	S ₂	C _n	A _n	B _n	F ₀	F ₁	F ₂	F ₃	OVR	C _{n + 4}
CLEAR	L	L	L	L	Х	Х	L	L	L	L	Н	Н
				Н	X	X	L	L	L	L	Н	Н
B MINUS A	Н	L	L	L	L	L	Н	Н	Н	Н	L	L
				L	L	Н	L	Н	Н	Н	L	Н
				L	Н	L	L	L	L	L	L	L
				L	Н	Н	Н	Н	Н	Н	L	L
				Н	L	L	L	L	L	L	L	Н
				Н	L	Н	Н	Н	Н	Н	L	Н
				Н	Н	L	Н	L	L	L	L	L
				Н	Н	Н	L	L	L	L	L	Н
A MINUS B	L	Н	L	L	L	L	Н	Н	Н	Н	L	L
				L	L	Н	L	L	L	L	L	L
				L	Н	L	L	Н	Н	Н	L	Н
				L	Н	Н	Н	Н	Н	Н	L	L
				Н	L	L	L	L	L	L	L	Н
				Н	L	Н	Н	L	L	L	L	L
				Н	Н	L	Н	Н	Н	Н	L	Н
				Н	Н	Н	L	L	L	L	L	Н
A PLUS B	Н	Н	L	L	L	L	L	L	L	L	L	L
				L	L	Н	Н	Н	Н	Н	L	L
				L	Н	L	Н	Н	Н	Н	L	L
				L	Н	Н	L	Н	Н	Н	L	Н
				Н	L	L	Н	L	L	L	L	L
				Н	L	Н	L	L	L	L	L	Н
				Н	Н	L	L	L	L	L	L	Н
				Н	Н	Н	Н	Н	Н	Н	L	Н
A⊕B	L	L	Н	Х	L	L	L	L	L	L	L	L
				X	L	Н	Н	Н	Н	Н	L	L
				L	Н	L	Н	Н	Н	Н	L	L
				X	Н	Н	L	L	L	L	Н	Н
				Н	Н	L	Н	Н	Н	Н	Н	Н
A + B	Н	L	Н	Х	L	L	L	L	L	L	L	L
				X	L	Н	Н	Н	Н	Н	L	L
				X	Н	L	Н	Н	Н	Н	L	L
				L	Н	Н	Н	Н	Н	Н	L	L
				Н	Н	Н	Н	Н	Н	Н	Н	Н
AB	L	Н	Н	Х	L	L	L	L	L	L	Н	Н
				Χ	L	Н	L	L	L	L	L	L
				Χ	Н	L	L	L	L	L	Н	Н
				L	Н	Н	Н	Н	Н	Н	L	L
				Н	Н	Н	Н	Н	Н	Н	Н	Н
PRESET	Н	Н	Н	Х	L	L	Н	Н	Н	Н	L	L
				Χ	L	Н	Н	Н	Н	Н	L	L
				Χ	Н	L	Н	Н	Н	Н	L	L
				L	Н	Н	Н	Н	Н	Н	L	L
	1			Н	Н	Н	Н	Н	Н	Н	Н	Н

Absolute Maximum Ratings(Note 1)

-65°C to +150°C Storage Temperature Ambient Temperature under Bias -55°C to +125°C

Junction Temperature under Bias -55°C to +150°C V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V

Input Voltage (Note 2) -0.5V to +7.0VInput Current (Note 2) -30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5V to V_{CC}

3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA)

Recommended Operating Conditions

0°C to +70°C Free Air Ambient Temperature Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

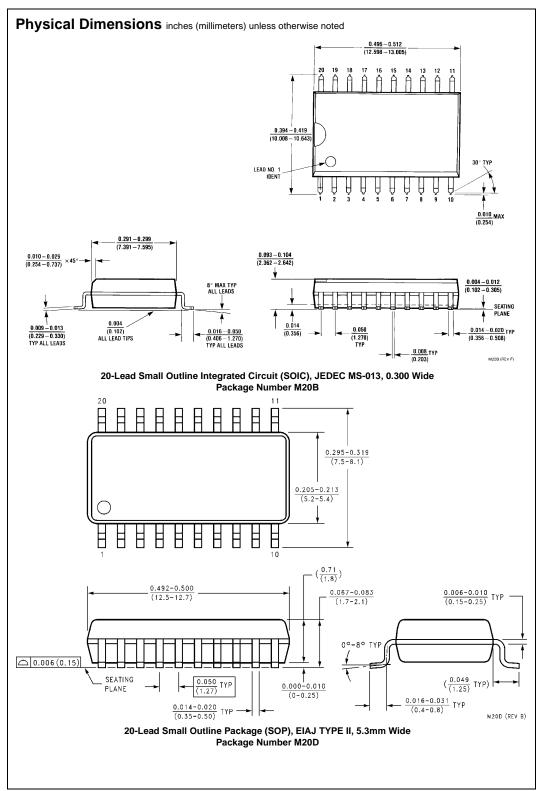
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics over Operating Temperature Range unless otherwise specified

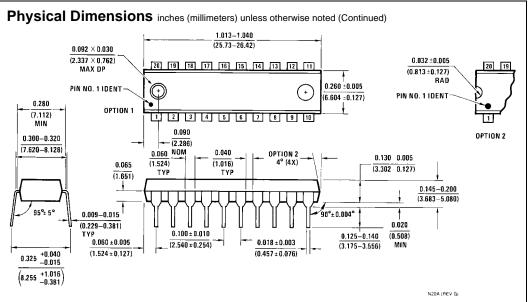
Symbol	Parameter		Min	Тур	Max	Units	v _{cc}	Conditions
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH	10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA
	Voltage	5% V _{CC}	2.7			V	IVIIII	$I_{OH} = -1 \text{ mA}$
V _{OL}	Output LOW	10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA
	Voltage	10% VCC			0.5	V	IVIIII	I _{OL} = 20 IIIA
I _{IH}	Input HIGH				5.0	μА	Max	V _{IN} = 2.7V
	Current				3.0	μΛ	IVIAX	V N - 2.1 V
I _{BVI}	Input HIGH Current				7.0	μА	Max	V _{IN} = 7.0V
	Breakdown Test				7.0	μΛ	IVIAX	V _{IN} = 1.0V
I _{CEX}	Output HIGH				50	μА	Max	V _{OUT} = V _{CC}
	Leakage Current				50	μΑ	IVIAX	VOUT = VCC
V _{ID}	Input Leakage		4.75			V	0.0	$I_{ID} = 1.9 \mu A$
	Test		4.73			V	0.0	All Other Pins Grounded
I _{OD}	Output Leakage				3.75	μА	0.0	V _{IOD} = 150 mV
	Circuit Current				3.73	μΛ	0.0	All Other Pins Grounded
I _{IL}	Input LOW Current				-0.6			$V_{IN} = 0.5V (S_0 - S_2)$
					-2.4	mA	Max	$V_{IN} = 0.5V (A_0 - A_3, B_0 - B_3)$
					-3.0			$V_{IN} = 0.5V (C_n)$
los	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V
Icc	Power Supply Current			54	81	mA	Max	

AC Electrical Characteristics

Symbol	Parameter		$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$	'	$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50$ pF		Units	
		Min	Тур	Max	Min	Max		
t _{PLH}	Propagation Delay	3.0	8.1	12.0	3.0	13.0	ns	
t _{PHL}	C _n to F _i	2.5	5.7	8.0	2.5	9.0	115	
t _{PLH}	Propagation Delay	4.0	10.4	15.0	3.5	17.0	ns	
t _{PHL}	Any A or B to Any F	3.0	8.2	11.0	2.5	12.0	ns	
t _{PLH}	Propagation Delay	6.5	11.0	20.5	5.5	21.5		
t _{PHL}	S _i to F _i	4.0	8.2	15.0	4.0	17.5	ns	
t _{PLH}	Propagation Delay	3.5	6.0	8.5	3.5	11.0	20	
t _{PHL}	A _i or B _i to C _n + 4	3.5	6.5	9.0	3.5	10.5	ns	
t _{PLH}	Propagation Delay	7.0	12.5	16.5	7.0	17.5	ns	
t _{PHL}	S _i to OVR or C _{n+4}	5.0	9.0	12.0	5.0	14.5	115	
t _{PLH}	Propagation Delay	2.5	5.6	8.0	2.0	9.0		
t _{PHL}	C_n to C_{n+4}	3.5	6.3	9.0	2.0	10.0	ns	
t _{PLH}	Propagation Delay	3.5	8.0	11.0	3.5	13.0		
t _{PHL}	C _n to OVR	2.5	7.1	10.0	2.5	11.0	ns	
t _{PLH}	Propagation Delay	7.0	11.5	15.5	7.0	16.5	ns	
t _{PHL}	A _i or B _i to OVR	3.0	8.0	10.5	3.0	11.5	115	







20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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