

Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use **<http://www.nexperia.com>**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

74HC112; 74HCT112

Dual JK flip-flop with set and reset; negative-edge trigger

Rev. 3 — 9 August 2016

Product data sheet

1. General description

The 74HC112; 74HCT112 is a dual negative-edge triggered JK flip-flop. It features individual J and K inputs, clock ($\overline{nCP}$) set ($\overline{nSD}$) and reset ($\overline{nRD}$) inputs. It also has complementary $\overline{nQ}$ and $\overline{n\overline{Q}}$ outputs. The set and reset are asynchronous active LOW inputs and operate independently of the clock input. The J and K inputs control the state changes of the flip-flops as described in the mode select function table. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

2. Features and benefits

- Input levels:
 - ◆ For 74HC112: CMOS level
 - ◆ For 74HCT112: TTL level
- Asynchronous set and reset
- Specified in compliance with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

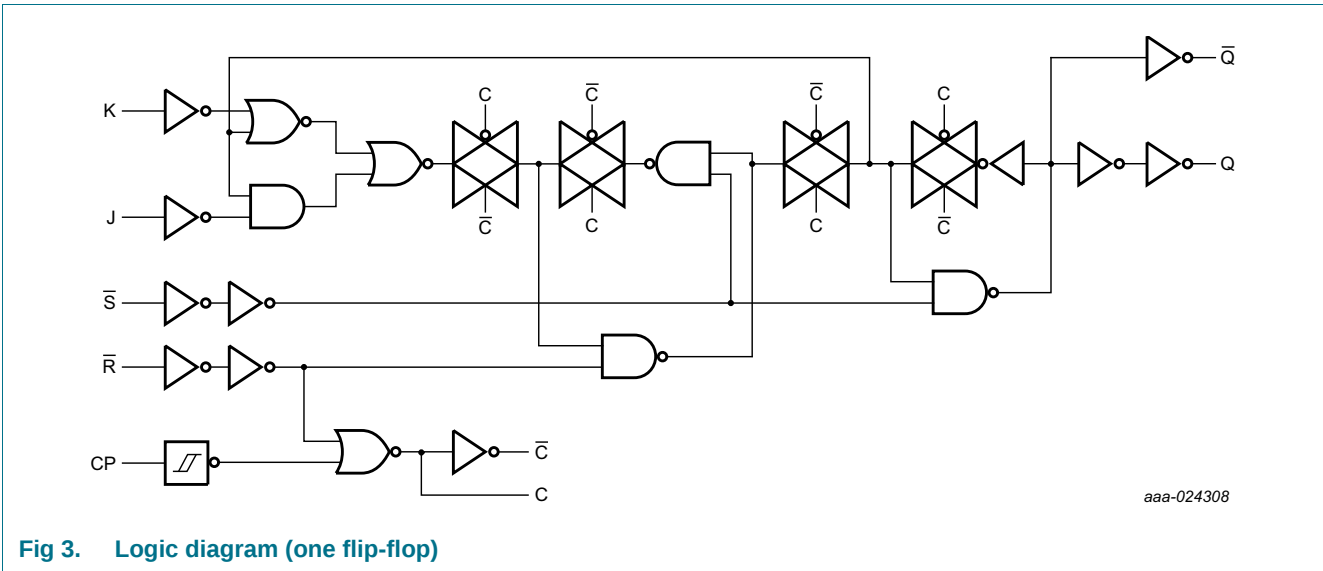
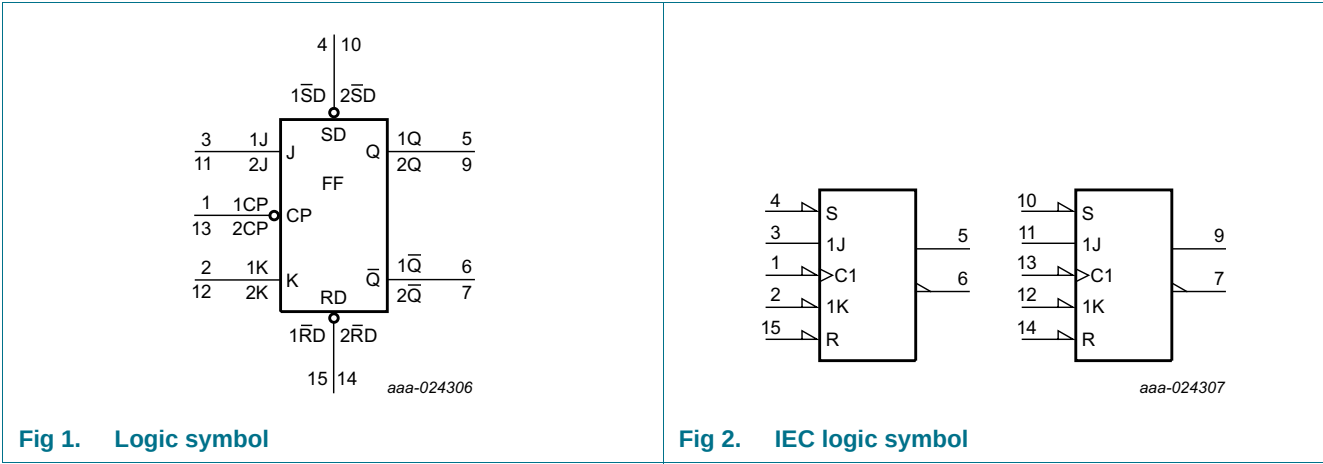
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC112D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT112D				
74HC112DB	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT112DB				
74HC112PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT112PW				



4. Functional diagram



5. Pinning information

5.1 Pinning

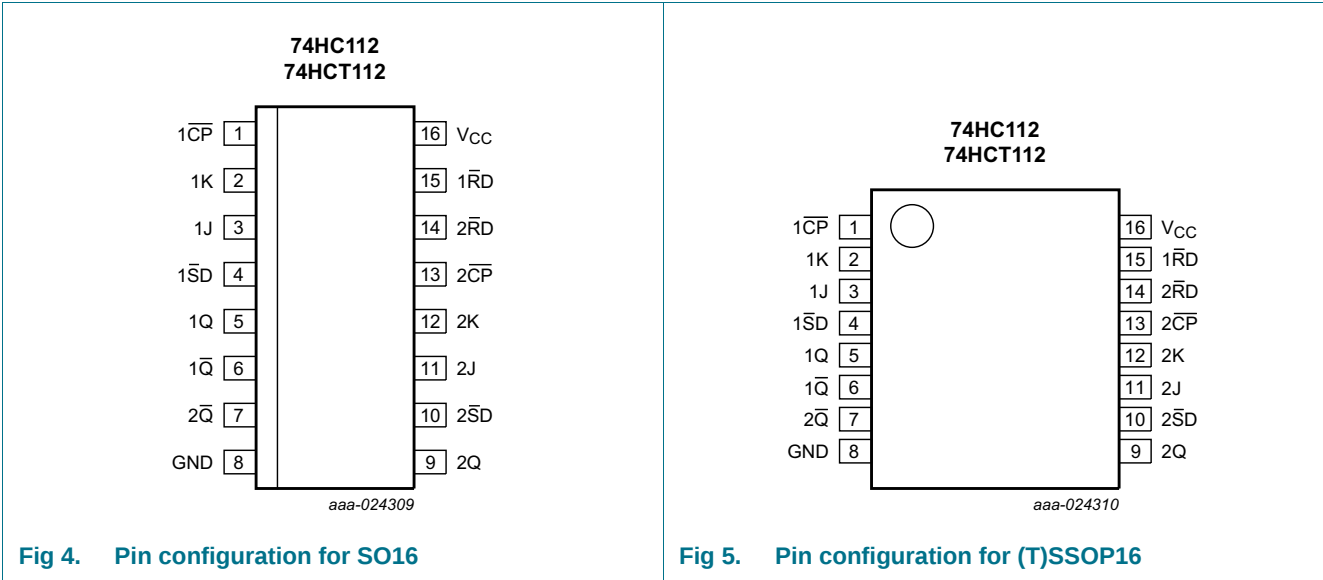


Fig 4. Pin configuration for SO16

Fig 5. Pin configuration for (T)SSOP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{1CP}, \overline{2CP}$	1, 13	clock input (HIGH-to-LOW; edge-triggered)
1K, 2K	2, 12	data input
1J, 2J	3, 11	data input
$\overline{1SD}, \overline{2SD}$	4, 10	set input (active LOW)
1Q, 2Q	5, 9	true flip-flop output
$\overline{1Q}, \overline{2Q}$	6, 7	complement flip-flop output
GND	8	ground (0 V)
$\overline{1RD}, \overline{2RD}$	15, 14	reset input (active LOW)
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function selection^[1]

Operating modes	Input					Output	
	nSD	nRD	nCP	nJ	nK	nQ	nQ
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	L
Toggle	H	H	↓	h	h	$\bar{q}$	q
Load 0 (reset)	H	H	↓	l	h	L	H
Load 1 (set)	H	H	↓	h	l	H	L
Hold no change	H	H	↓	l	l	q	$\bar{q}$

[1] If nSD and nRD simultaneously go from LOW-to-HIGH, the output states are unpredictable.

H = HIGH voltage level

h = HIGH voltage level one set-up time before the HIGH-to-LOW clock transition

L = LOW voltage level

l = LOW voltage level one set-up time before the HIGH-to-LOW clock transition

q = lowercase letters indicate the state of the referenced output one set-up time before the HIGH-to-LOW clock transition

X = don't care

↓ = HIGH-to-LOW clock transition

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	SO16 and (T)SSOP16 packages ^[1]	-	500	mW

[1] For SO16 packages: above 70 °C, the value of P_{tot} derates linearly with 8 mW/K.

For (T)SSOP16 packages: above 60 °C, the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC112			74HCT112			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC112										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = −20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = −4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = −5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	4.0	-	40	-	80	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT112										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = –20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} – 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		nSD inputs	-	50	180	-	225	-	245	µA
		nK inputs	-	60	216	-	270	-	294	µA
		nRD inputs	-	65	236	-	293	-	319	µA
		nJ, and nCP inputs	-	100	360	-	450	-	490	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
74HC112										
t _{pd}	propagation delay	nCP to nQ; see Figure 6 ^[2]								
		V _{CC} = 2.0 V	-	55	175	-	220	-	265	ns
		V _{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	16	30	-	37	-	45	ns
		nCP to nQ; see Figure 6								
		V _{CC} = 2.0 V	-	55	175	-	220	-	265	ns
		V _{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	16	30	-	37	-	45	ns
		nRD to nQ, nQ; see Figure 7								
		V _{CC} = 2.0 V	-	58	180	-	225	-	270	ns
		V _{CC} = 4.5 V	-	21	36	-	45	-	54	ns
		V _{CC} = 5 V; C _L = 15 pF	-	18	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	17	31	-	38	-	46	ns
		nSD to nQ, nQ; see Figure 7								
		V _{CC} = 2.0 V	-	50	155	-	295	-	235	ns
		V _{CC} = 4.5 V	-	18	31	-	39	-	47	ns
		V _{CC} = 5 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	14	26	-	33	-	40	ns
t _t	transition time	nQ, nQ; see Figure 6 ^[3]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _w	pulse width	nCP HIGH or LOW; see Figure 6								
		V _{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		nSD, nRD LOW; see Figure 7								
		V _{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	8	-	20	-	24	-	ns
V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns		

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
t_{rec}	recovery time	$\overline{\text{nRD}}$ to $\overline{\text{nCP}}$; see Figure 7								
		$V_{\text{CC}} = 2.0$ V	80	22	-	125	-	150	-	ns
		$V_{\text{CC}} = 4.5$ V	16	8	-	25	-	30	-	ns
		$V_{\text{CC}} = 6.0$ V	14	6	-	21	-	26	-	ns
		$\overline{\text{nSD}}$ to $\overline{\text{nCP}}$; see Figure 7								
		$V_{\text{CC}} = 2.0$ V	80	–19	-	100	-	120	-	ns
		$V_{\text{CC}} = 4.5$ V	16	–7	-	20	-	24	-	ns
		$V_{\text{CC}} = 6.0$ V	14	–6	-	17	-	20	-	ns
t_{su}	set-up time	nJ and nK to $\overline{\text{nCP}}$; see Figure 6								
		$V_{\text{CC}} = 2.0$ V	80	19	-	100	-	120	-	ns
		$V_{\text{CC}} = 4.5$ V	16	7	-	20	-	24	-	ns
		$V_{\text{CC}} = 6.0$ V	14	6	-	17	-	20	-	ns
t_{h}	hold time	nJ and nK to $\overline{\text{nCP}}$; see Figure 6								
		$V_{\text{CC}} = 2.0$ V	0	–11	-	0	-	0	-	ns
		$V_{\text{CC}} = 4.5$ V	0	–4	-	0	-	0	-	ns
		$V_{\text{CC}} = 6.0$ V	0	–3	-	0	-	0	-	ns
f_{max}	maximum frequency	$\overline{\text{nCP}}$; see Figure 6								
		$V_{\text{CC}} = 2.0$ V	6	20	-	4.8	-	4.0	-	MHz
		$V_{\text{CC}} = 4.5$ V	30	60	-	24	-	20	-	MHz
		$V_{\text{CC}} = 5$ V; $C_L = 15$ pF	-	66	-	-	-	-	-	MHz
		$V_{\text{CC}} = 6.0$ V	35	71	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{\text{CC}}$ ^[4]	-	27	-			-	-	pF

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
74HCT112										
t _{pd}	propagation delay	nCP to nQ; see Figure 6 ^[2]								
		V _{CC} = 4.5 V	-	21	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	19	-	-	-	-	-	ns
		nCP to nQ; see Figure 6 ^[2]								
		V _{CC} = 4.5 V	-	23	40	-	50	-	60	ns
		V _{CC} = 5 V; C _L = 15 pF	-	19	-	-	-	-	-	ns
		nRD to nQ, nQ; see Figure 7								
		V _{CC} = 4.5 V	-	22	37	-	46	-	56	ns
		V _{CC} = 5 V; C _L = 15 pF	-	19	-	-	-	-	-	ns
		nSD to nQ, nQ; see Figure 7								
		V _{CC} = 4.5 V	-	18	32	-	40	-	48	ns
		V _{CC} = 5 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
t _t	transition time	nQ, nQ; see Figure 6 ^[3]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t _w	pulse width	nCP HIGH or LOW; see Figure 6								
		V _{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		nSD, nRD LOW; see Figure 7								
		V _{CC} = 4.5 V	18	10	-	23	-	27	-	ns
t _{rec}	recovery time	nRD to nCP; see Figure 7								
		V _{CC} = 4.5 V	20	11	-	25	-	30	-	ns
		nSD to nCP; see Figure 7								
		V _{CC} = 4.5 V	20	–8	-	25	-	30	-	ns
t _{su}	set-up time	nJ and nK to nCP; see Figure 6								
		V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
t _h	hold time	nJ and nK to nCP; see Figure 6								
		V _{CC} = 4.5 V	0	–7	-	0	-	0	-	ns
f _{max}	maximum frequency	nCP; see Figure 6								
		V _{CC} = 4.5 V	30	64	-	24	-	20	-	MHz
		V _{CC} = 5 V; C _L = 15 pF	-	70	-	-	-	-	-	MHz

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC}$ ^[4]	-	30	-	-	-	-	-	pF

[1] All typical values are measured at $T_{amb} = 25$ °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] t_t is the same as t_{THL} and t_{TLH} .

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

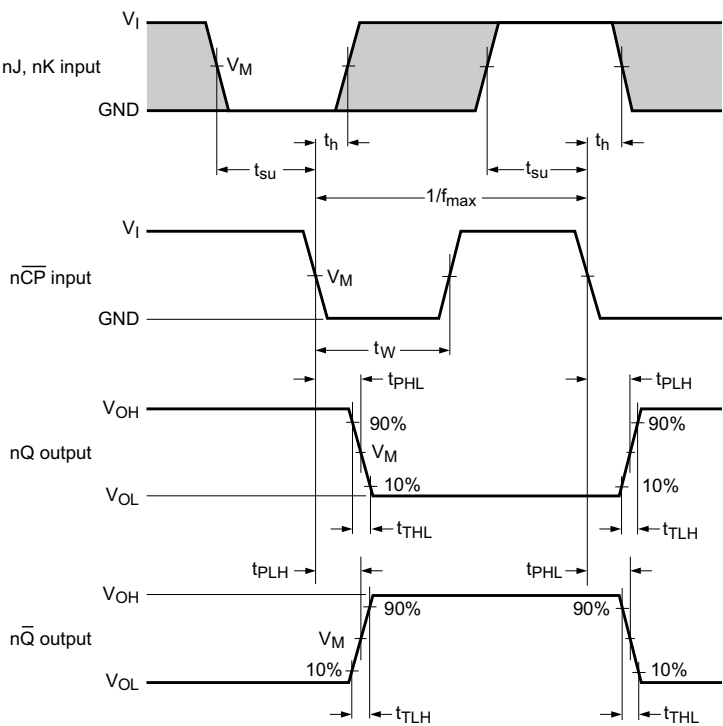
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



aaa-024311

Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Clock propagation delays, output transition time, pulse width, set-up, hold times, and maximum frequency

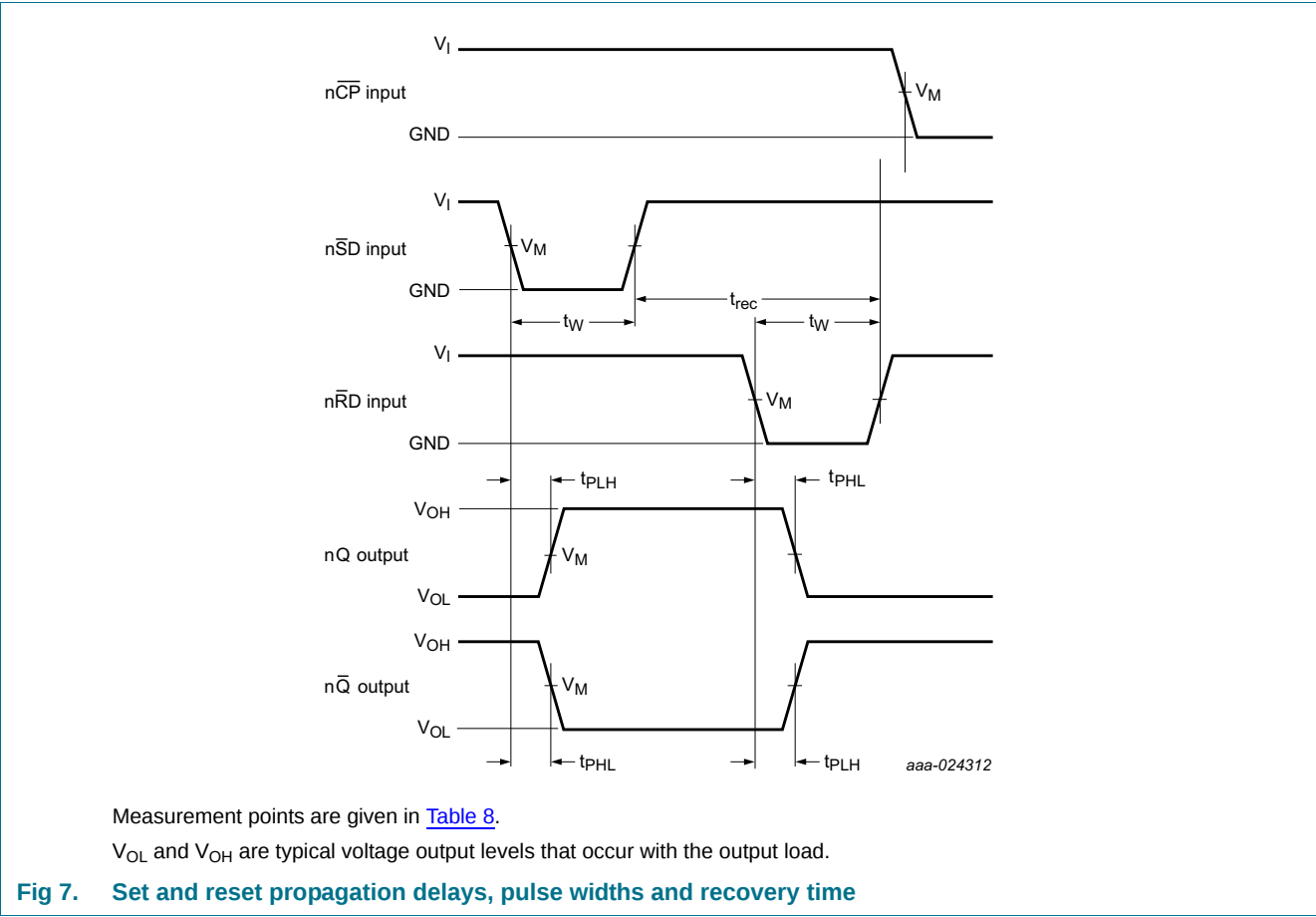
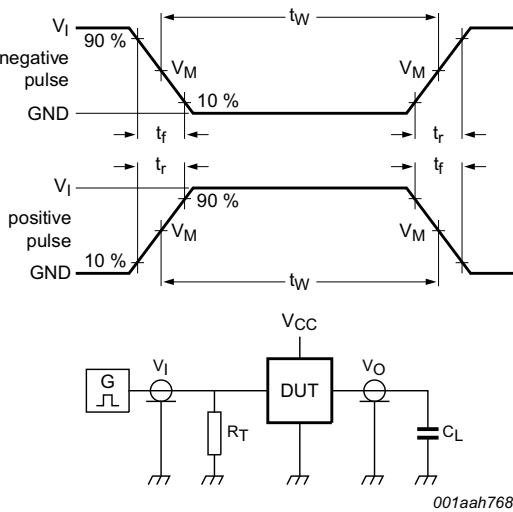


Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC112	$0.5V_{CC}$	$0.5V_{CC}$
74HCT112	1.3 V	1.3 V



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC112	V_{CC}	6 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT112	3 V	6 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

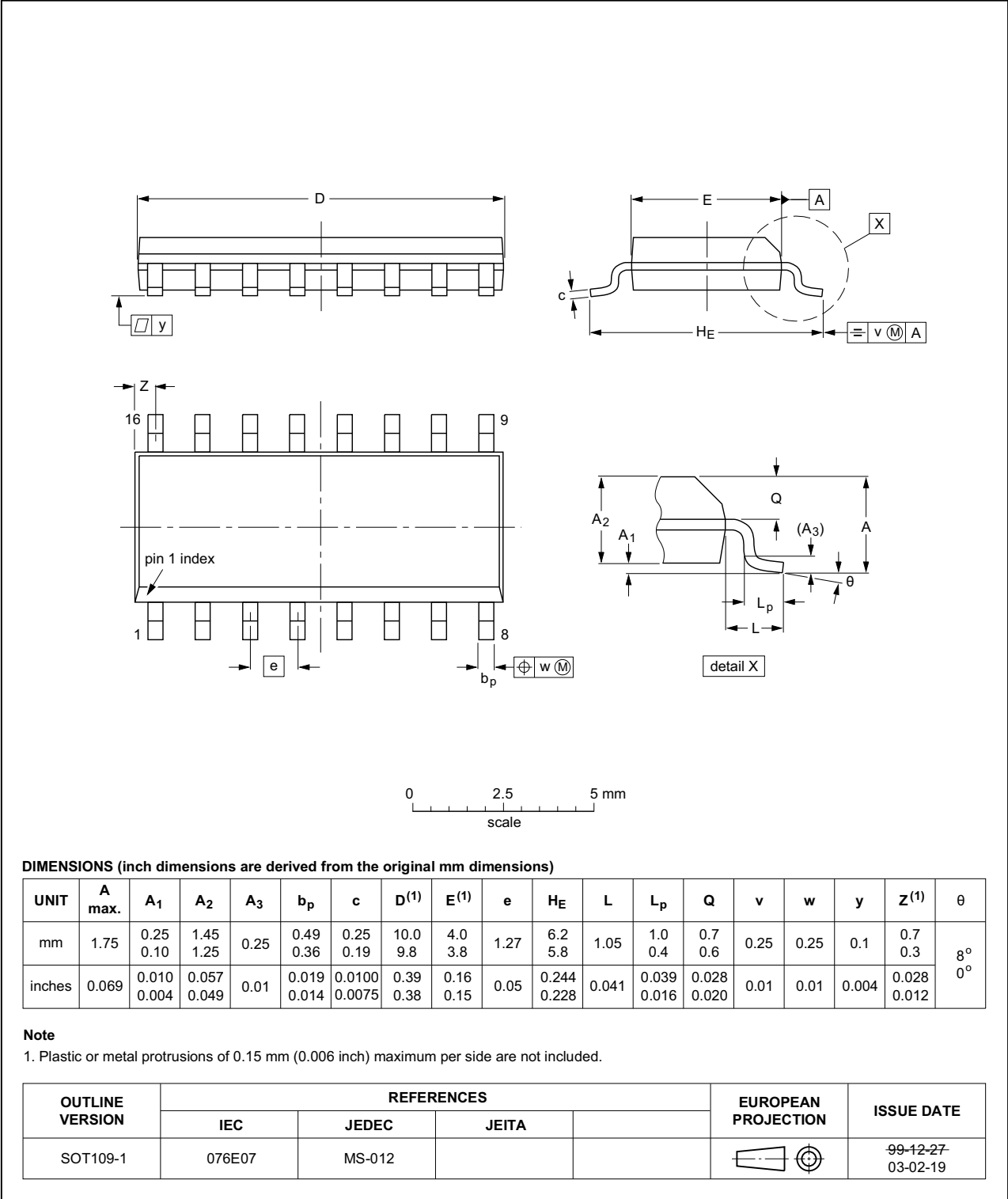


Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

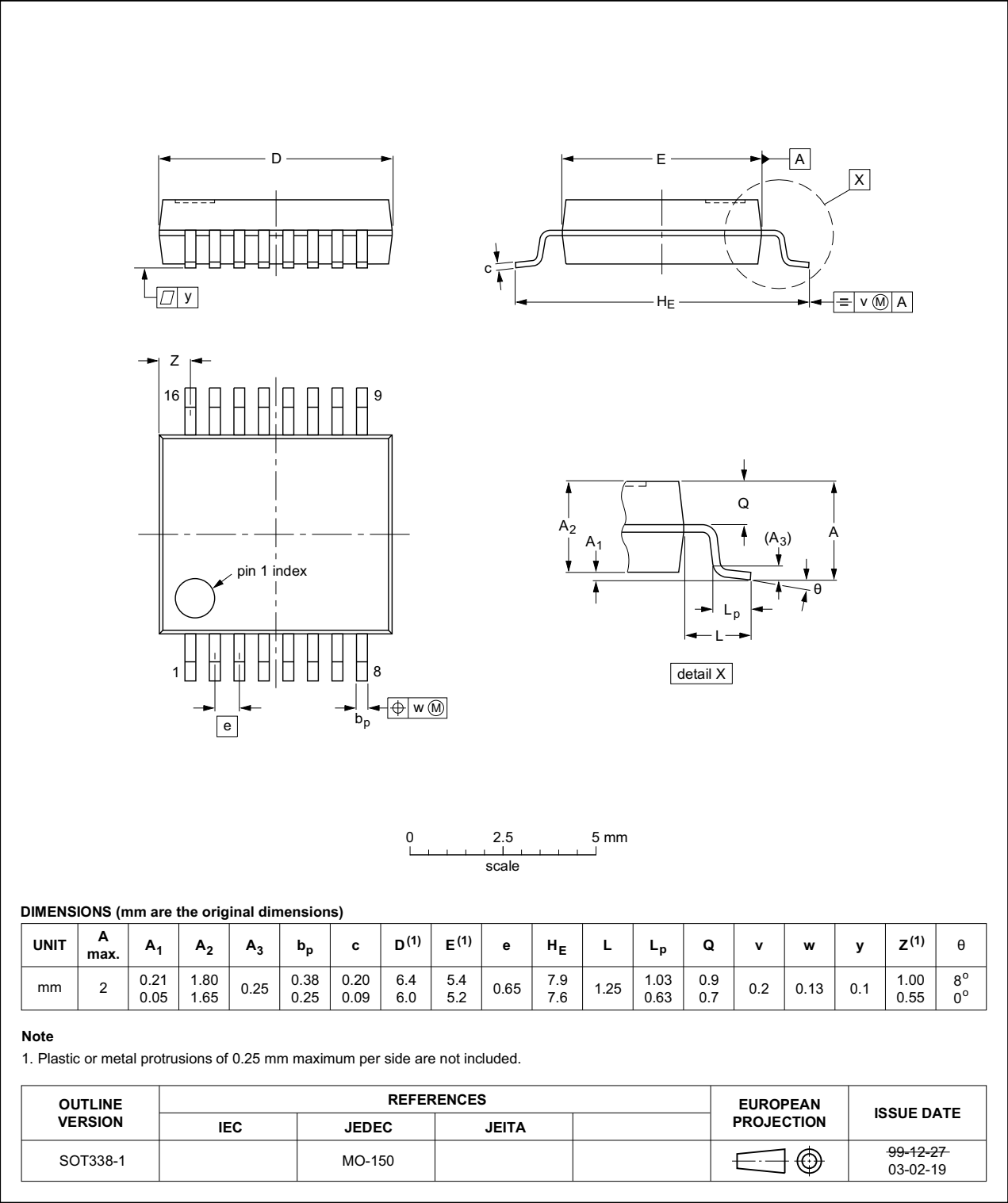


Fig 10. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

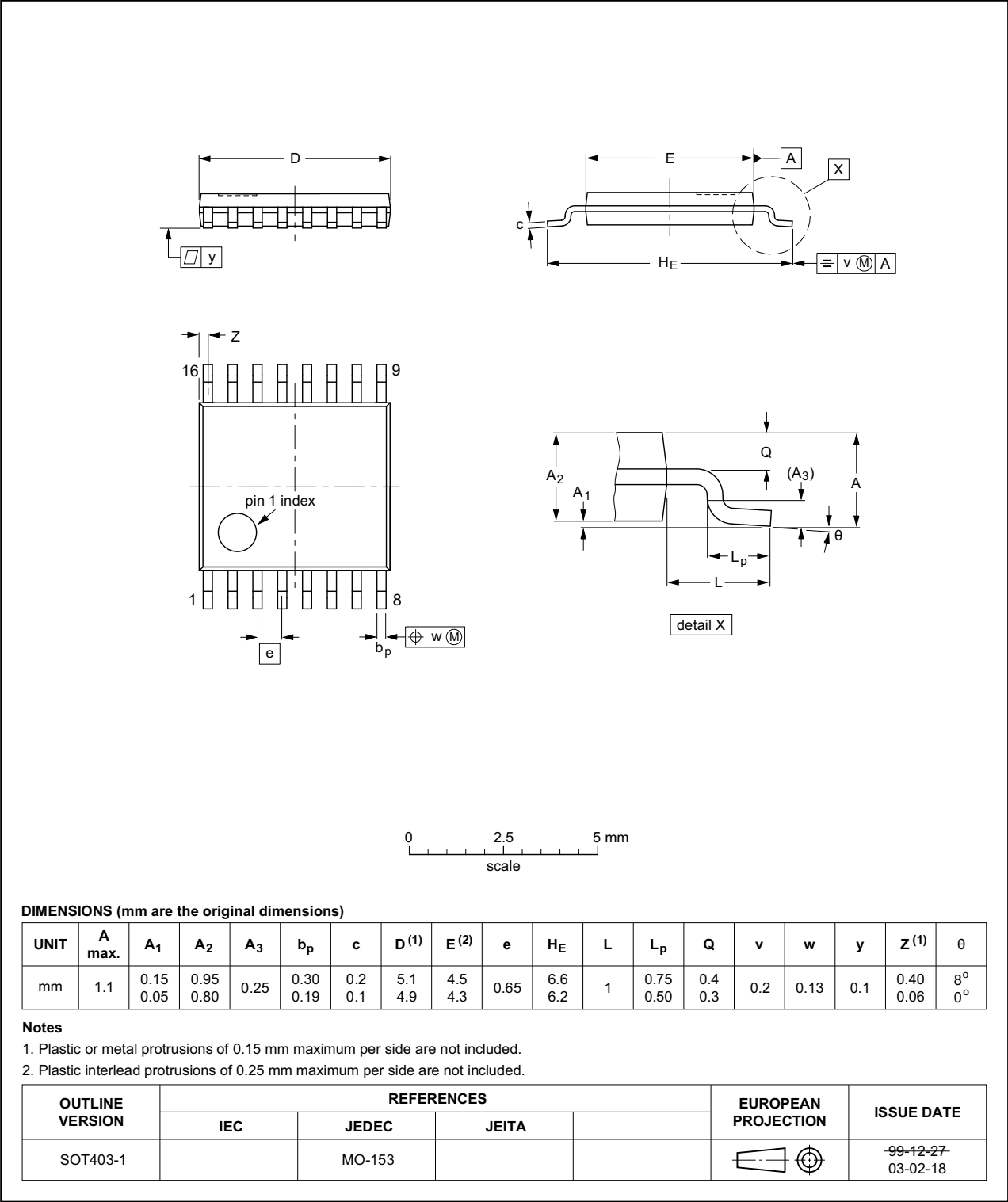


Fig 11. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT112 v.3	20160809	Product data sheet	-	74HC_HCT112_CNV v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Type numbers 74HC112N and 74HCT112N removed.			
74HC_HCT112_CNV v.2	19980610	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	4
7	Limiting values	4
8	Recommended operating conditions	5
9	Static characteristics	5
10	Dynamic characteristics	7
11	Waveforms	11
12	Package outline	14
13	Abbreviations	17
14	Revision history	17
15	Legal information	18
15.1	Data sheet status	18
15.2	Definitions	18
15.3	Disclaimers	18
15.4	Trademarks	19
16	Contact information	19
17	Contents	20

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2016.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 9 August 2016

Document identifier: 74HC_HCT112