# SN74LV8154 Dual 16-Bit Binary Counters With 3-State Output Registers

**Check for Samples: SN74LV8154**

## 1 Features

- Can Be Used as Two 16-Bit Counters or a Single 32-Bit Counter
- 8 bit counter read bus
- 2-V to 5.5-V $V_{CC}$ Operation
- Maximum $t_{pd}$ of 25 ns at 5 V (RCLK to Y)
- Typical $V_{OLP}$ (Output Ground Bounce)
  < 0.7 V at $V_{CC}$ = 5 V, $T_A$ = 25°C
- Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot)
  > 4.4 V at $V_{CC}$ = 5 V, $T_A$ = 25°C
- $I_{off}$ Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- Up Counters
- Dual Up Counters

## 3 Description

The SN74LV8154 device is a dual 16-bit binary counter with 3-state output registers, designed for 2-V to 5.5-V $V_{CC}$ operation.

The counters have dedicated clock inputs. The counters share a clocked storage register to sample and save the counter contents. Both counters share an asynchronous clear input. The 32-bit storage register can be mapped on the output bus 8-bits at a time. Four bus reads are needed to access the contents of both stored counts. The two counters can be chained by connecting $\overline{CLKBEN}$ to $\overline{RCOA}$. All clocks are positive edge triggered. All other inputs are active low.

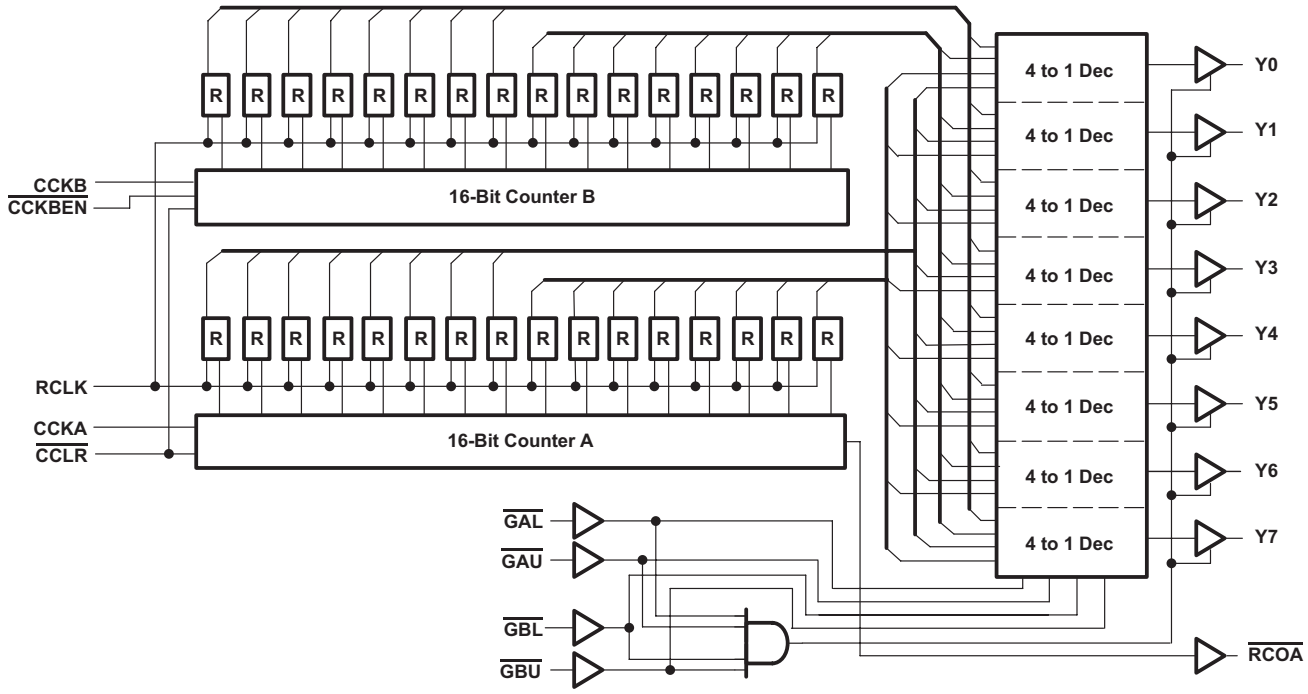
This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LV8154N | PDIP (20) | 6.50 mm x 4.40 mm |
| SN74LV8154PW | TSSOP (20) | 26.92 mm x 6.35 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (August 2004) to Revision A | Page |
|---|---|
| • Added *Pin Configuration and Functions* section, *Storage Conditions* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |
| • Removed *Ordering Information* table | 1 |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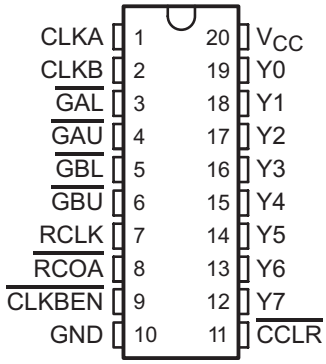
# 5 Pin Configuration and Functions

**N or PW Package**
**20-Pin PDIP or TSSOP**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $\overline{CCLR}$ | 11 | I | Clock clear, asyncrounous active-low clear for both counters |
| CLKA | 1 | I | Clock A, rising edge count clock |
| CLKB | 2 | I | Clock B, rising edge count clock |
| $\overline{CLKBEN}$ | 9 | I | Clock B enable, acitive-low allows clocking for counter B; connect to $\overline{RCOA}$ for 32-bit counter. |
| $\overline{GAL}$ | 3 | I | Gate A lower byte, acitve-low puts lower byte of stored counter A on the Y bus. |
| $\overline{GAU}$ | 4 | I | Gate A upper byte, acitve-low puts upper byte of stored counter A on the Y bus. |
| $\overline{GBL}$ | 5 | I | Gate B lower byte, acitve-low puts lower byte of stored counter B on the Y bus. |
| $\overline{GBU}$ | 6 | I | Gate B upper byte, acitve-low puts upper byte of stored counter B on the Y bus. |
| GND | 10 | — | Ground |
| RCLK | 7 | I | Register Clock, rising edge stores counters into an internal storage register |
| $\overline{RCOA}$ | 8 | O | Ready case overflow A, active low when counter A is full count and ready to overflow on next clock A |
| $V_{CC}$ | 20 | — | Power supply pin |
| Y0 | 19 | O | Data output bit 0 (LSB) |
| Y1 | 18 | O | Data output bit 1 |
| Y2 | 17 | O | Data output bit 2 |
| Y3 | 16 | O | Data output bit 3 |
| Y4 | 15 | O | Data output bit 4 |
| Y5 | 14 | O | Data output bit 5 |
| Y6 | 13 | O | Data output bit 6 |
| Y7 | 12 | O | Data output bit 7 (MSB) |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $V_I$ | Input voltage(2) | | –0.5 | 7 | V |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state(2) | | –0.5 | 7 | V |
| $V_O$ | Output voltage(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±35 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±70 | mA |
| $T_J$ | Junction Temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions(1)

| | | | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 V | 1.5 | | V |
| | | | 3 V to 3.6 V | $V_{CC}$ × 0.7 | | |
| | | | 4.5 V to 5.5 V | $V_{CC}$ × 0.7 | | |
| $V_{IL}$ | Low-level input voltage | | 2 V | | 0.5 | V |
| | | | 3 V to 3.6 V | | $V_{CC}$ × 0.3 | |
| | | | 4.5 V to 5.5 V | | $V_{CC}$ × 0.3 | |
| $V_I$ | Input voltage | | | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | | 0 | $V_{CC}$ | V |
| | | 3-state | | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | | 2 V | | –50 | µA |
| | | | 3 V to 3.6 V | | –6 | mA |
| | | | 4.5 V to 5.5 V | | –12 | |
| $I_{OL}$ | Low-level output current | | 2 V | | 50 | µA |
| | | | 3 V to 3.6 V | | 6 | mA |
| | | | 4.5 V to 5.5 V | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise and fall rate | | 3 V to 3.6 V | | 100 | ns/V |
| | | | 4.5 V to 5.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.


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## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74LV8154N N (PDIP) 20 PINS | SN74LV8154PW PW (TSSOP) 20 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 54.9 | 100.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 46.5 | 30.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 35.9 | 47.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 23.5 | 1.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 35.7 | 46.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage | $I_{OH}$ = –50 µA | | 2 V | 1.9 | | | V |
| | | $I_{OH}$ = –6 mA | | 3 V | 2.48 | | | |
| | | $I_{OH}$ = –12 mA | | 4.5 V | 3.8 | | | |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 50 µA | | 2 V | | | 0.1 | V |
| | | $I_{OL}$ = 6 mA | | 3 V | | | 0.44 | |
| | | $I_{OL}$ = 12 mA | | 4.5 V | | | 0.55 | |
| $I_I$ | Input current | $V_I$ = 5.5 V or GND | | 0 to 5.5 V | | | ±1 | µA |
| $I_{OZ}$ | Output off current | $V_O = V_{CC}$ or GND | | 5.5 V | | | ±5 | µA |
| $I_{CC}$ | Supply current | $V_I = V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | | 20 | µA |
| $I_{off}$ | Off current | $V_I$ or $V_O$ = 0 to 5.5 V | | 0 | | | 5 | µA |
| $C_I$ | Input capacitance | $V_I = V_{CC}$ or GND | | 5 V | | 3 | | pF |
| $C_o$ | Output capacitance | $V_O = V_{CC}$ or GND | | 5 V | | 5 | | pF |
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = No load, | CCLK = 10 MHz<br>RCLK = 1 MHz | 5 V | | 56 | | pF |

## 6.6 Timing Requirements

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

| | | | MIN | UNIT |
|---|---|---|---|---|
| $t_w$ | Pulse duration | CLKA, CLKB, RCLK high or low | 10 | ns |
| | | $\overline{CCLR}$ low | 20 | |
| $t_{su}$ | Set-up time | $\overline{CLKBEN}$ low before CLKB↑ | 10 | ns |
| | | $\overline{CCLR}$ high (inactive) before CLKA↑or CLKB↑ | 10 | |
| | | CLKA↑ or CLKB↑ before RCLK↑ | 10 | |
| | | RCLK↑ before $\overline{GAL}$ or $\overline{GAU}$ or $\overline{GBL}$ or $\overline{GBU}$ low | 10 | |
| | | $\overline{GAL}$ or $\overline{GAU}$ or $\overline{GBL}$ or $\overline{GBU}$ high (inactive) before RCLK↑ | 10 | |
| $t_h$ | Hold time | $\overline{CLKBEN}$ low after CLKB↑ | 0 | ns |
| | | CLKA or CLKB after RCLK | 0 | |
| $t_z$[1] | Z-period | $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$ all high before one of them switches low | 200 | ns |

(1) $t_z$ condition: $C_L$ = 50 pF, $R_L$ = 1 kΩ

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## 6.7 Switching Characteristics - $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | | | $C_L$ = 15 pF | 40 | | | MHz |
| | | | $C_L$ = 50 pF | 25 | | | |
| $t_{pd}$ | RCLK | Y | $C_L$ = 15 pF | 1 | 22 | 38 | ns |
| | CLKA | $\overline{RCOA}$ | | 1 | 26 | 44 | |
| $t_{PLH}$ | $\overline{CCLR}$ | $\overline{RCOA}$ | | 1 | 18 | 32 | ns |
| $t_{en}$ | $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$ | Y | | 1 | 27 | 46 | ns |
| $t_{dis}$ | $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$ | Y | | 1 | 12 | 21 | ns |
| $t_{pd}$ | RCLK | Y | $C_L$ = 50 pF | 1 | 25 | 42 | ns |
| | CLKA | $\overline{RCOA}$ | | 1 | 28 | 46 | |
| $t_{PLH}$ | $\overline{CCLR}$ | $\overline{RCOA}$ | | 1 | 20 | 35 | ns |
| $t_{en}$ | $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$ | Y | | 1 | 30 | 50 | ns |
| $t_{dis}$ | $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$ | Y | | 1 | 14 | 24 | ns |

## 6.8 Switching Characteristics $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | | | $C_L$ = 15 pF | 40 | | | MHz |
| | | | $C_L$ = 50 pF | 25 | | | |
| $t_{pd}$ | RCLK | Y | $C_L$ = 15 pF | 1 | 14 | 25 | ns |
| | CLKA | $\overline{RCOA}$ | | 1 | 16 | 27 | |
| $t_{PLH}$ | $\overline{CCLR}$ | $\overline{RCOA}$ | | 1 | 12 | 20 | ns |
| $t_{en}$ | $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$ | Y | | 1 | 16 | 28 | ns |
| $t_{dis}$ | $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$ | Y | | 1 | 8 | 15 | ns |
| $t_{pd}$ | RCLK | Y | $C_L$ = 50 pF | 1 | 16 | 27 | ns |
| | CLKA | $\overline{RCOA}$ | | 1 | 17 | 28 | |
| $t_{PLH}$ | $\overline{CCLR}$ | $\overline{RCOA}$ | | 1 | 13 | 21 | ns |
| $t_{en}$ | $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$ | Y | | 1 | 18 | 30 | ns |
| $t_{dis}$ | $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$ | Y | | 1 | 9 | 16 | ns |

## 6.9 Noise Characteristics

$V_{CC}$ = 5 V, $C_L$ = 50 pF

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.7 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.75 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.4 | | V |


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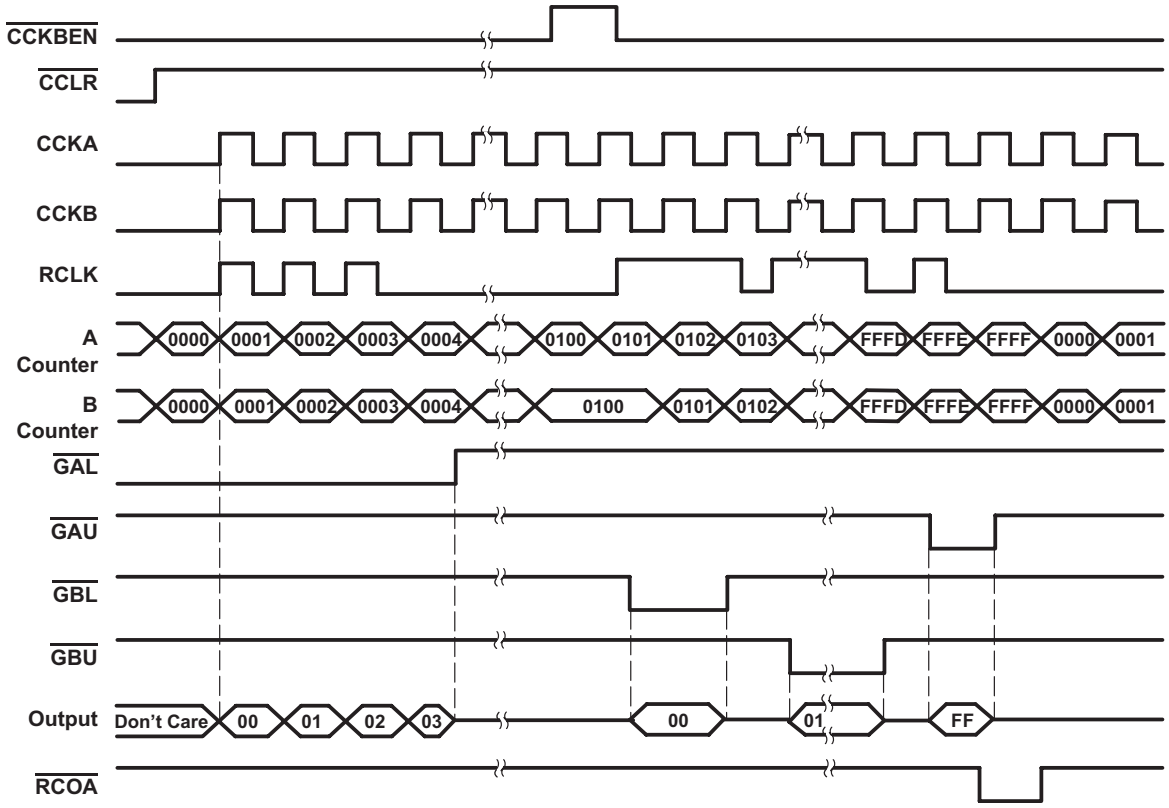
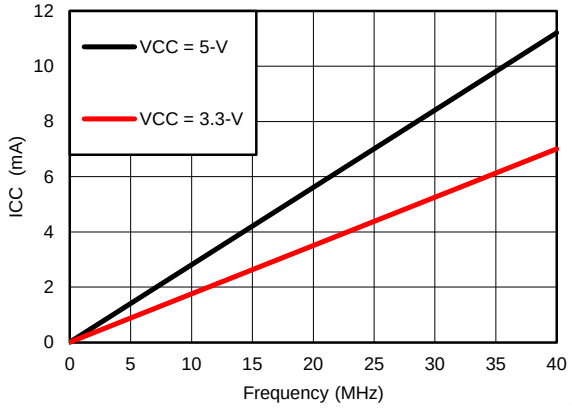



**Figure 1. Timing Diagram**

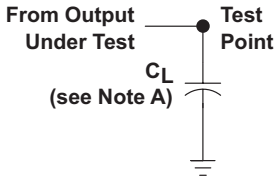
## 6.10 Typical Characteristics



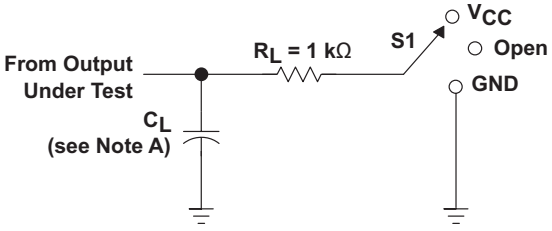

RCLK = CLKA,B / 10; No load

**Figure 2. ICC vs CLKA, CLKB Frequency**

# 7 Parameter Measurement Information

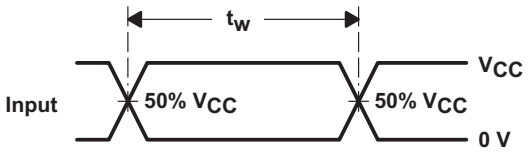



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

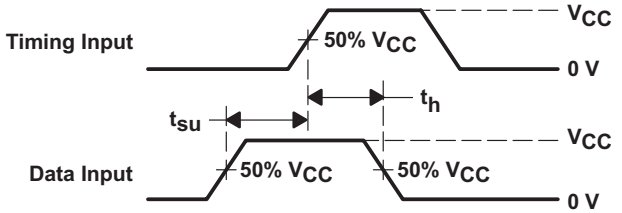



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

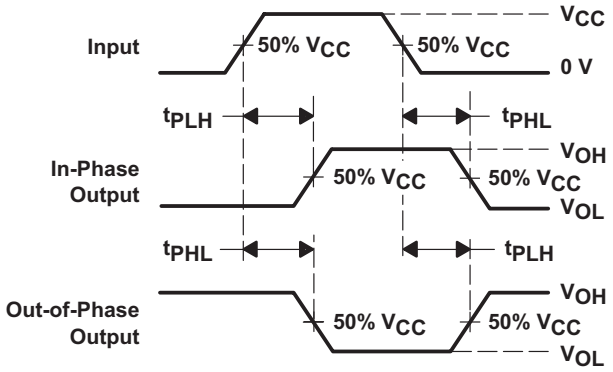
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



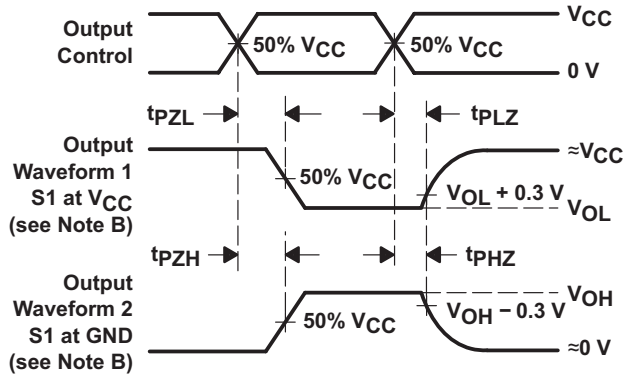

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**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# 8 Detailed Description

## 8.1 Overview

The SN74LV8154 device is a dual 16-bit binary counter with 3-state output registers, designed for 2-V to 5.5-V $V_{CC}$ operation. The counters have dedicated clock inputs. The counters share a storage register clock and an asynchronous clear input. The 32-bit storage register can be mapped on the output bus 8-bit at a time. Four bus reads are needed to access the contents of both counters. The two counters can be chained by connecting $\overline{CLKBEN}$ to $\overline{RCOA}$

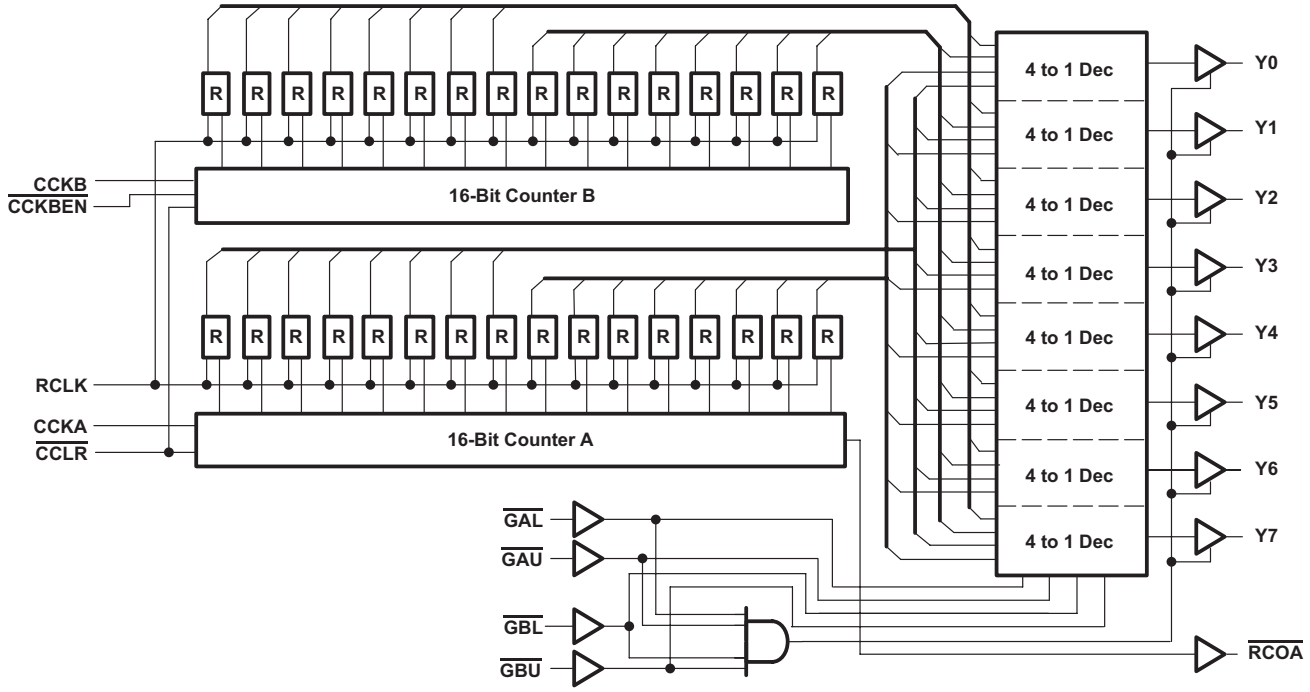
This 16-bit counter (A or B) feeds a 16-bit storage register, and each storage register is further divided into an upper byte and lower byte. The $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$ inputs are used to select the byte that needs to be output at Y0−Y7. CLKA is the clock for A counter, and CLKB is the clock for B counter. RCLK is the clock for the A and B storage registers. All three clock signals are positive-edge triggered.

A 32-bit counter can be realized by connecting CLKA and CLKB together and by connecting $\overline{RCOA}$ to $\overline{CLKBEN}$.

To ensure the high-impedance state during power up or power down, $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, and $\overline{GBU}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

Two 16-bit counters count up on each positive edge of the respective clock input. $\overline{RCOA}$ is set low when counter A is full count. Counter B clock is gated by the $\overline{CCKBEN}$ input. Connecting $\overline{RCOA}$ to $\overline{CCKBEN}$ together chains the counters to make one 32-bit counter.

Asynchronous $\overline{CCLR}$ input resets both counter to zero.

One 32-bit storage register records the contents of both counters on the rising edge of RCLK. The contents of the storage register are saved until the next rising edge of the RCLK.

Mapped output bus can be set to high impedance or output 8-bits of the 32-bit storage register.

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## 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LV8154.

**Table 1. Function Table**

| INPUTS | | | | OUTPUT Yn |
|---|---|---|---|---|
| $\overline{GAL}$ | $\overline{GAU}$ | $\overline{GBL}$ | $\overline{GBU}$ | |
| L | H | H | H | Lower byte in A storage register |
| H | L | H | H | Upper byte in A storage register |
| H | H | L | H | Lower byte in B storage register |
| H | H | H | L | Upper byte in B storage register |
| H | H | H | H | Z |


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# 9 Application and Implementation

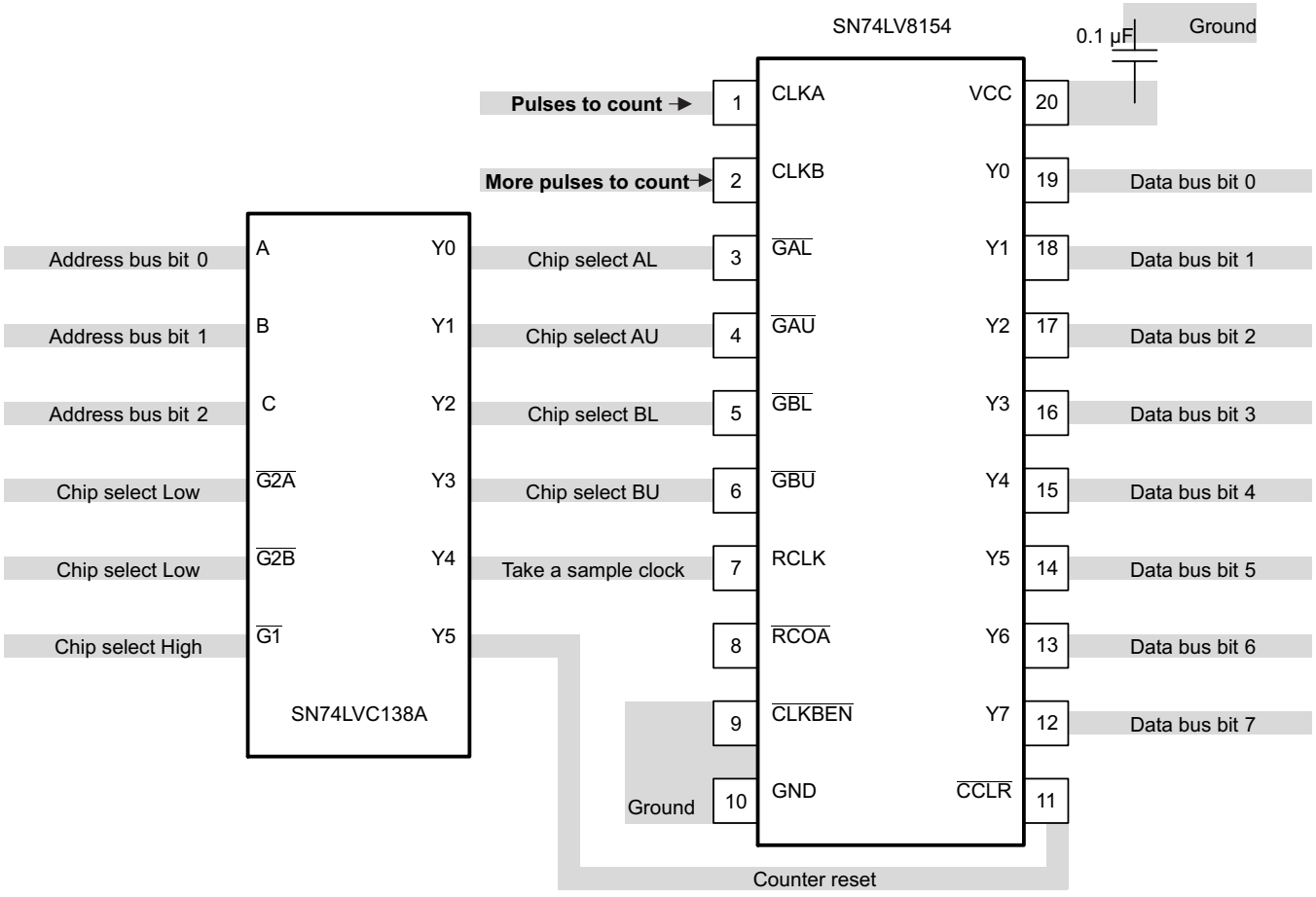
**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LV8154 can count any two events up to a count of 65,535 per storage register read. It can also count one event up to a count of 4,294,967,295 per storage register read.

## 9.2 Typical Application




**Dual Counter With Address Mapping**

### 9.2.1 Design Requirements

- $V_{CC}$ must be acceptable for both SN74LV8154 and SN74LVC138A.
- $\overline{CCLR}$ low time must be greater than 20 ns.
- 8 bytes of unique address space are needed.
- CLKA and CLKB inputs must have input transition rate specified in *Recommended Operating Conditions*.
- RCLK and $\overline{CCLR}$ inputs must be free of glitches to prevent accidental register saves or counter clears.

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## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

- Connect Y0 through Y7 to the data bus.
- Connect A, B, and C to lower address bus lines.
- Connect $\overline{G2A}$, $\overline{G2B}$, and G1 to decoded addresses to provide 8 or more unique memory locations.
- Connect two pulse sources to CLKA and CLKB inputs. If sources have noise or slow edges then pass the signal through a Schmitt trigger buffer first.
- If only one counter is needed, connect the single pulse source to both CLKA and CLKB.
- Also connect $\overline{CLKBEN}$ to $\overline{RCOA}$ instead of ground.

**Table 2. Function Table**

| INPUTS(1) | | | | | | OUTPUT(1) | RESULT |
|---|---|---|---|---|---|---|---|
| G1 | $\overline{G2A}$ | $\overline{G2B}$ | C | B | A | Yn | |
| L | X | X | X | X | X | Z | No action |
| X | H | X | X | X | X | Z | No action |
| X | X | H | X | X | X | Z | No action |
| H | L | L | L | L | L | A lower byte | Read lower byte of counter A storage register |
| H | L | L | L | L | H | A upper byte | Read upper byte of counter A storage register |
| H | L | L | L | H | L | B lower byte | Read lower byte of counter B storage register |
| H | L | L | L | H | H | B upper byte | Read upper byte of counter B storage register |
| H | L | L | H | L | L | Z | Save counters into storage register after changing any input |
| H | L | L | H | L | H | Z | Reset both counters to zero |
| H | L | L | H | H | L | Z | No action |
| H | L | L | H | H | H | Z | No action |

(1) L = low, H = high, X = don't care, Z = high Impedance.

### 9.2.3 Application Curve

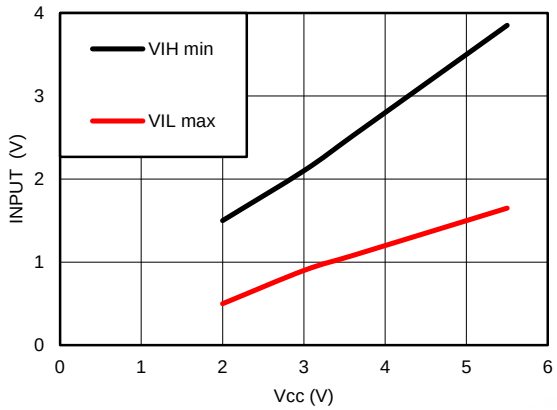


**Figure 4. Input Voltage Range vs $\overline{VCC}$**


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# 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions* table.

Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended. If there are multiple $V_{CC}$ terminals then 0.01-µF or 0.022-µF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

# 11 Layout

## 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 5 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient.

## 11.2 Layout Example

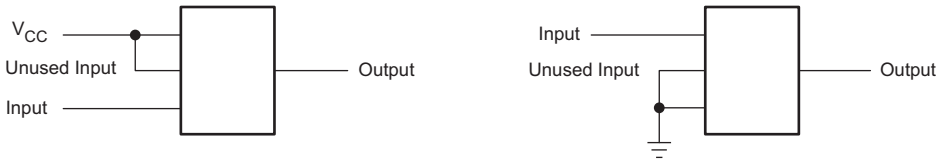


**Figure 5. Layout Diagram**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation, see the following:

*Implications of Slow or Floating CMOS Inputs*, SCBA004

## 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV8154N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74LV8154N | Samples |
| SN74LV8154NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74LV8154N | Samples |
| SN74LV8154PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV8154 | Samples |
| SN74LV8154PWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV8154 | Samples |
| SN74LV8154PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV8154 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LV8154 :**

- Enhanced Product: SN74LV8154-EP

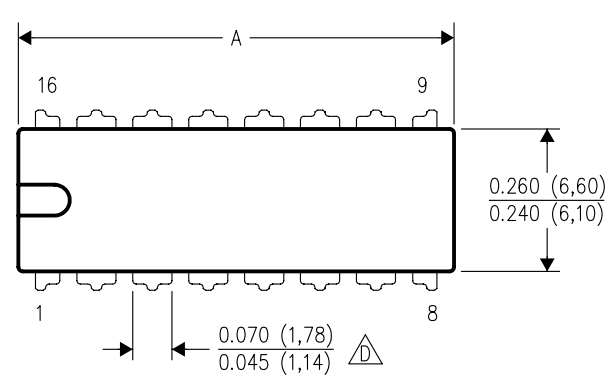
NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

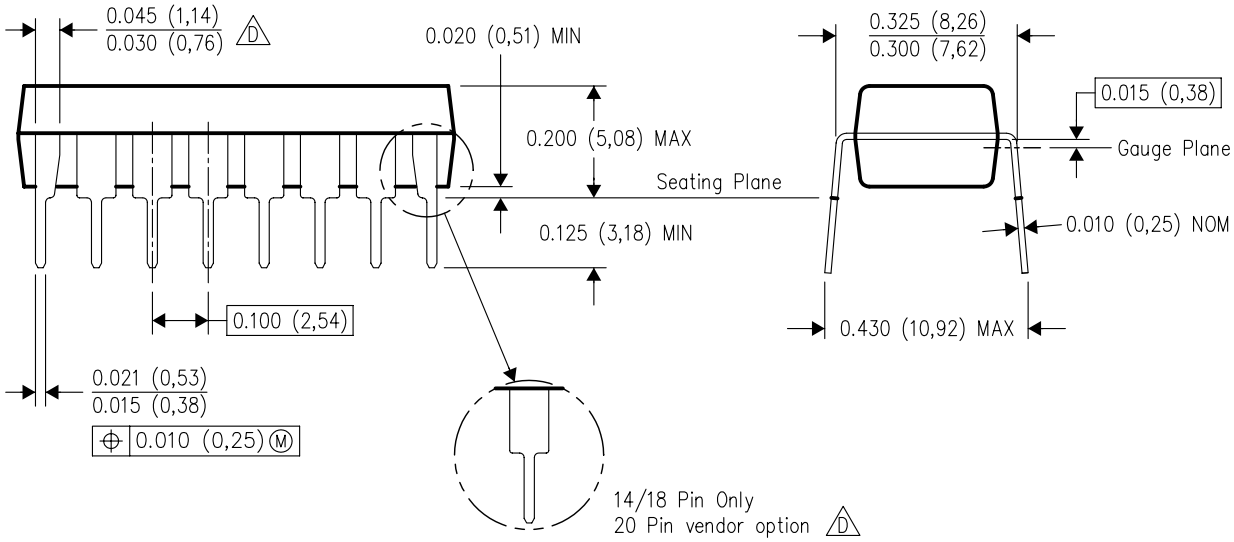
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



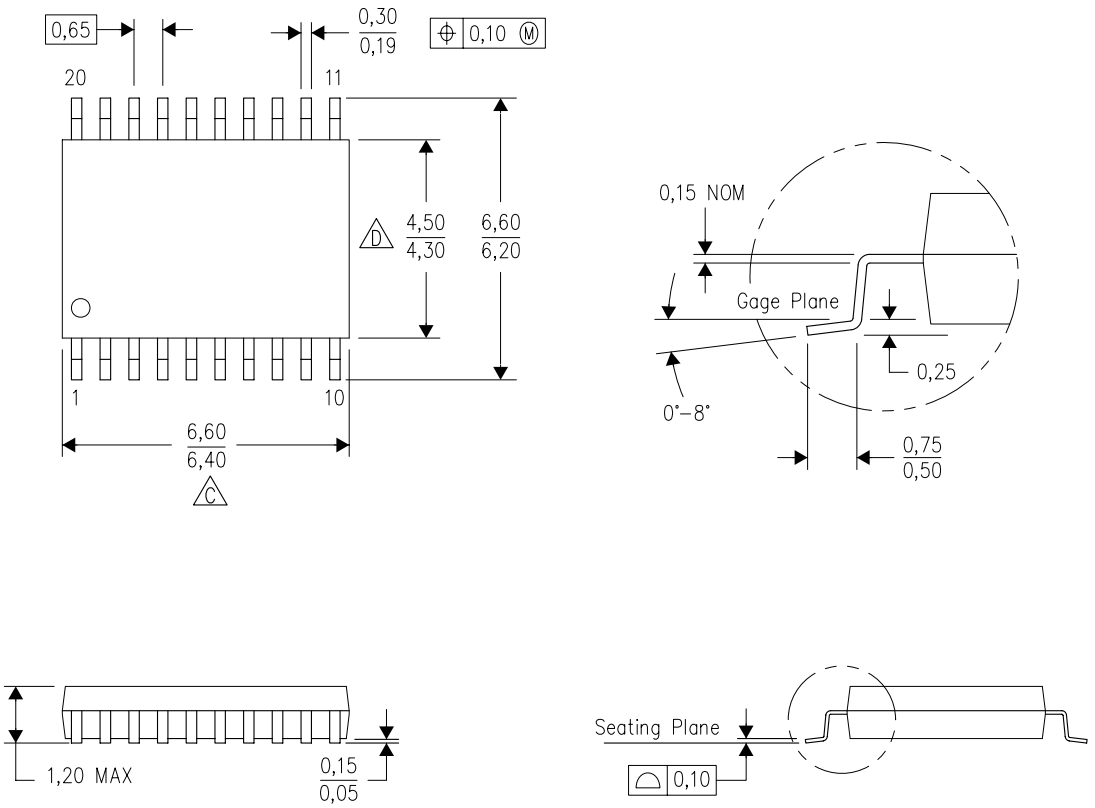

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

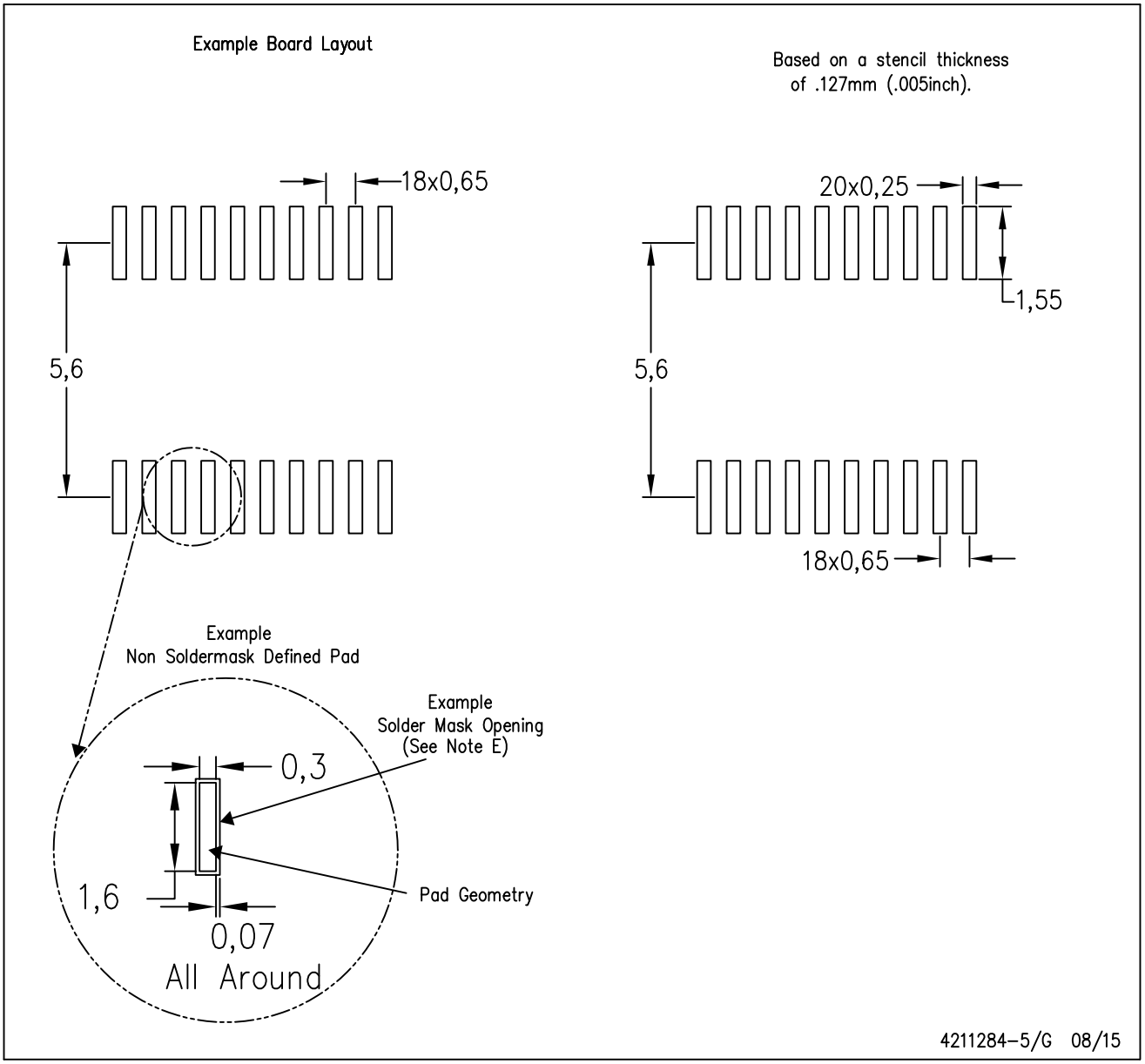
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE




4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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