74HC193; 74HCT193

Presettable synchronous 4-bit binary up/down counter

Product data sheet

1. General description

The 74HC193 and 74HCT193 are high-speed Si-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC193 and 74HCT193 are 4-bit synchronous binary up/down counters. Separate up/down clocks, CPU and CPD respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CPU clock is pulsed while CPD is held HIGH, the device will count up. If the CPD clock is pulsed while CPU is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$).

The 74HC193 and 74HCT193 each contain four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CPD input will decrease the count by one, while a similar transition on the CPU input will advance the count by one.

One clock should be held HIGH while counting with the other, otherwise the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up ($\overline{TCU}$) and terminal count down ($\overline{TCD}$) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CPU will cause $\overline{TCU}$ to go LOW.

$\overline{TCU}$ will stay LOW until CPU goes HIGH again, duplicating the count up clock.

Likewise, the $\overline{TCD}$ output will go LOW when the circuit is in the zero state and the CPD goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs (Q0 to Q3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q0 to

Q3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

2. Features

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC193D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC193DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC193N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC193PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT193D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT193DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT193N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT193PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

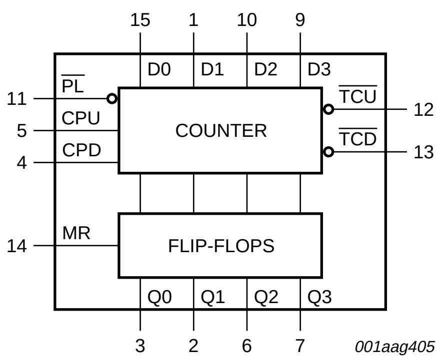


Fig 1. Functional diagram

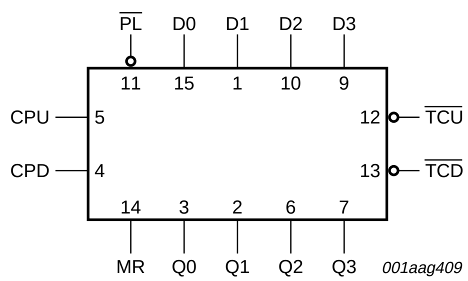


Fig 2. Logic symbol

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	DIP16 package	[2]	-	750	mW
		SO16 package	[2]	-	500	mW
		SSOP16 package	[2]	-	500	mW
		TSSOP16 package	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP16 packages: above 70 °C the value of P_{tot} derates linearly at 12 mW/K.
For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
For SSOP16 and TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC193						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r	rise time	inputs				
		$V_{CC} = 2.0$ V	-	-	1000	ns
		$V_{CC} = 4.5$ V	-	6.0	500	ns
		$V_{CC} = 6.0$ V	-	-	400	ns
t_f	fall time	inputs				
		$V_{CC} = 2.0$ V	-	-	1000	ns
		$V_{CC} = 4.5$ V	-	6.0	500	ns
		$V_{CC} = 6.0$ V	-	-	400	ns

Table 5. Recommended operating conditions *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HCT193						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r	rise time	inputs; V_{CC} = 4.5 V	-	6.0	500	ns
t_f	fall time	inputs; V_{CC} = 4.5 V	-	6.0	500	ns

9. Static characteristics

Table 6. Static characteristics type 74HC193

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	-	-	-	
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	μA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V

Table 6. Static characteristics type 74HC193 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	µA
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	µA

10. Dynamic characteristics

Table 8. Dynamic characteristics type 74HC193

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	CPU, CPD to Qn; see Figure 9 [1]	-							
		V_{CC} = 2.0 V	-	63	215	-	270	-	325	ns
		V_{CC} = 4.5 V	-	23	43	-	54	-	65	ns
		V_{CC} = 6.0 V	-	18	37	-	46	-	55	ns
		CPU to $\overline{\mathrm{TCU}}$; see Figure 10								
		V_{CC} = 2.0 V	-	39	125	-	155	-	190	ns
		V_{CC} = 4.5 V	-	14	25	-	31	-	38	ns
		V_{CC} = 6.0 V	-	11	21	-	26	-	32	ns
		CPD to $\overline{\mathrm{TCD}}$; see Figure 10								
		V_{CC} = 2.0 V	-	39	125	-	155	-	190	ns
		V_{CC} = 4.5 V	-	14	25	-	31	-	38	ns
		V_{CC} = 6.0 V	-	11	21	-	26	-	32	ns
		$\overline{\mathrm{PL}}$ to Qn; see Figure 11								
		V_{CC} = 2.0 V	-	69	220	-	275	-	330	ns
		V_{CC} = 4.5 V	-	25	44	-	55	-	66	ns
		V_{CC} = 6.0 V	-	20	37	-	47	-	56	ns
		MR to Qn; see Figure 12								
		V_{CC} = 2.0 V	-	58	200	-	250	-	300	ns
		V_{CC} = 4.5 V	-	21	40	-	50	-	60	ns
		V_{CC} = 6.0 V	-	17	34		43	-	51	ns
		Dn to Qn; see Figure 11								
		V_{CC} = 2.0 V	-	69	210	-	265	-	315	ns
		V_{CC} = 4.5 V	-	25	42	-	53	-	63	ns
		V_{CC} = 6.0 V	-	20	36	-	45	-	54	ns
		$\overline{\mathrm{PL}}$ to $\overline{\mathrm{TCU}}$, $\overline{\mathrm{PL}}$ to $\overline{\mathrm{TCD}}$; see Figure 14								
		V_{CC} = 2.0 V	-	80	290	-	365	-	435	ns
		V_{CC} = 4.5 V	-	29	58	-	73	-	87	ns
		V_{CC} = 6.0 V	-	23	49	-	62	-	74	ns
		MR to $\overline{\mathrm{TCU}}$, MR to $\overline{\mathrm{TCD}}$; see Figure 14								
		V_{CC} = 2.0 V	-	74	285	-	355	-	430	ns
		V_{CC} = 4.5 V	-	27	57	-	71	-	86	ns
		V_{CC} = 6.0 V	-	22	48	-	60	-	73	ns

Table 8. Dynamic characteristics type 74HC193 *...continued*

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	Dn to $\overline{TCU}$, Dn to $\overline{TCD}$; see Figure 14								
		V_{CC} = 2.0 V	-	80	290	-	365	-	435	ns
		V_{CC} = 4.5 V	-	29	58	-	73	-	87	ns
		V_{CC} = 6.0 V	-	23	49	-	62	-	74	ns
t_{THL}	HIGH to LOW output transition time	see Figure 12								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_{TLH}	LOW to HIGH output transition time	see Figure 12								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	CPU, CPD (HIGH or LOW); see Figure 9								
		V_{CC} = 2.0 V	100	22	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	8	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	6	-	21	-	26	-	ns
		MR (HIGH); see Figure 12								
		V_{CC} = 2.0 V	100	25	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	9	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	7	-	21	-	26	-	ns
		$\overline{PL}$ (LOW); see Figure 11								
		V_{CC} = 2.0 V	100	19	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	7	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	6	-	21	-	26	-	ns
t_{rec}	recovery time	$\overline{PL}$ to CPU, CPD; see Figure 11								
		V_{CC} = 2.0 V	50	8	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	3	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	2	-	11	-	13	-	ns
		MR to CPU, CPD; see Figure 12								
		V_{CC} = 2.0 V	50	0	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	0	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	0	-	11	-	13	-	ns

Table 8. Dynamic characteristics type 74HC193 *…continued*

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	Dn to $\overline{PL}$; see Figure 13; note: CPU = CPD = HIGH									
		V_{CC} = 2.0 V		80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V		16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V		14	6	-	17	-	20	-	ns
t_h	hold time	Dn to $\overline{PL}$; see Figure 13									
		V_{CC} = 2.0 V		0	–14	-	0	-	0	-	ns
		V_{CC} = 4.5 V		0	–5	-	0	-	0	-	ns
		V_{CC} = 6.0 V		0	–4	-	0		0	-	ns
		CPU to CPD, CPD to CPU; see Figure 15									
		V_{CC} = 2.0 V		80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V		16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V		8	6	-	17	-	20	-	ns
f_{max}	maximum frequency	CPU, CPD; see Figure 9									
		V_{CC} = 2.0 V		4.0	13.5	-	3.2	-	2.6	-	MHz
		V_{CC} = 4.5 V		20	41	-	16	-	13	-	MHz
		V_{CC} = 6.0 V		24	49	-	19	-	15	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; f_i = 1 MHz	[2]	-	24	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

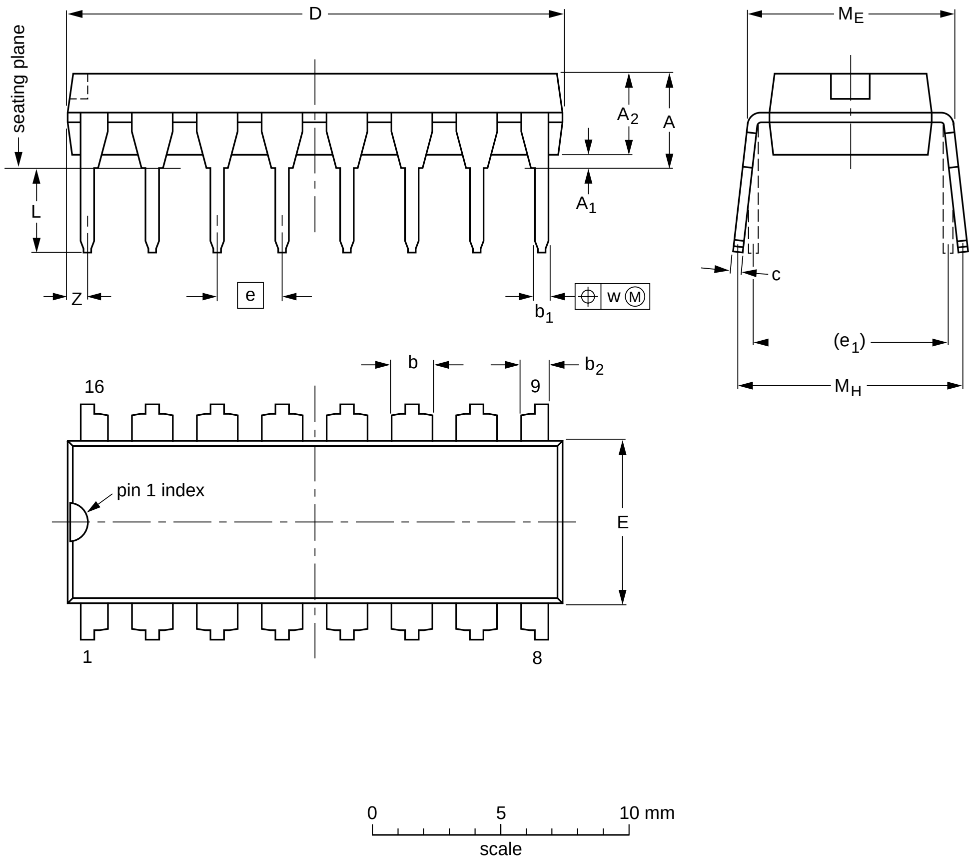
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT38-4						

Fig 20. Package outline SOT38-4 (DIP16)