74HC73

Dual JK flip-flop with reset; negative-edge trigger

Rev. 5 — 2 December 2015 Product data sheet

1. General description

The 74HC73 is a dual negative edge triggered JK flip-flop with individual J, K, clock ($n\overline{CP}$) and reset ($n\overline{R}$) inputs and complementary nQ and $n\overline{Q}$ outputs. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. ($n\overline{R}$) is asynchronous, when LOW it overrides the clock and data inputs, forcing the nQ output LOW and the $n\overline{Q}$ output HIGH. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC73D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC73DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HC73PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

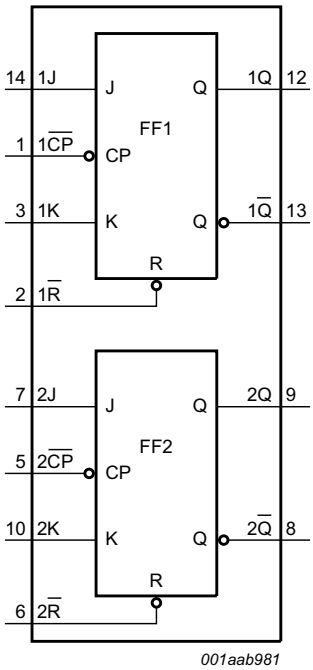

Fig 1. Functional diagram

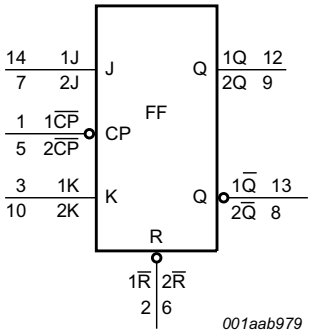

Fig 2. Logic symbol

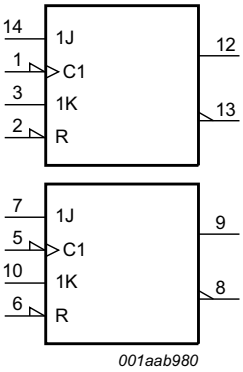

Fig 3. IEC logic symbol

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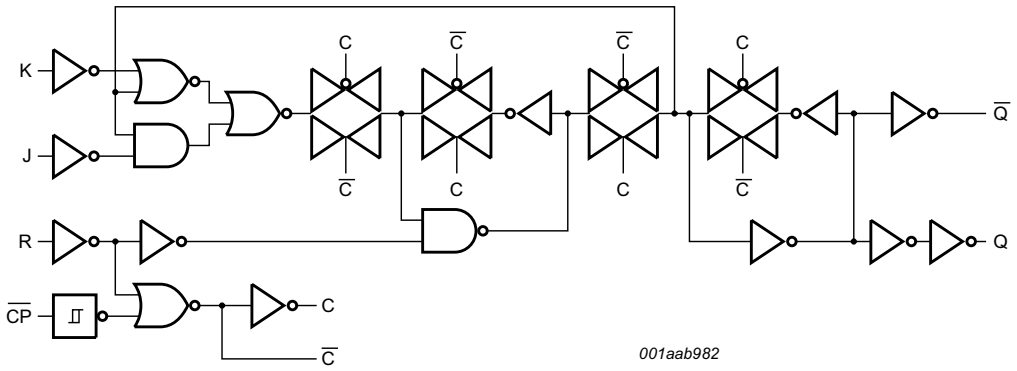

Fig 4. Logic diagram (one flip-flop)

5. Pinning information

5.1 Pinning

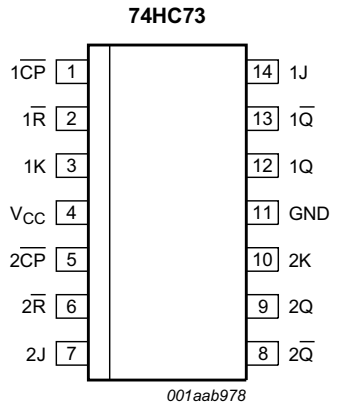

Fig 5. Pin configuration SO14, SSOP14 and TSSOP14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1CP, 2CP	1, 5	clock input (HIGH-to-LOW edge-triggered); also referred to as nCP
1R, 2R	2, 6	asynchronous reset input (active LOW); also referred to as nR
1K, 2K	3, 10	synchronous K input; also referred to as nK
V_{CC}	4	positive supply voltage
GND	11	ground (0 V)
1Q, 2Q	12, 9	true output; also referred to as nQ
1Q, 2Q	13, 8	complement output; also referred to as nQ
1J, 2J	14, 7	synchronous J input; also referred to as nJ

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6. Functional description

Table 3. Function table[1]

Input				Output		Operating mode
$n\overline{R}$	$n\overline{CP}$	nJ	nK	nQ	$n\overline{Q}$	
L	X	X	X	L	H	asynchronous reset
H	↓	h	h	$\overline{q}$	q	toggle
H	↓	l	h	L	H	load 0 (reset)
H	↓	h	l	H	L	load 1 (set)
H	↓	l	l	q	$\overline{q}$	hold (no change)

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;
q = state of referenced output one set-up time prior to the HIGH-to-LOW clock transition;
X = don't care;
↓ = HIGH-to-LOW clock transition.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C				
		SO14 package	[2]	-	500	mW
		(T)SSOP14 package	[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	4.0	-	40.0	-	80.0	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 8

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	$n\overline{CP}$ to nQ; see Figure 6 [1]								
		V_{CC} = 2.0 V	-	52	160	-	200	-	240	ns
		V_{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V_{CC} = 6.0 V	-	15	27	-	34	-	41	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
		$n\overline{CP}$ to $n\overline{Q}$; see Figure 6								
		V_{CC} = 2.0 V	-	52	160	-	200	-	240	ns
		V_{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V_{CC} = 6.0 V	-	15	27		34	-	41	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	-				ns
		$n\overline{R}$ to nQ, $n\overline{Q}$; see Figure 7								
		V_{CC} = 2.0 V	-	50	145	-	180	-	220	ns
		V_{CC} = 4.5 V	-	18	29	-	36	-	44	ns
		V_{CC} = 6.0 V	-	14	25		31	-	38	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
t_t	transition time	nQ, $n\overline{Q}$; see Figure 6 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13		16	-	19	ns
t_W	pulse width	$n\overline{CP}$ input, HIGH or LOW; see Figure 6								
		V_{CC} = 2.0 V	80	22	-	100		120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20		ns
		$n\overline{R}$ input, HIGH or LOW; see Figure 7								
		V_{CC} = 2.0 V	80	22	-	100		120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20		ns
t_{rec}	recovery time	$n\overline{R}$ to $n\overline{CP}$; see Figure 7								
		V_{CC} = 2.0 V	80	22	-	100		120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20		ns
t_{su}	set-up time	nJ, nK to $n\overline{CP}$; see Figure 6								
		V_{CC} = 2.0 V	80	22	-	100		120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20		ns

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Table 7. Dynamic characteristics *...continued*

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 8

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_h	hold time	nJ, nK to $n\overline{CP}$; see Figure 6								
		V_{CC} = 2.0 V	3	–8	-	3		3	-	ns
		V_{CC} = 4.5 V	3	–3	-	3	-	3	-	ns
		V_{CC} = 6.0 V	3	–2	-	3	-	3		ns
f_{max}	maximum frequency	$n\overline{CP}$ input; see Figure 6								
		V_{CC} = 2.0 V	6.0	23	-	4.8		4.0	-	MHz
		V_{CC} = 4.5 V	30	70	-	24	-	20	-	MHz
		V_{CC} = 6.0 V	35	83	-	28	-	24	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	77	-		-		-	MHz
C_{PD}	power dissipation capacitance	per flip-flop; V_I = GND to V_{CC} [3]	-	30	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

[2] t_t is the same as t_{THL}, t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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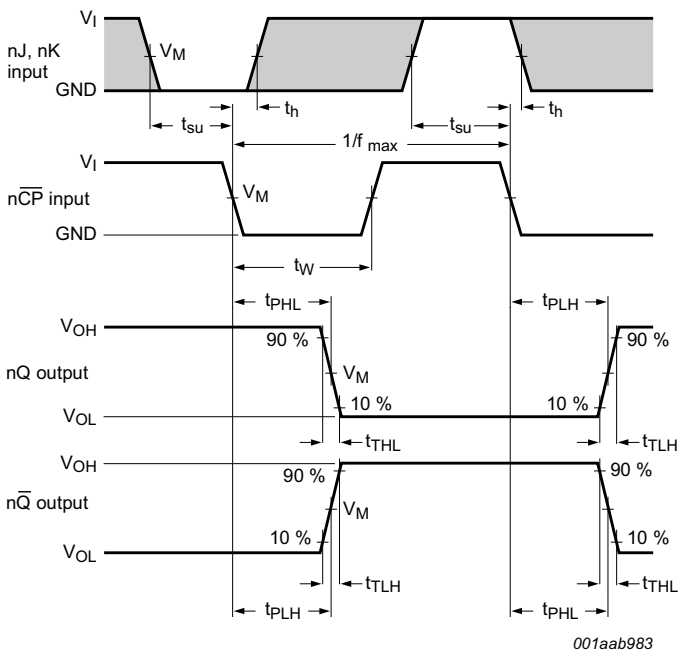
11. Waveforms

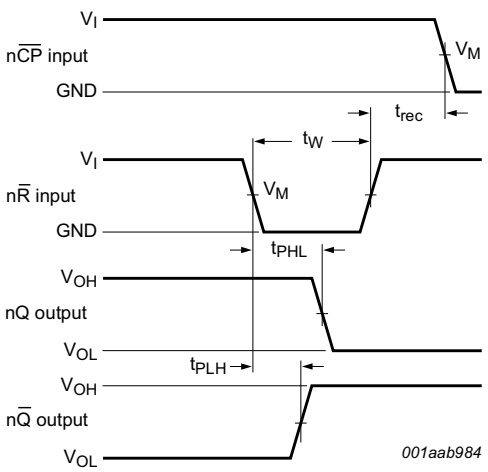


The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Waveforms showing the clock (nCP) to output (nQ, nQ) propagation delays, the clock pulse width, the J and K to nCP set-up and hold times, the output transition times and the maximum clock frequency



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Waveforms showing the reset (nR) input to output (nQ, nQ) propagation delays and the reset pulse width and the nR to nCP removal time

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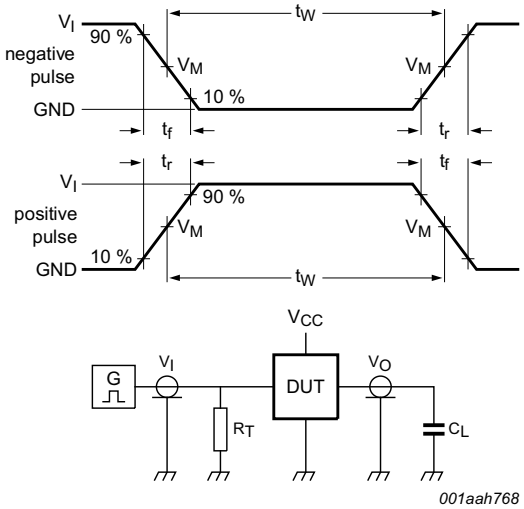
Table 8. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC73	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 9.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load
	V_I	t_r, t_f	C_L
74HC73	V_{CC}	6 ns	15 pF, 50 pF

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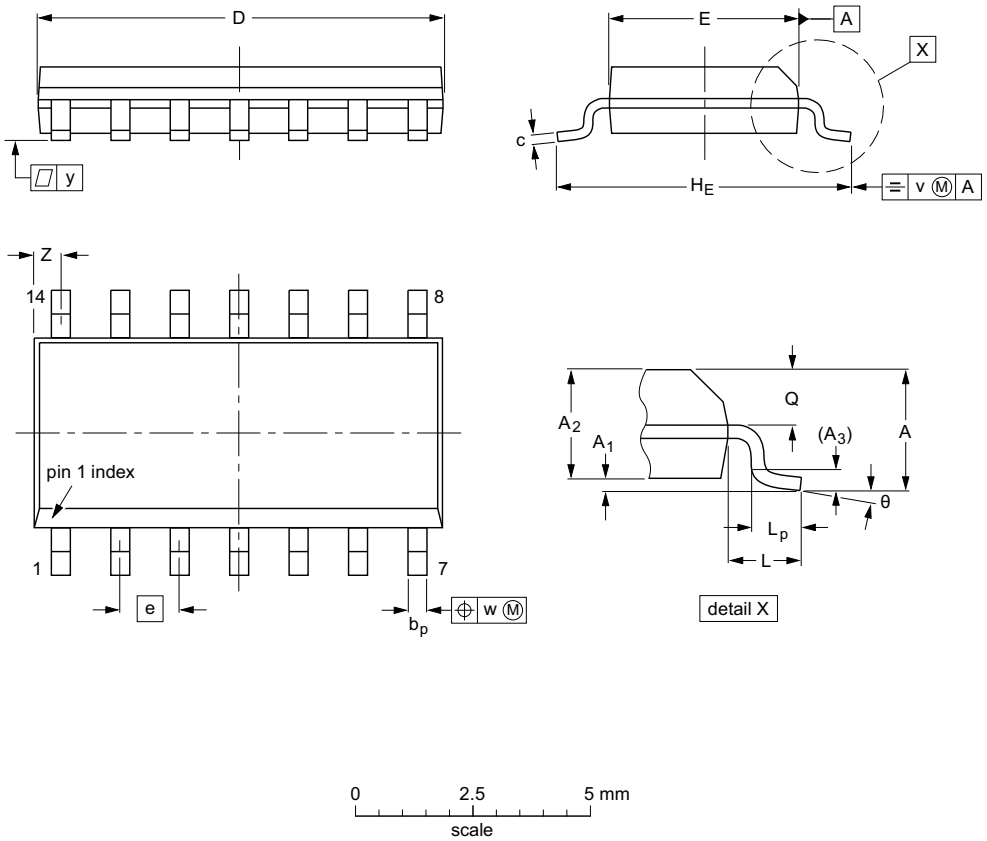
12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT108-1 (SO14)

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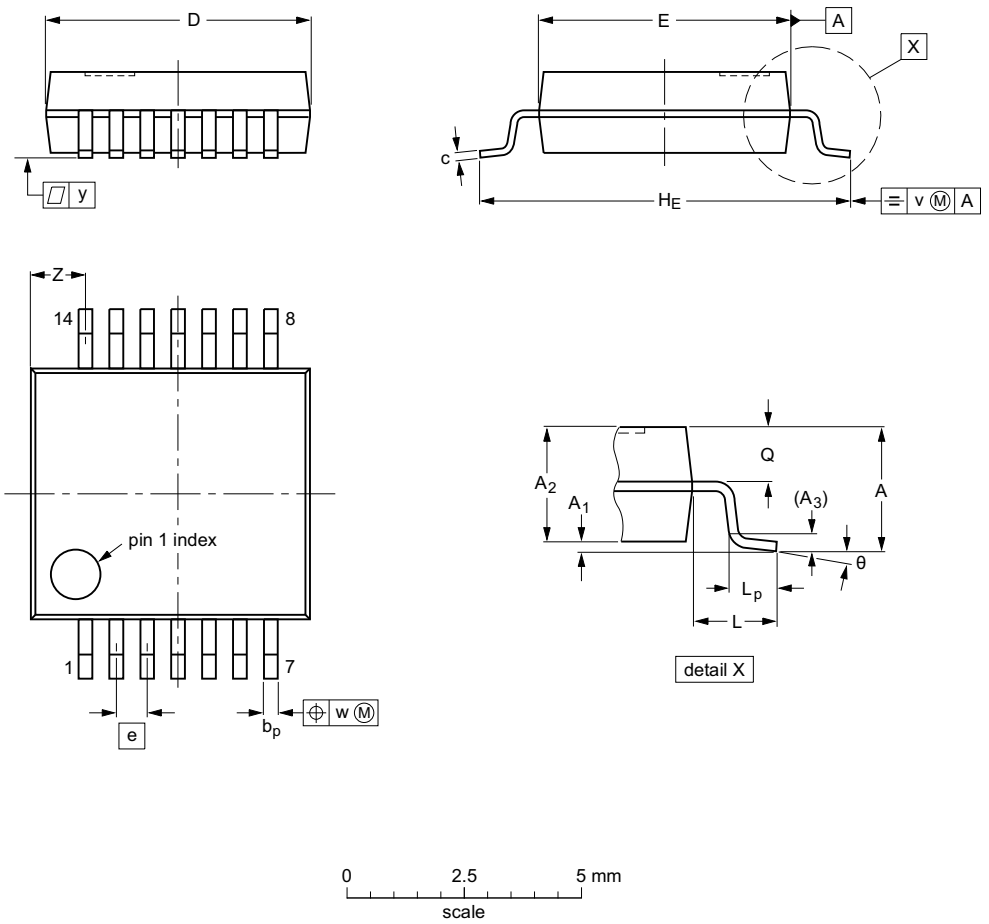
SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT337-1 (SSOP14)

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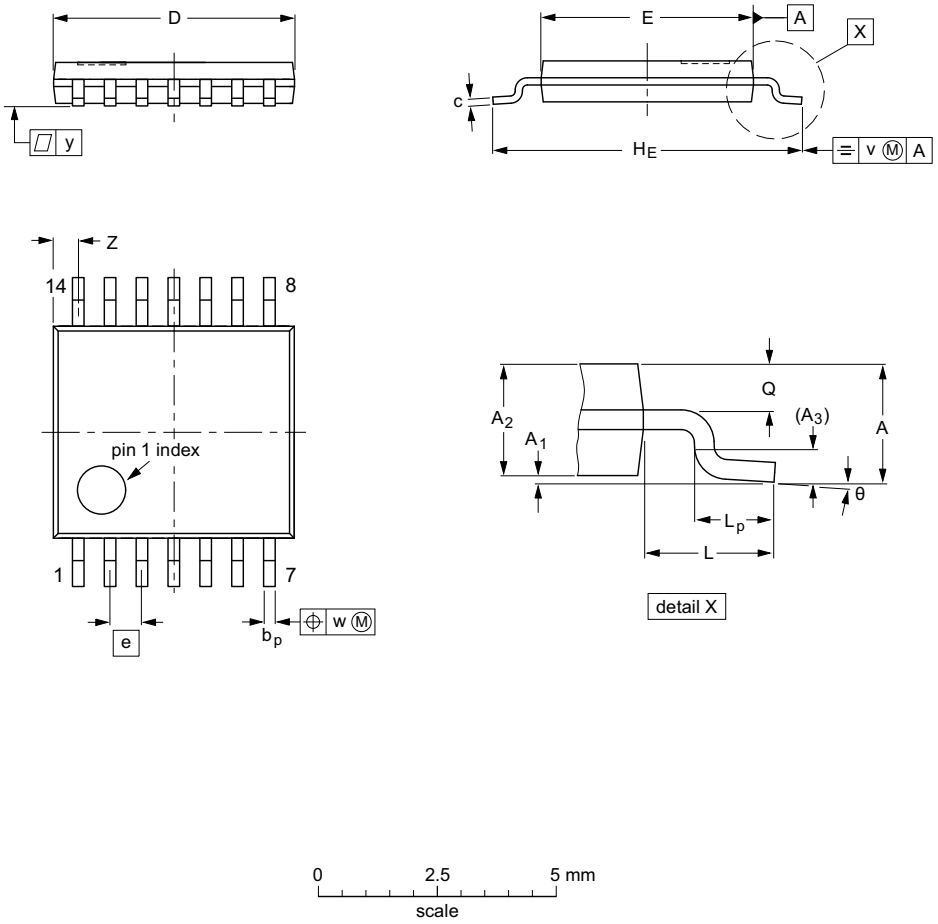
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT402-1 (TSSOP14)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC73 v.5	20151202	Product data sheet	-	74HC73 v.4
Modifications:	• Type number 74HC73N (SOT27-1) removed.			
74HC73 v.4	20080319	Product data sheet	-	74HC73 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Quick reference data incorporated into Section 9 and 10. • Section 8 “Recommended operating conditions” t_r, t_f converted to $\Delta t/\Delta V$.			
74HC73 v.3	20041112	Product data sheet	-	74HC_HCT73_CNV v.2
74HC_HCT73_CNV v.2	December 1990	Product specification	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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For sales office addresses, please send an email to: **salesaddresses@nexperia.com**

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