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Kind regards,

Team Nexperia

74HC1G125-Q100; 74HCT1G125-Q100

Bus buffer/line driver; 3-state

Rev. 1 — 18 June 2013

Product data sheet

1. General description

The 74HC1G125-Q100; 74HCT1G125-Q100 is a single buffer/line driver with 3-state output. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Input levels:
 - ◆ For 74HC1G125-Q100: CMOS level
 - ◆ For 74HCT1G125-Q100: TTL level
- Symmetrical output impedance
- High noise immunity
- Low power consumption
- Balanced propagation delays
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC1G125GW-Q100 74HCT1G125GW-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74HC1G125GV-Q100 74HCT1G125GV-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SC-74A	plastic surface mounted package; 5 leads	SOT753



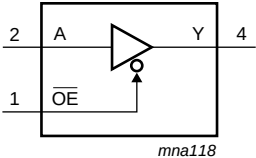
4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74HC1G125GW-Q100	HM
74HCT1G125GW-Q100	TM
74HC1G125GV-Q100	H25
74HCT1G125GV-Q100	T25

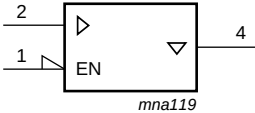
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



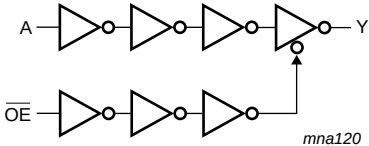
The logic symbol shows a rectangular box with input A on pin 2, output Y on pin 4, and an active-low enable input OE on pin 1. An internal buffer symbol is shown with OE controlling its enable.

Fig 1. Logic symbol



The IEC logic symbol shows a rectangular box with input A on pin 2, output Y on pin 4, and an enable input EN on pin 1. The EN input is shown with a bubble, indicating active-low.

Fig 2. IEC logic symbol



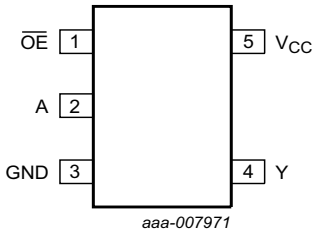
The logic diagram shows the internal structure of the device. It consists of a 3-input NAND gate with inputs A, OE, and a constant high signal. The output of the NAND gate is connected to the output Y. The OE input is shown with a bubble, indicating active-low.

Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

74HC1G125-Q100
74HCT1G125-Q100



The pin configuration diagram shows a rectangular package with pins 1 through 5. Pin 1 is OE, pin 2 is A, pin 3 is GND, pin 4 is Y, and pin 5 is VCC.

Fig 4. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	output enable input (active LOW)
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V _{CC}	5	supply voltage

7. Functional description

7.1 Function table

Table 4. Function table^[1]

Control	Input	Output
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	^[1] -	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	^[1] -	±20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	^[1] -	±35	mA
I _{CC}	supply current		-	70	mA
I _{GND}	ground current		-70	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[2] -	200	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC1G125-Q100			74HCT1G125-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	-	139	-	-	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics 74HC1G125-Q100

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{amb} = -40 °C to +85 °C [1]						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	V
		I _O = -6.0 mA; V _{CC} = 4.5 V	3.84	4.32	-	V
		I _O = -7.8 mA; V _{CC} = 6.0 V	5.34	5.81	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	V
		I _O = 7.8 mA; V _{CC} = 6.0 V	-	0.16	0.33	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	1.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V	-	-	5	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	10	μA
C _I	input capacitance		-	1.5	-	pF

Table 7. Static characteristics **74HC1G125-Q100** ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -6.0 mA; V _{CC} = 4.5 V	3.7	-	-	V
		I _O = -7.8 mA; V _{CC} = 6.0 V	5.2	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 µA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V	-	-	0.4	V
		I _O = 7.8 mA; V _{CC} = 6.0 V	-	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	1.0	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V	-	-	10	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	20	µA

[1] All typical values are measured at T_{amb} = 25 °C.

Table 8. Static characteristics 74HCT1G125-Q100

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C[1]						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V				
		I _O = -20 µA	4.4	4.5	-	V
		I _O = -6.0 mA	3.84	4.32	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V				
		I _O = 20 µA	-	0	0.1	V
		I _O = 6.0 mA	-	0.16	0.33	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	1.0	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	5	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	10	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V	-	-	500	µA
C _I	input capacitance		-	1.5	-	pF
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V				
		I _O = -20 µA	4.4	-	-	V
		I _O = -6.0 mA	3.7	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V				
		I _O = 20 µA	-	-	0.1	V
		I _O = 6.0 mA	-	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	1.0	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	10	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	20	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V	-	-	850	µA

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 9. Dynamic characteristics 74HC1G125-Q100

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 7](#)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40$ °C to $+85$ °C^[1]						
t_{pd}	propagation delay	A to Y; see Figure 5	[2]			
		$V_{CC} = 2.0$ V	-	24	125	ns
		$V_{CC} = 4.5$ V	-	10	25	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	9	-	ns
t_{en}	enable time	$\overline{OE}$ to Y; see Figure 6	[2]			
		$V_{CC} = 2.0$ V	-	19	155	ns
		$V_{CC} = 4.5$ V	-	9	31	ns
		$V_{CC} = 6.0$ V	-	7	26	ns
t_{dis}	disable time	$\overline{OE}$ to Y; see Figure 6	[2]			
		$V_{CC} = 2.0$ V	-	18	155	ns
		$V_{CC} = 4.5$ V	-	12	31	ns
		$V_{CC} = 6.0$ V	-	11	26	ns
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$	[3]	-	30	pF
$T_{amb} = -40$ °C to $+125$ °C						
t_{pd}	propagation delay	A to Y; see Figure 5	[2]			
		$V_{CC} = 2.0$ V	-	-	150	ns
		$V_{CC} = 4.5$ V	-	-	30	ns
		$V_{CC} = 6.0$ V	-	-	26	ns
t_{en}	enable time	$\overline{OE}$ to Y; see Figure 6	[2]			
		$V_{CC} = 2.0$ V	-	-	190	ns
		$V_{CC} = 4.5$ V	-	-	38	ns
		$V_{CC} = 6.0$ V	-	-	32	ns
t_{dis}	disable time	$\overline{OE}$ to Y; see Figure 6	[2]			
		$V_{CC} = 2.0$ V	-	-	190	ns
		$V_{CC} = 4.5$ V	-	-	38	ns
		$V_{CC} = 6.0$ V	-	-	32	ns

[1] All typical values are measured at $T_{amb} = 25$ °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

Table 10. Dynamic characteristics 74HCT1G125-Q100

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 7](#)

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40$ °C to $+85$ °C						
t_{pd}	propagation delay	A to Y; see Figure 5	[2]			
		$V_{CC} = 4.5$ V	-	11	30	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	10	-	ns
t_{en}	enable time	$V_{CC} = 4.5$ V; $\overline{OE}$ to Y; see Figure 6	[2] -	10	35	ns
t_{dis}	disable time	$V_{CC} = 4.5$ V; $\overline{OE}$ to Y; see Figure 6	[2] -	11	31	ns
C_{PD}	power dissipation capacitance	$V_I = GND$ to $V_{CC} - 1.5$ V	[3] -	27	-	pF
$T_{amb} = -40$ °C to $+125$ °C						
t_{pd}	propagation delay	$V_{CC} = 4.5$ V; A to Y; see Figure 5	[2] -	-	36	ns
t_{en}	enable time	$V_{CC} = 4.5$ V; $\overline{OE}$ to Y; see Figure 6	[2] -	-	42	ns
t_{dis}	disable time	$V_{CC} = 4.5$ V; $\overline{OE}$ to Y; see Figure 6	[2] -	-	38	ns

[1] All typical values are measured at $T_{amb} = 25$ °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12. Waveforms

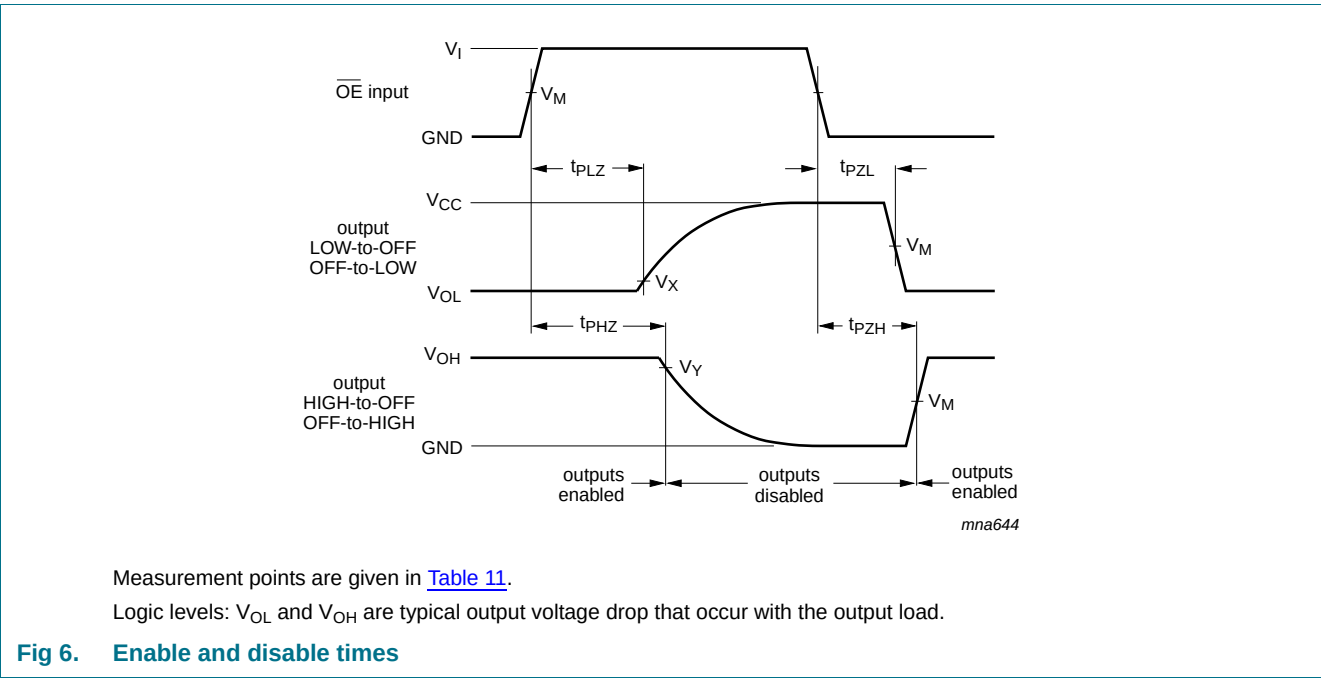
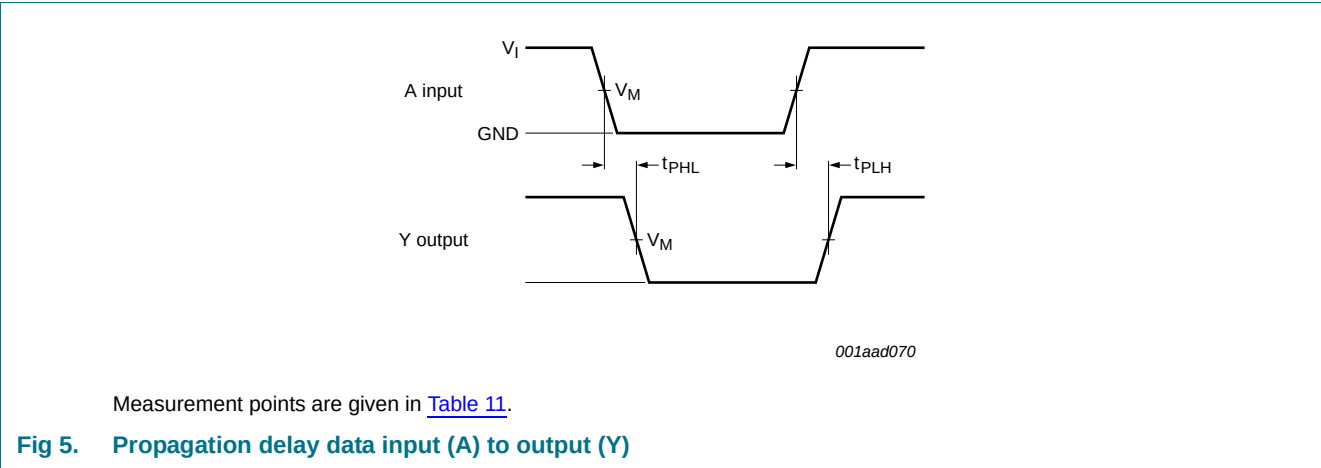


Table 11. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC1G125-Q100	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$
74HCT1G125-Q100	1.3 V	1.3 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

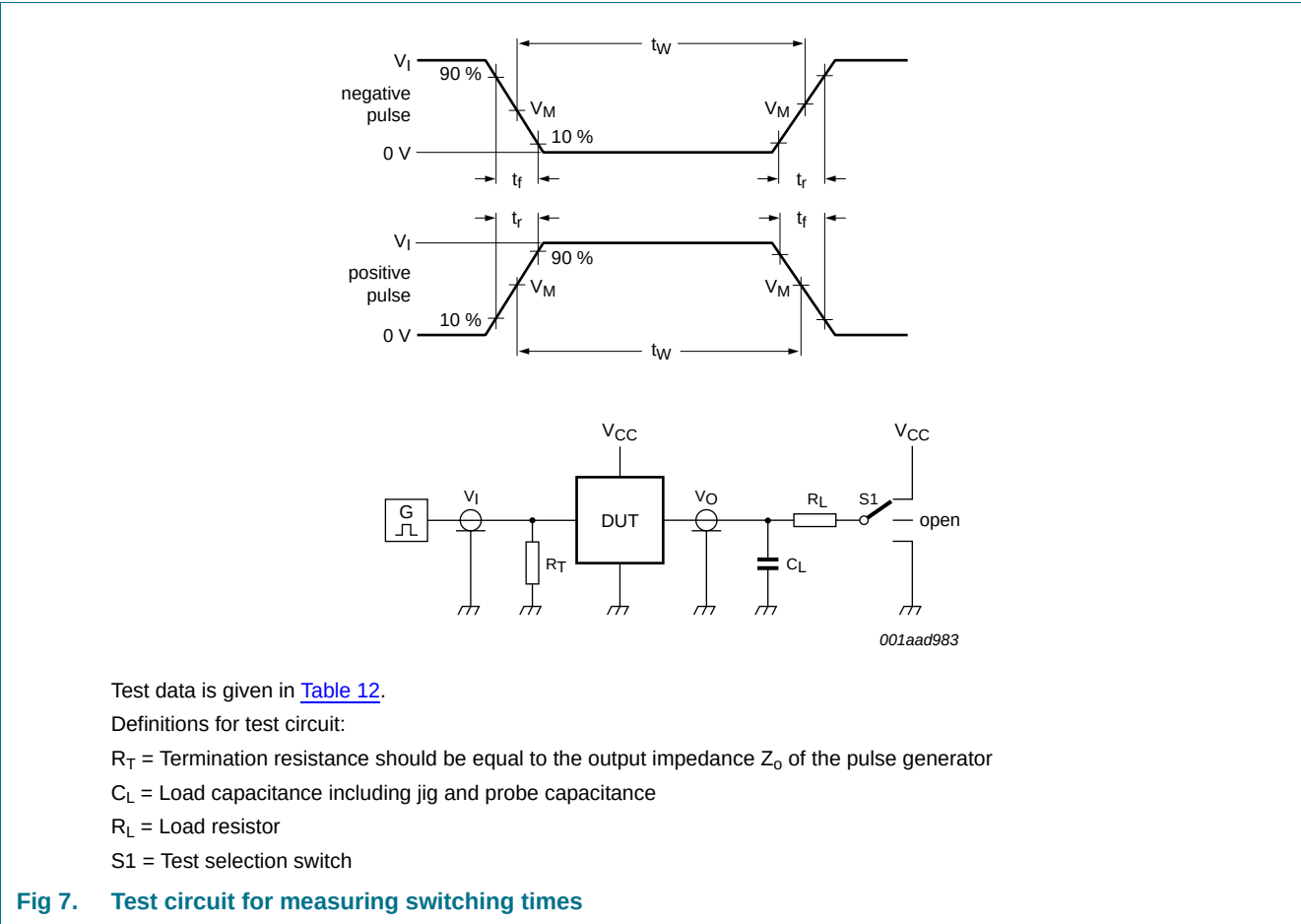


Table 12. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC1G125-Q100	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74HCT1G125-Q100	3 V	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

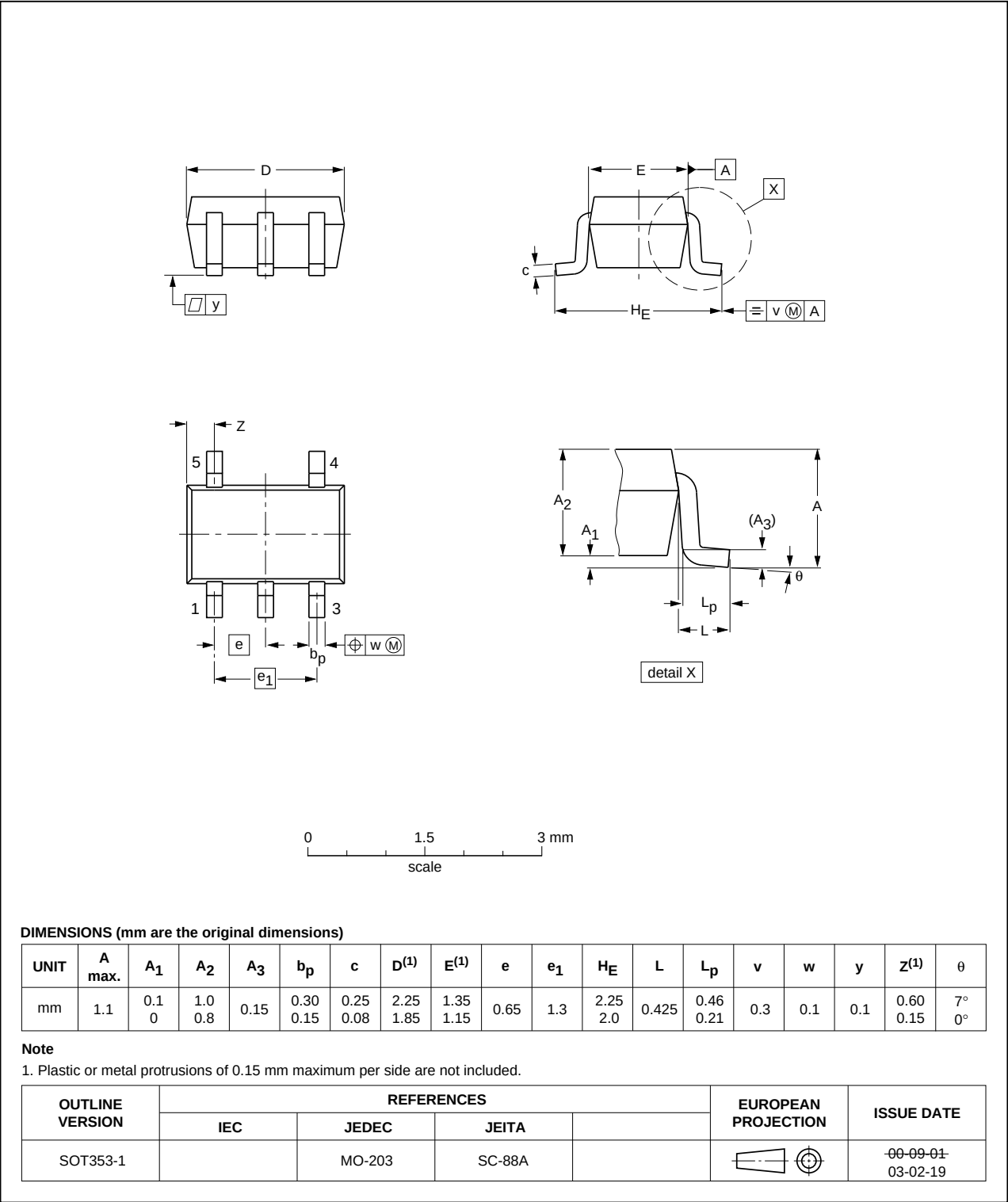


Fig 8. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

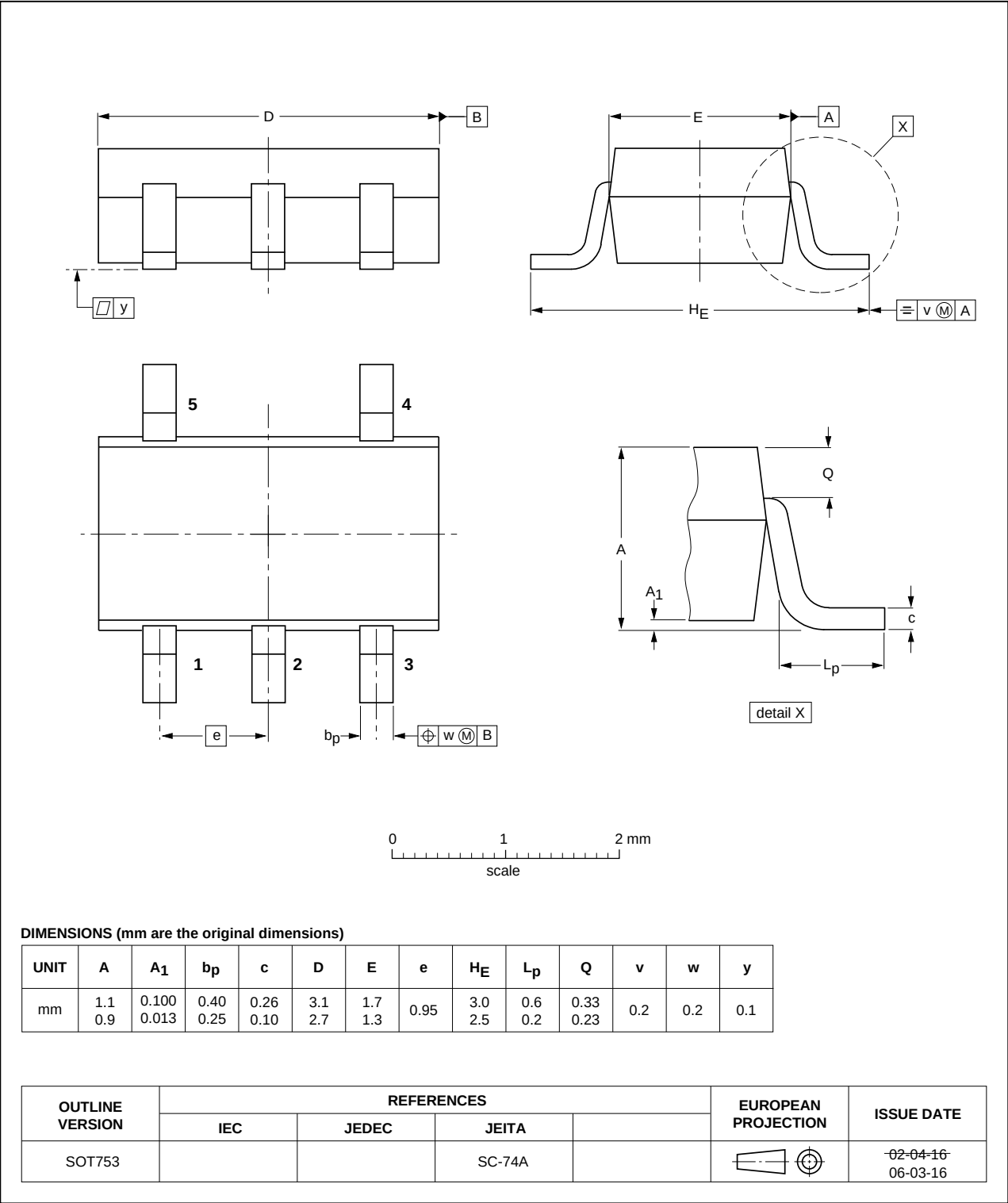


Fig 9. Package outline SOT753 (SC-74A)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic
MM	Machine Model

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT1G125_Q100 v.1	20130618	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

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