

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4016 Quad bilateral switches

Product specification
File under Integrated Circuits, IC06

December 1990

Quad bilateral switches

74HC/HCT4016

FEATURES

- Low “ON” resistance:
160 Ω (typ.) at $V_{CC} = 4.5\text{ V}$
120 Ω (typ.) at $V_{CC} = 6.0\text{ V}$
80 Ω (typ.) at $V_{CC} = 9.0\text{ V}$
- Individual switch controls
- Typical “break before make” built in
- Output capability: non-standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT4016 are high-speed Si-gate CMOS devices and are pin compatible with the “4016” of the

“4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4016 have four independent analog switches (transmission gates).

Each switch has two input/output terminals (Y_n , Z_n) and an active HIGH enable input (E_n). When E_n is connected to V_{CC} , a low bidirectional path between Y_n and Z_n is established (ON condition). When E_n is connected to ground (GND), the switch is disabled and a high impedance between Y_n and Z_n is established (OFF condition).

Current through a switch will not cause additional V_{CC} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $V_{CC} \gg (V_Y, V_Z) \gg \text{GND}$. Inputs Y_n and Z_n are electrically equivalent terminals.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^\circ\text{C}$; $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/t_{PZL}	turn “ON” time E_n to V_{OS}	$C_L = 15\text{ pF}$; $R_L = 1\text{ k}\Omega$; $V_{CC} = 5\text{ V}$	16	17	ns
t_{PHZ}/t_{PLZ}	turn “OFF” time E_n to V_{OS}		14	20	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	12	12	pF
C_S	max. switch capacitance		5	5	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \} \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$ = sum of outputs

C_L = output load capacitance in pF

C_S = max. switch capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

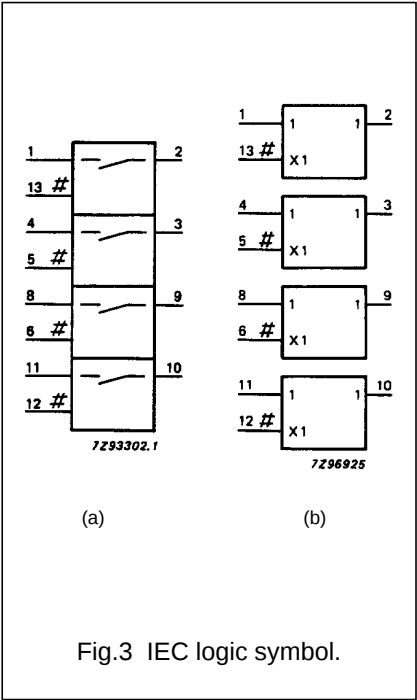
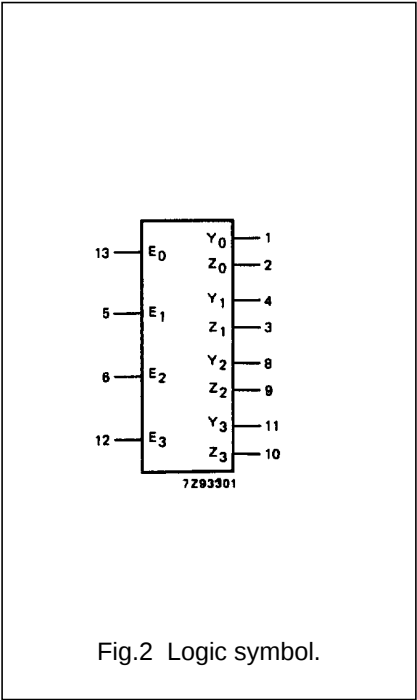
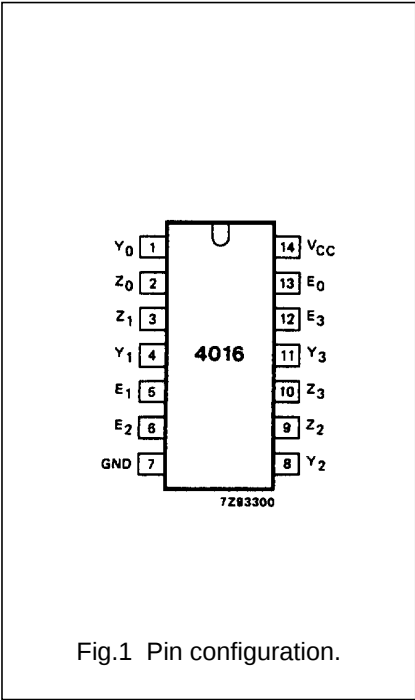
See “74HC/HCT/HCU/HCMOS Logic Package Information”.

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	Y ₀ to Y ₃	independent inputs/outputs
7	GND	ground (0 V)
2, 3, 9, 10	Z ₀ to Z ₃	independent inputs/outputs
13, 5, 6, 12	E ₀ to E ₃	enable inputs (active HIGH)
14	V _{CC}	positive supply voltage



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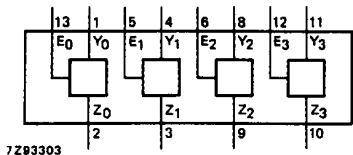


Fig.4 Functional diagram.

APPLICATIONS

- Signal gating
- Modulation
- Demodulation
- Chopper

FUNCTION TABLE

INPUT E_n	CHANNEL IMPEDANCE
L	high
H	low

Notes

1. H = HIGH voltage level
L = LOW voltage level

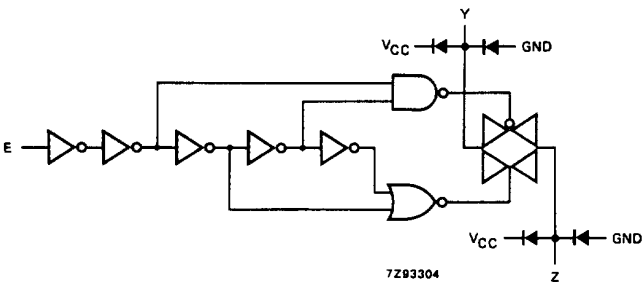


Fig.5 Schematic diagram (one switch).

Quad bilateral switches

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{CC}; \pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	-65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	10.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	GND		V_{CC}	GND		V_{CC}	V	
T_{amb}	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERIS- TICS
T_{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V $V_{CC} = 10.0$ V

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DC CHARACTERISTICS FOR 74HC/HCT

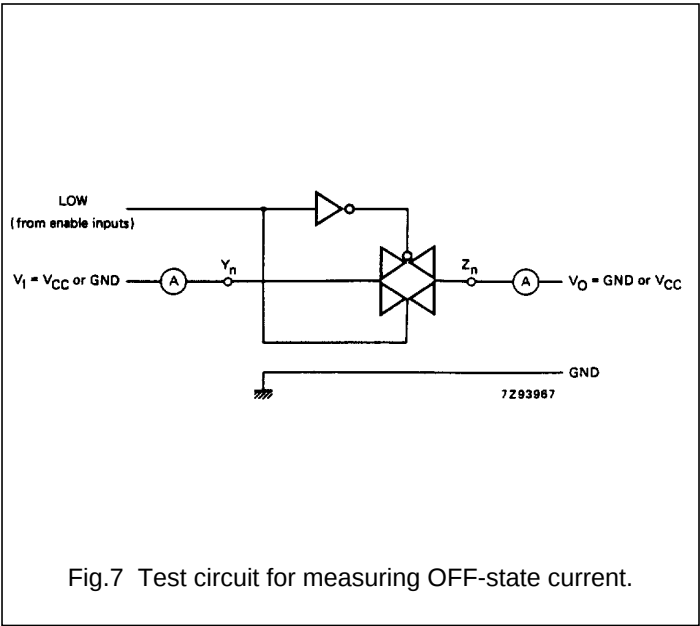
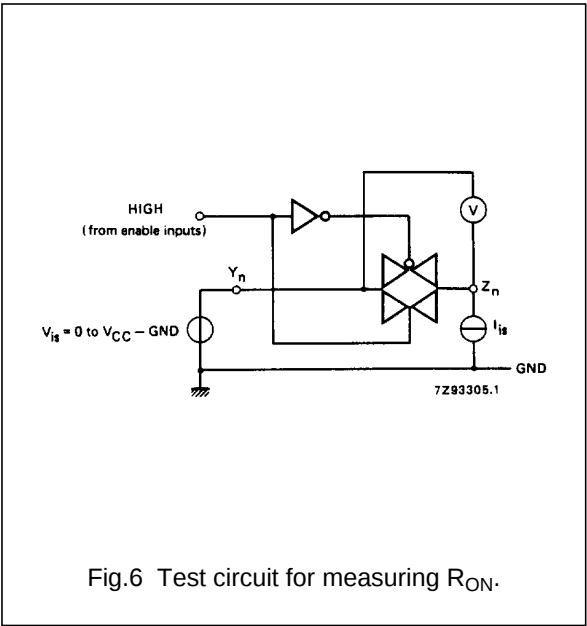
For 74HC: $V_{CC} = 2.0, 4.5, 6.0$ and 9.0 V

For 74HCT: $V_{CC} = 4.5$ V

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC/HCT								V _{CC} (V)	I _S (μA)	V _{is}	V _I
		+25			−40 to +85		−40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
R _{ON}	ON resistance (peak)		−	−		−		−	Ω	2.0	100	V _{CC} to GND	V _{IH} or V _{IL}
			160	320		400		480	Ω	4.5	1000		
			120	240		300		360	Ω	6.0	1000		
			85	170		213		255	Ω	9.0	1000		
R _{ON}	ON resistance (rail)		160	−		−		−	Ω	2.0	100	GND	V _{IH} or V _{IL}
			80	160		200		240	Ω	4.5	1000		
			70	140		175		210	Ω	6.0	1000		
			60	120		150		180	Ω	9.0	1000		
R _{ON}	ON resistance (rail)		170	−		−		−	Ω	2.0	100	V _{CC}	V _{IH} or V _{IL}
			90	180		225		270	Ω	4.5	1000		
			80	160		200		240	Ω	6.0	1000		
			65	135		170		205	Ω	9.0	1000		
ΔR _{ON}	maximum ΔON resistance between any two channels		− 16 12 9						Ω Ω Ω Ω	2.0 4.5 6.0 9.0		V _{CC} to GND	V _{IH} or V _{IL}

Notes to the DC Characteristics

- At supply voltages approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring R_{ON} see Fig.6.



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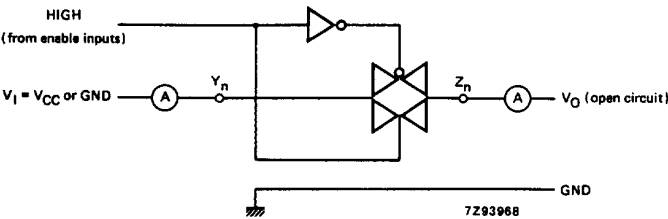


Fig.8 Test circuit for measuring ON-state current.

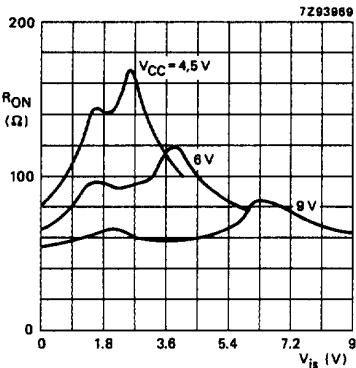


Fig.9 Typical R_{ON} as a function of input voltage V_{is} for $V_{is} = 0$ to V_{CC} .

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DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS		
		74HC									V _{CC} (V)	V _I	OTHER
		+25			−40 to +85		−40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V _{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.3		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0			
V _{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70	V	2.0 4.5 6.0 9.0			
±I _I	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	V _{CC} or GND		
±I _S	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	V _{IH} or V _{IL}	V _S = V _{CC} – GND (see Fig.7)	
±I _S	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	V _{IH} or V _{IL}	V _S = V _{CC} – GND (see Fig.8)	
I _{CC}	quiescent supply current			2.0 4.0		20.0 40.0		40.0 80.0	μA	6.0 10.0	V _{CC} or GND	V _{IS} = GND or V _{CC} ; V _{OS} = V _{CC} or GND	

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay V _{is} to V _{os}		17 6 5 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 9.0	R _L = ∞; C _L = 50 pF (see Fig.16)
t _{PZH} / t _{PZL}	turn “ON” time E _n to V _{os}		52 19 15 11	190 38 32 28		240 48 41 35		235 57 48 42	ns	2.0 4.5 6.0 9.0	R _L = 1 kΩ; C _L = 50 pF (see Figs 17 and 18)
t _{PHZ} / t _{PLZ}	turn “OFF” time E _n to V _{os}		47 17 14 13	145 29 25 22		180 36 31 28		220 44 38 33	ns	2.0 4.5 6.0 9.0	R _L = 1 kΩ; C _L = 50 pF (see Figs 17 and 18)

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DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V _{CC} (V)	V _I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V _{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V _{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
±I _I	input leakage current			0.1		1.0		1.0	μA	5.5	V _{CC} or GND	
±I _S	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	5.5	V _{IH} or V _{IL}	V _S = V _{CC} – GND (see Fig.7)
±I _S	analog switch ON-state current			0.1		1.0		1.0	μA	5.5	V _{IH} or V _{IL}	V _S = V _{CC} – GND (see Fig.8)
I _{CC}	quiescent supply current			2.0		20.0		40.0	μA	4.5 to 5.5	V _{CC} or GND	V _{IS} = GND or V _{CC} ; V _{OS} = V _{CC} or GND
ΔI _{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V _{CC} –2.1V	other inputs at V _{CC} or GND

Note

- The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
E _N	1.00

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AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay V _{is} to V _{os}		6	12		15		18	ns	4.5	R _L = ∞; C _L = 50 pF (see Fig.16)
t _{PZH}	turn “ON” time E _n to V _{os}		19	35		44		53	ns	4.5	R _L = 1 kΩ; C _L = 50 pF (see Figs 17 and 18)
t _{PZL}	turn “ON” time E _n to V _{os}		20	35		44		53	ns	4.5	R _L = 1 kΩ; C _L = 50 pF (see Figs 17 and 18)
t _{PHZ} / t _{PLZ}	turn “OFF” time E _n to V _{os}		23	35		44		53	ns	4.5	R _L = 1 kΩ; C _L = 50 pF (see Figs 17 and 18)

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; $t_r = t_f = 6$ ns

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} (V)	$V_{is(p-p)}$ (V)	CONDITIONS
	sine-wave distortion $f = 1$ kHz	0.80 0.40	% %	4.5 9.0	4.0 8.0	$R_L = 10$ k Ω ; $C_L = 50$ pF (see Fig.14)
	sine-wave distortion $f = 10$ kHz	2.40 1.20	% %	4.5 9.0	4.0 8.0	$R_L = 10$ k Ω ; $C_L = 50$ pF (see Fig.14)
	switch “OFF” signal feed-through	−50 −50	dB dB	4.5 9.0	note 3	$R_L = 600$ Ω ; $C_L = 50$ pF; $f = 1$ MHz (see Figs 10 and 15)
	crosstalk between any two switches	−60 −60	dB dB	4.5 9.0	note 3	$R_L = 600$ Ω ; $C_L = 50$ pF; $f = 1$ MHz (see Fig.12)
$V_{(p-p)}$	crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 220	mV mV	4.5 9.0		$R_L = 600$ Ω ; $C_L = 50$ pF; $f = 1$ MHz (E_n , square wave between V_{CC} and GND, $t_r = t_f = 6$ ns) (see Fig.13)
f_{max}	minimum frequency response (−3dB)	150 160	MHz MHz	4.5 9.0	note 4	$R_L = 50$ Ω ; $C_L = 10$ pF (see Figs 11 and 14)
C_S	maximum switch capacitance	5	pF			

Notes

- V_{is} is the input voltage at a Y_n or Z_n terminal, whichever is assigned as an input.
- V_{os} is the output voltage at a Y_n or Z_n terminal, whichever is assigned as an output.
- Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
- Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

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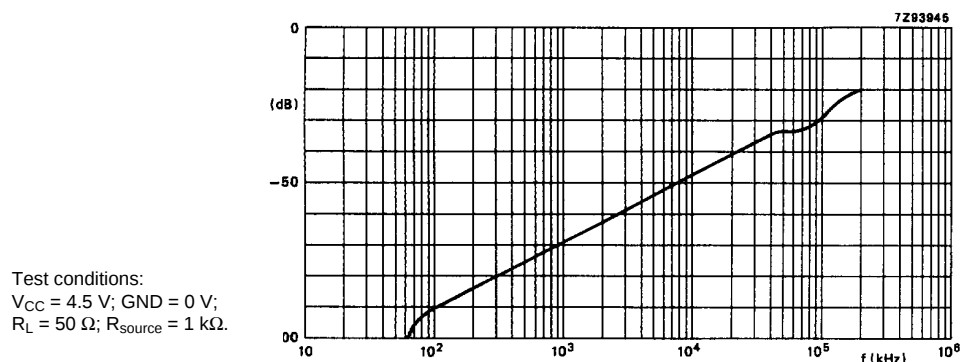


Fig.10 Typical switch "OFF" signal feed-through as a function of frequency.

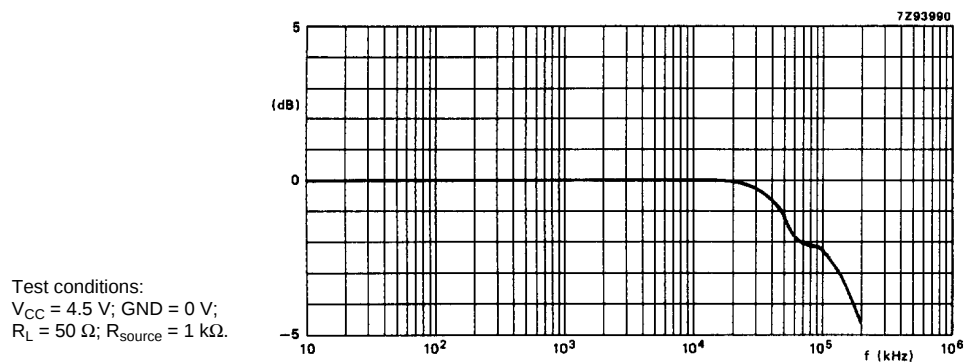


Fig.11 Typical frequency response.

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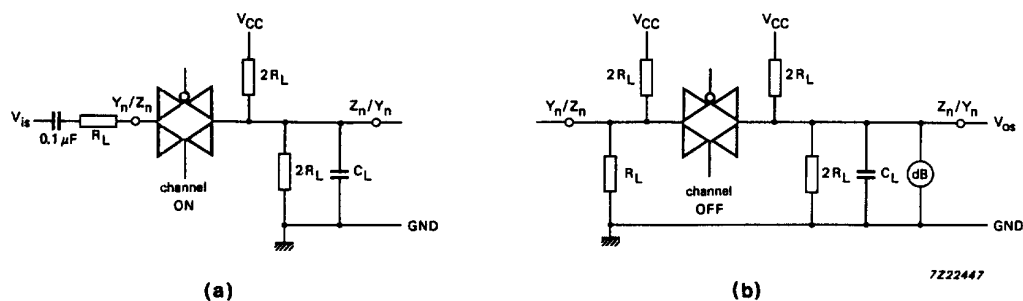


Fig.12 Test circuit for measuring crosstalk between any two switches.
(a) channel ON condition; (b) channel OFF condition.

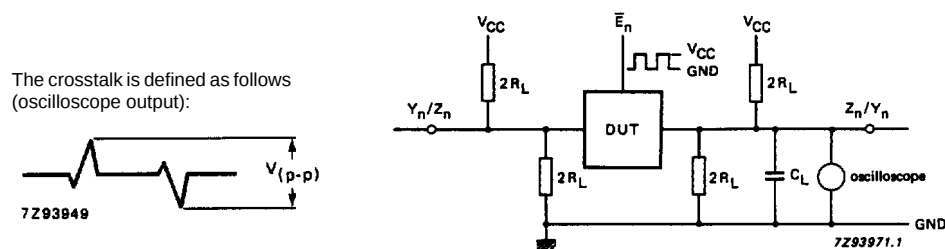


Fig.13 Test circuit for measuring crosstalk between control and any switch.

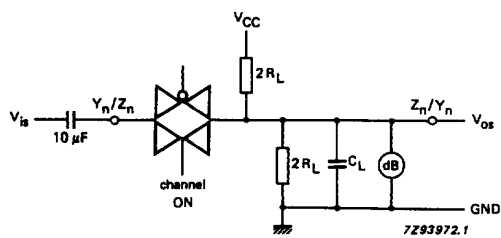


Fig.14 Test circuit for measuring sine-wave distortion and minimum frequency response.

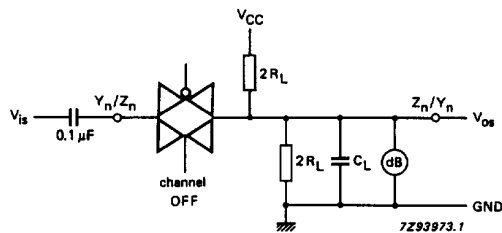


Fig.15 Test circuit for measuring switch "OFF" signal feed-through.

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AC WAVEFORMS

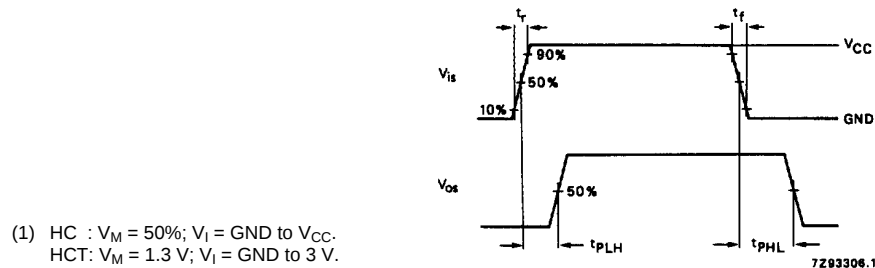
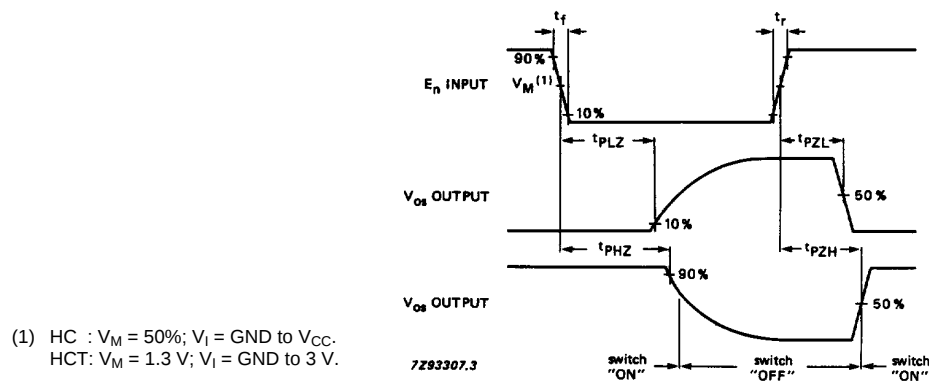
Fig.16 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

Fig.17 Waveforms showing the turn-ON and turn-OFF times.

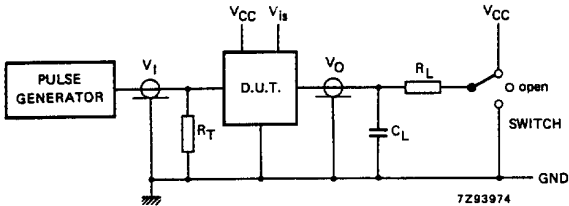
Quad bilateral switches

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TEST CIRCUIT AND WAVEFORMS

Conditions

TEST	SWITCH	V _{is}
t _{PZH}	GND	V _{CC}
t _{PZL}	V _{CC}	GND
t _{PHZ}	GND	V _{CC}
t _{PLZ}	V _{CC}	GND
others	open	pulse

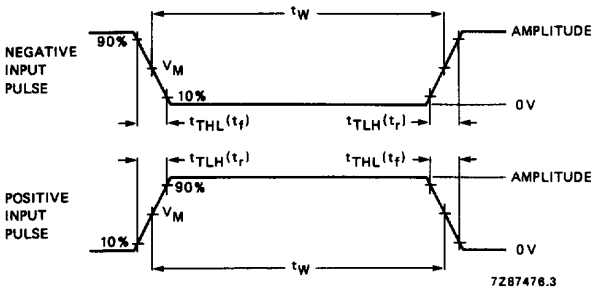


C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.
t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint t_r, t_f with 50% duty factor.

FAMILY	AMPLITUDE	V _M	t _r ; t _f	
			f _{max} ; PULSE WIDTH	OTHER
74HC	V _{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Fig.18 Test circuit for measuring AC performance.

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.
t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint t_r, t_f with 50% duty factor.



FAMILY	AMPLITUDE	V _M	t _r ; t _f	
			f _{max} ; PULSE WIDTH	OTHER
74HC	V _{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Fig.19 Input pulse definitions.

PACKAGE OUTLINES

See *“74HC/HCT/HCU/HCMOS Logic Package Outlines”*.

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