

# 74HC574; 74HCT574

Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 5 — 25 April 2012

Product data sheet

## 1. General description

The 74HC574; 74HCT574 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL. It is specified in compliance with JEDEC standard no. 7A.

The 74HC574; 74HCT574 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A clock (CP) and an output enable (OE) input are common to all flip-flops. The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When  $\overline{OE}$  is LOW the contents of the 8 flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

The 74HC574; 74HCT574 is functionally identical to:

- 74HC564: but has non-inverting outputs
- 74HC374; 74HCT374: but has a different pin arrangement

## 2. Features and benefits

- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

## 3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74HC574N	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	DIP20	plastic dual in-line package; 20 leads (300 mil)		SOT146-1
74HCT574N					
74HC574D	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	SO20	plastic small outline package; 20 leads; body width 7.5 mm		SOT163-1
74HCT574D					



Table 1. Ordering information ...continued

Type number	Package	Temperature range	Name	Description	Version
74HC574DB		−40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HCT574DB					
74HC574PW		−40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT574PW					

## 4. Functional diagram

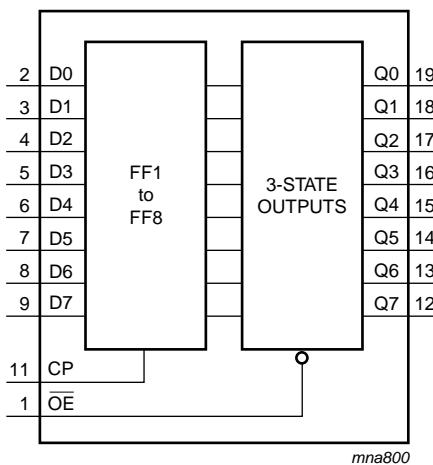


Fig 1. Functional diagram

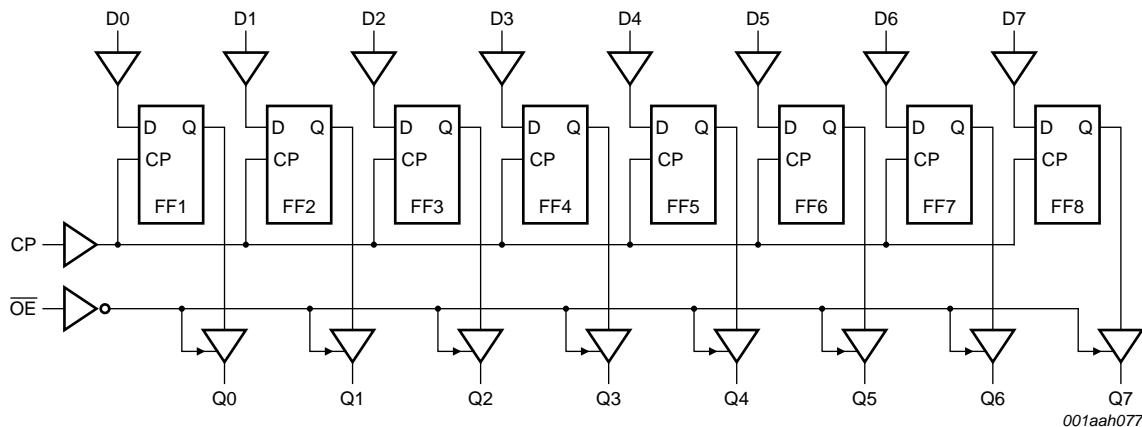


Fig 2. Logic diagram

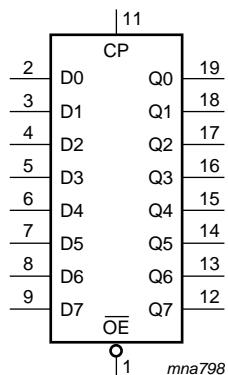


Fig 3. Logic symbol

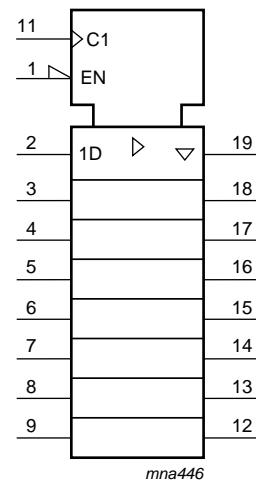


Fig 4. IEC logic symbol

## 5. Pinning information

### 5.1 Pinning

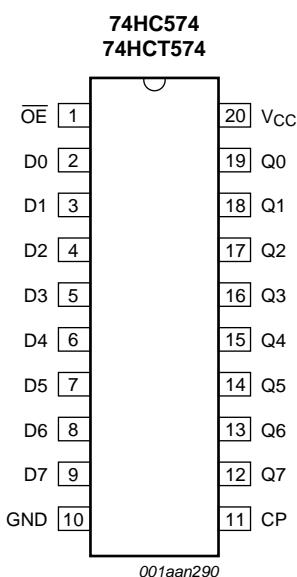


Fig 5. Pin configuration DIP20 and SO20

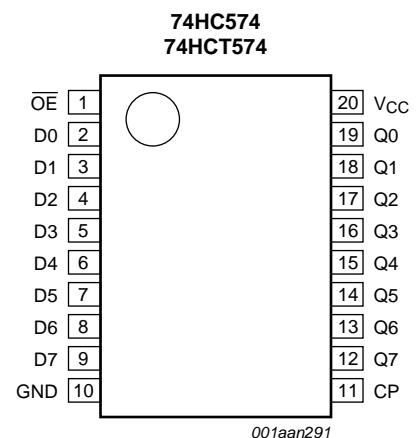


Fig 6. Pin configuration SSOP20 and TSSOP20

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
D[0:7]	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge triggered)
Q[0:7]	19, 18, 17, 16, 15, 14, 13, 12	3-state flip-flop output
$V_{CC}$	20	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating mode	Input			Internal flip-flop	Output
	OE	CP	Dn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable output	H	↑	l	L	Z
	H	↑	h	H	Z

[1] H = HIGH voltage level;  
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW CP transition;  
 L = LOW voltage level;  
 l = LOW voltage level one setup time prior to the HIGH-to-LOW CP transition;  
 Z = high-impedance OFF-state;  
 ↑ = LOW-to-HIGH clock transition.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	$\pm 20$	mA
$I_O$	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5)$ V	-	$\pm 35$	mA
$I_{CC}$	supply current		-	$+70$	mA
$I_{GND}$	ground current		-	-70	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	DIP20 package	[1]	-	750
		SO20, SSOP20 and TSSOP20 packages		[2]	500
					mW

[1] For DIP20 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.  
 [2] For SO20:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.  
 For SSOP20 and TSSOP20 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC574			74HCT574			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC574</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = −20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = −20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = −20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = −6.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = −7.8 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 7.8 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>oz</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.5	-	±5.0	-	±10.0	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	µA
C <sub>I</sub>	input capacitance		-	3.5	-					pF
<b>74HCT574</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = −20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = −6 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 6.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = V <sub>CC</sub> or GND per input pin; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	-	±0.5	-	±5.0	-	±10	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = V <sub>CC</sub> − 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 0 A								
		per input pin; D <sub>n</sub> inputs	-	50	180	-	225	-	245	µA
		per input pin; $\overline{OE}$ input	-	125	450	-	563	-	613	µA
		per input pin; CP input	-	150	540	-	675	-	735	µA
C <sub>I</sub>	input capacitance		-	3.5	-					pF

## 10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>For type 74HC574</b>										
$t_{pd}$	propagation delay	CP to Qn; see <a href="#">Figure 7</a>	[1]							
		$V_{CC} = 2.0 \text{ V}$	-	47	150	-	190	-	225	ns
		$V_{CC} = 4.5 \text{ V}$	-	17	30	-	35	-	45	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	14	-	-	-	-	-	ns
$t_{en}$	enable time	$\overline{OE}$ to Qn; see <a href="#">Figure 9</a>	[2]							
		$V_{CC} = 2.0 \text{ V}$	-	44	140	-	175	-	210	ns
		$V_{CC} = 4.5 \text{ V}$	-	16	28	-	35	-	42	ns
		$V_{CC} = 6.0 \text{ V}$	-	13	24	-	30	-	36	ns
$t_{dis}$	disable time	$\overline{OE}$ to Qn; see <a href="#">Figure 9</a>	[3]							
		$V_{CC} = 2.0 \text{ V}$	-	39	125	-	155	-	190	ns
		$V_{CC} = 4.5 \text{ V}$	-	14	25	-	31	-	38	ns
		$V_{CC} = 6.0 \text{ V}$	-	11	21	-	26	-	32	ns
$t_t$	transition time	Qn; see <a href="#">Figure 7</a>	[4]							
		$V_{CC} = 2.0 \text{ V}$	-	14	60	-	75	-	90	ns
		$V_{CC} = 4.5 \text{ V}$	-	5	12	-	15	-	18	ns
		$V_{CC} = 6.0 \text{ V}$	-	4	10	-	13	-	15	ns
$t_w$	pulse width	CP HIGH or LOW; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0 \text{ V}$	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$	14	4	-	17	-	20	-	ns
$t_{su}$	set-up time	Dn to CP; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0 \text{ V}$	60	6	-	75	-	90	-	ns
		$V_{CC} = 4.5 \text{ V}$	12	2	-	15	-	18	-	ns
		$V_{CC} = 6.0 \text{ V}$	10	2	-	13	-	15	-	ns
$t_h$	hold time	Dn to CP; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0 \text{ V}$	5	0	-	5	-	5	-	ns
		$V_{CC} = 4.5 \text{ V}$	5	0	-	5	-	5	-	ns
		$V_{CC} = 6.0 \text{ V}$	5	0	-	5	-	5	-	ns
$f_{max}$	maximum frequency	CP; see <a href="#">Figure 7</a>								
		$V_{CC} = 2.0 \text{ V}$	6.0	37	-	4.8	-	4.0	-	MHz
		$V_{CC} = 4.5 \text{ V}$	30	112	-	24	-	20	-	MHz
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	123	-	-	-	-	-	MHz
$V_{CC} = 6.0 \text{ V}$			35	133	-	28	-	24	-	MHz

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$C_{PD}$	power dissipation capacitance	$C_L = 50 \text{ pF}; f = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$	[5]	-	22	-	-	-	-	pF
<b>For type 74HCT574</b>										
$t_{pd}$	propagation delay	CP to Qn; see <a href="#">Figure 7</a>	[1]							
		$V_{CC} = 4.5 \text{ V}$	-	18	33	-	41	-	50	ns
$t_{en}$	enable time	$\overline{OE}$ to Qn; see <a href="#">Figure 9</a>	[2]							
		$V_{CC} = 4.5 \text{ V}$	-	19	33	-	41	-	50	ns
$t_{dis}$	disable time	$\overline{OE}$ to Qn; see <a href="#">Figure 9</a>	[3]							
		$V_{CC} = 4.5 \text{ V}$	-	16	28	-	35	-	42	ns
$t_t$	transition time	Qn; see <a href="#">Figure 7</a>	[4]							
		$V_{CC} = 4.5 \text{ V}$	-	5	12	-	15	-	18	ns
$t_w$	pulse width	CP HIGH or LOW; see <a href="#">Figure 8</a>								
		$V_{CC} = 4.5 \text{ V}$	16	7	-	20	-	24	-	ns
$t_{su}$	set-up time	Dn to CP; see <a href="#">Figure 8</a>								
		$V_{CC} = 4.5 \text{ V}$	12	3	-	15	-	18	-	ns
$t_h$	hold time	Dn to CP; see <a href="#">Figure 8</a>								
		$V_{CC} = 4.5 \text{ V}$	5	-1	-	5	-	5	-	ns
$f_{max}$	maximum frequency	CP; see <a href="#">Figure 7</a>								
		$V_{CC} = 4.5 \text{ V}$	30	69	-	24	-	20	-	MHz
$C_{PD}$	power dissipation capacitance	$C_L = 50 \text{ pF}; f = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$	[5]	-	25	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .[2]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .[3]  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .[4]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .[5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

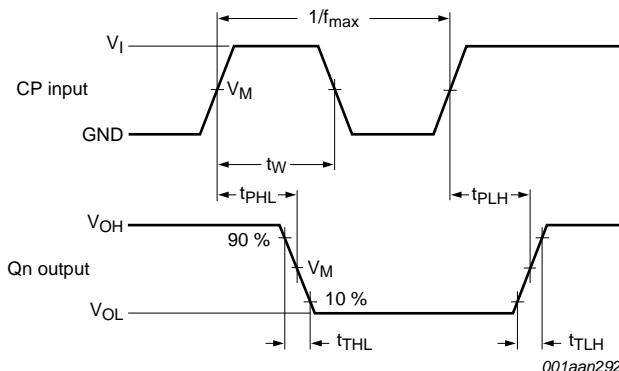
$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 $f_i$  = input frequency in MHz; $f_o$  = output frequency in MHz; $C_L$  = output load capacitance in pF; $V_{CC}$  = supply voltage in V;

N = number of inputs switching;

 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

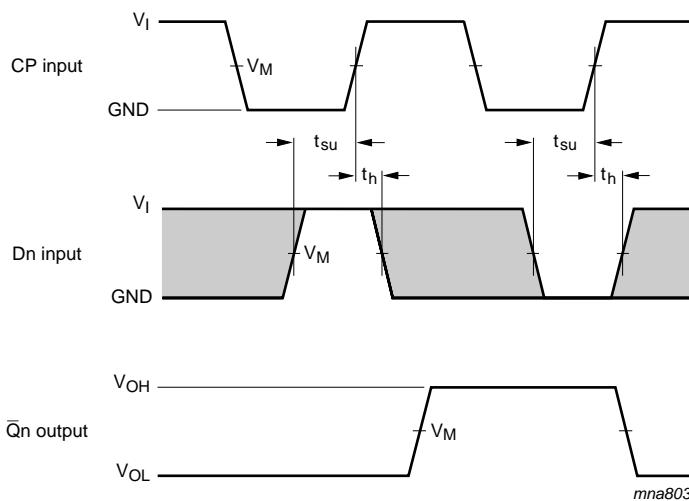
## 11. Waveforms



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Propagation delay input (CP) to output (Qn), output transition time, clock input (CP) pulse width and the maximum frequency (CP)**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 8. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times**

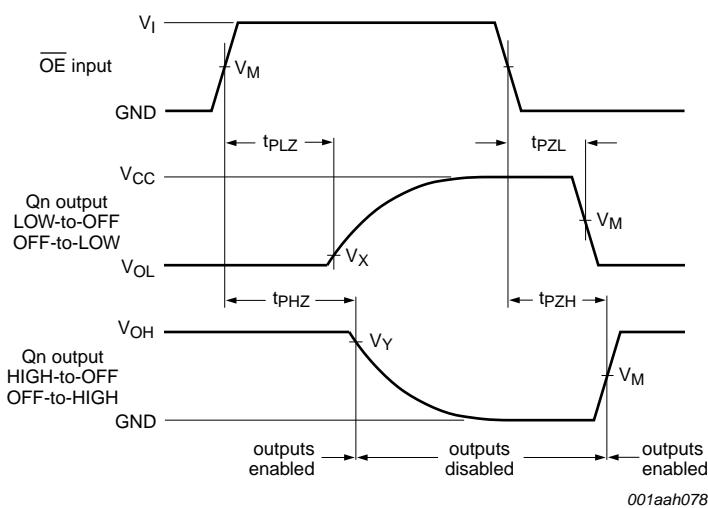
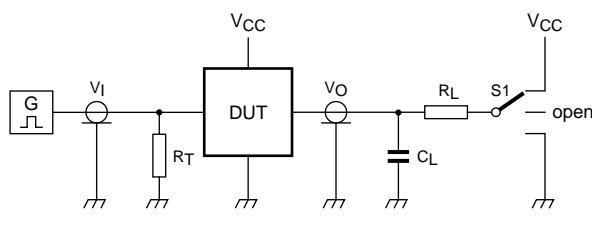
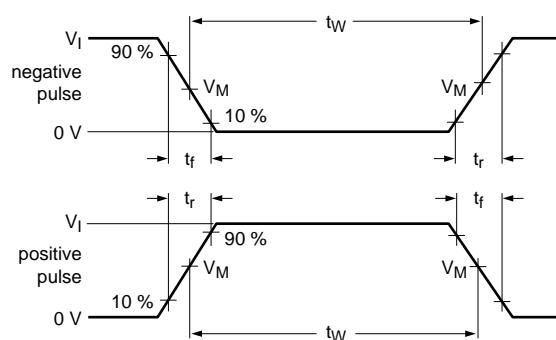


Fig 9. Enable and disable times

Table 8. Measurement points

Type	Input	Output		
		$V_M$	$V_M$	$V_x$
74HC574	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT574	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



001aad983

Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

S1 = Test selection switch.

**Fig 10. Test circuit for measuring switching times**

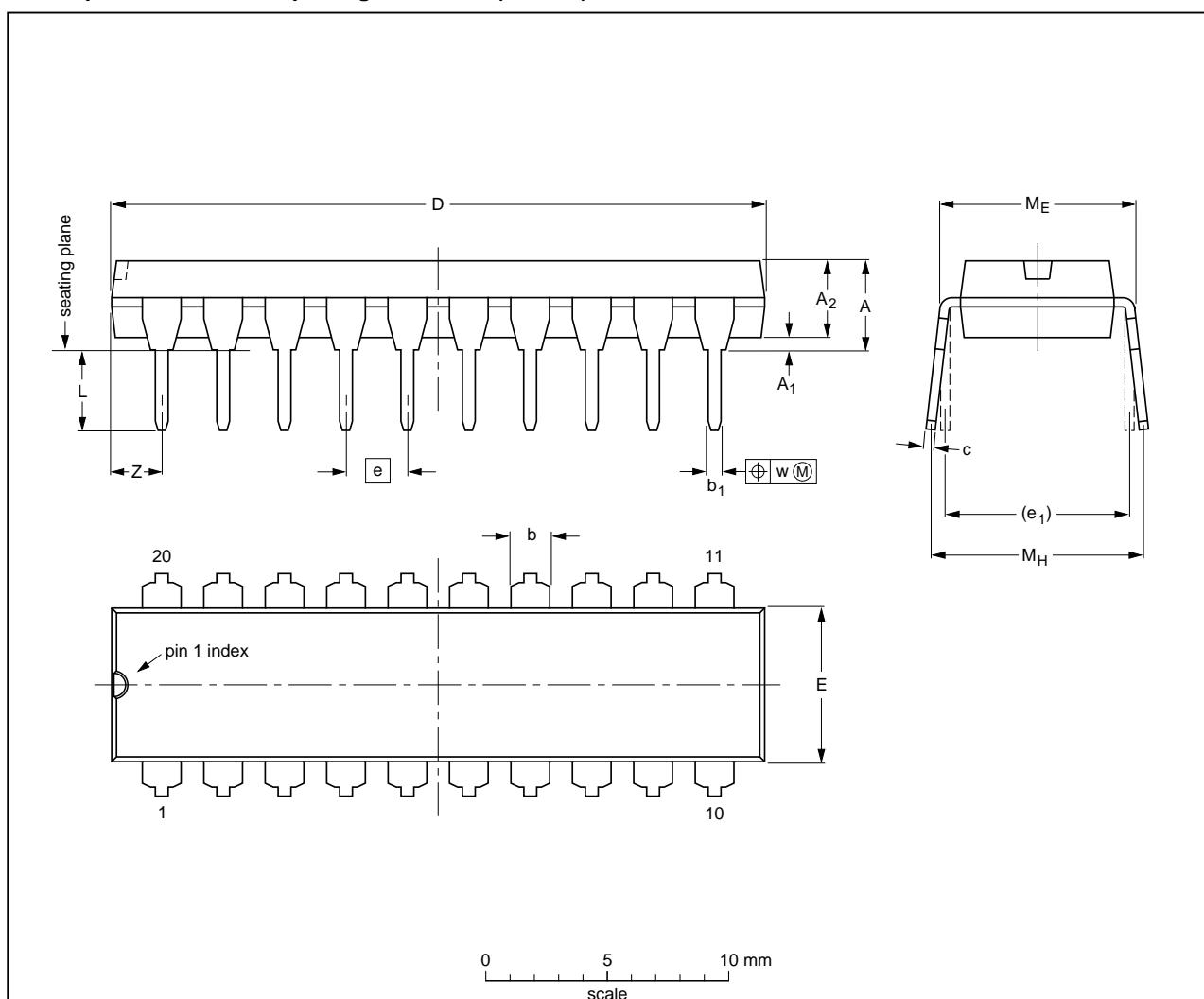
**Table 9. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC574	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT574	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

## 12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



## DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

## Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			99-12-27 03-02-13

Fig 11. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

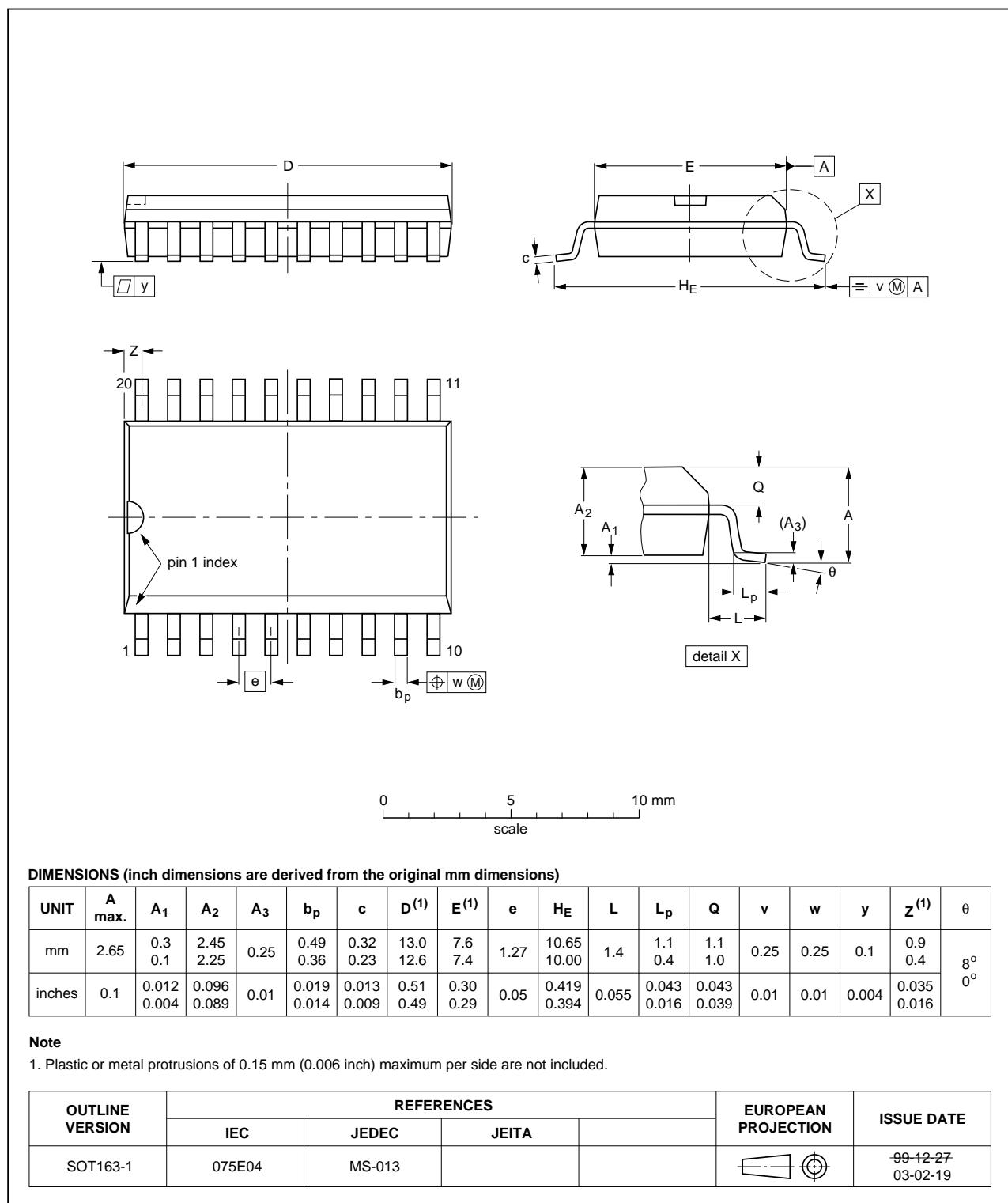


Fig 12. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

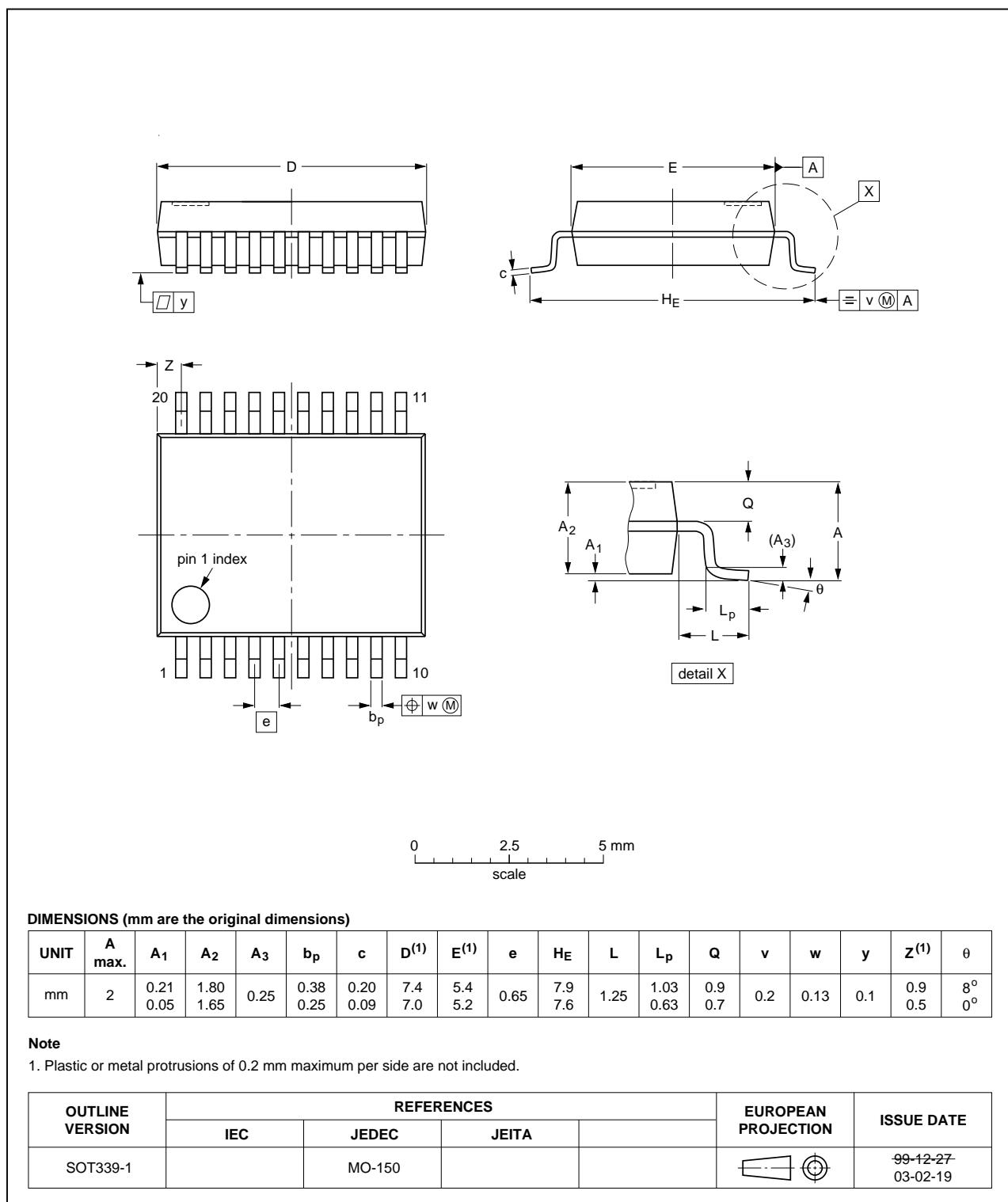


Fig 13. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

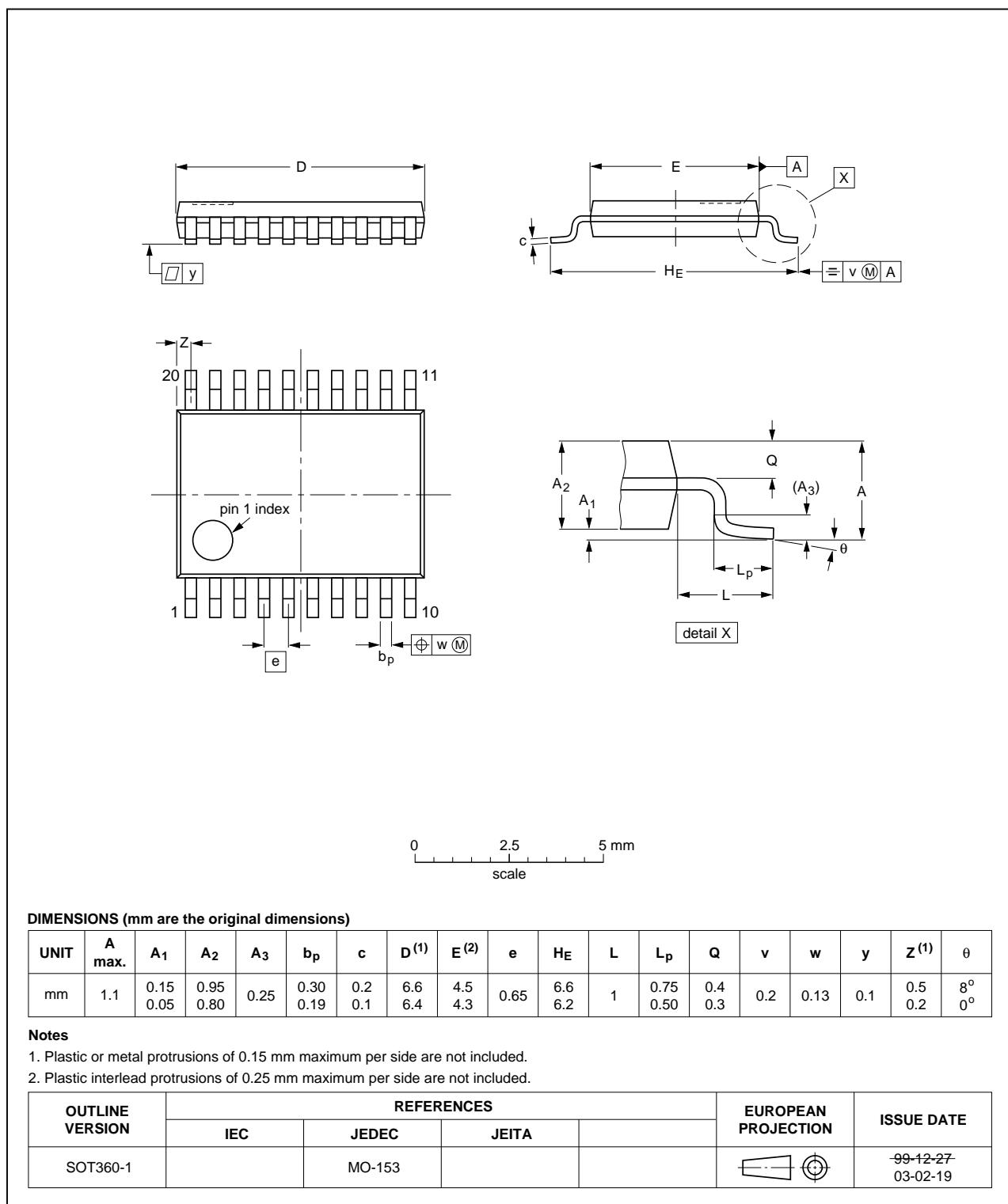


Fig 14. Package outline SOT360-1 (TSSOP20)

## 13. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT574 v.5	20120425	Product data sheet	-	74HC_HCT574 v.4
Modifications:		• $V_X$ and $V_Y$ measurement points added to Table 8.		
74HC_HCT574 v.4	20111219	Product data sheet	-	74HC_HCT574 v.3
Modifications:		• Legal pages updated.		
74HC_HCT574 v.3	20101215	Product data sheet	-	74HC_HCT574_CNV v.2
74HC_HCT574_CNV v.2	19970827	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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