

December 2013

74LCX32 Low Voltage Quad 2-Input OR Gate with 5V Tolerant Inputs

Features

- 5V tolerant inputs
- 2.3V-3.6V V_{CC} specifications provided
- 5.5ns t_{PD} max. $(V_{CC} = 3.3V)$, $10\mu A I_{CC}$ max.
- Power down high impedance inputs and outputs
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- Implements proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds JEDEC 78 conditions
- ESD performance:
 - Human body model > 2000V
 - Machine model > 150V
- Leadless DQFN package

General Description

The LCX32 contains four 2-input OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX32 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Ordering Information

| Order Number | Package Number | Package Description |
|--------------------------|-------------------|---|
| 74LCX32M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74LCX32SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74LC32BQX ⁽¹⁾ | MLP14A | 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm |
| 74LCX32MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Note:

1. DQFN package available in Tape and Reel only.

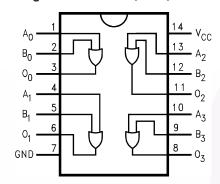
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



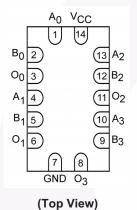
All packages are lead free per JEDEC: J-STD-020B standard.

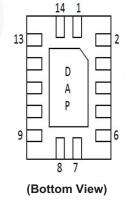
Connection Diagrams

Pin Assignments for SOIC, SOP, and TSSOP



Pad Assignments for DQFN





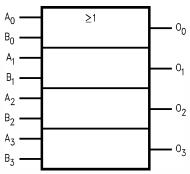
Pin Description

| Pin Names | Description |
|---------------------------------|-------------|
| A _n , B _n | Inputs |
| O _n | Outputs |
| DAP | No Connect |

Note: DAP (Die Attach Pad)

Logic Symbol

IEEE/IEC



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|------------------|---|---------------------------------|
| V _{CC} | Supply Voltage | -0.5V to +7.0V |
| V _I | DC Input Voltage | -0.5V to +7.0V |
| Vo | DC Output Voltage, Output in HIGH or LOW State ⁽²⁾ | -0.5V to V _{CC} + 0.5V |
| I _{IK} | DC Input Diode Current, V _I < GND | –50mA |
| I _{OK} | DC Output Diode Current | |
| | V _O < GND | –50mA |
| | V _O > V _{CC} | +50mA |
| Io | DC Output Source/Sink Current | ±50mA |
| I _{CC} | DC Supply Current per Supply Pin | ±100mA |
| I _{GND} | DC Ground Current per Ground Pin | ±100mA |
| T _{STG} | Storage Temperature | −65°C to +150°C |

Note:

2. IO Absolute Maximum Rating must be observed.

Recommended Operating Conditions⁽³⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Units |
|-----------------------------------|--|------|-----------------|-------|
| V _{CC} | Supply Voltage | | | |
| | Operating | 2.0 | 3.6 | V |
| | Data Retention | 1.5 | 3.6 | |
| V _I | Input Voltage | 0 | 5.5 | V |
| Vo | Output Voltage, HIGH or LOW State | 0 | V _{CC} | V |
| I _{OH} / I _{OL} | Output Current | | | |
| | $V_{CC} = 3.0V - 3.6V$ | | ±24 | mA |
| | $V_{CC} = 2.7V - 3.0V$ | | ±12 | |
| | $V_{CC} = 2.3V - 2.7V$ | | ±8 | |
| T _A | Free-Air Operating Temperature | -40 | 85 | °C |
| Δt / ΔV | Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V | 0 | 10 | ns/V |

Note:

3. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| | | | | T _A = -40°C | to +85°C | |
|------------------|---------------------------------------|---------------------|--------------------------|------------------------|----------|-------|
| Symbol | Parameter | V _{CC} (V) | Conditions | Min. | Max. | Units |
| V _{IH} | HIGH Level Input Voltage | 2.3–2.7 | | 1.7 | | V |
| | | 2.7–3.6 | | 2.0 | | |
| V _{IL} | LOW Level Input Voltage | 2.3–2.7 | | | 0.7 | V |
| | | 2.7–3.6 | | | 0.8 | |
| V _{OH} | HIGH Level Output Voltage | 2.3–3.6 | $I_{OH} = -100 \mu A$ | V _{CC} - 0.2 | | V |
| | | 2.3 | $I_{OH} = -8mA$ | 1.8 | | |
| | | 2.7 | $I_{OH} = -12mA$ | 2.2 | | |
| | | 3.0 | $I_{OH} = -18mA$ | 2.4 | | |
| | | | $I_{OH} = -24mA$ | 2.2 | | |
| V _{OL} | LOW Level Output Voltage | 2.3–3.6 | $I_{OL} = 100 \mu A$ | | 0.2 | V |
| | | 2.3 | $I_{OL} = 8mA$ | | 0.6 | |
| | | 2.7 | I _{OL} = 12mA | | 0.4 | |
| | | 3.0 | I _{OL} = 16mA | | 0.4 | |
| | | | I _{OL} = 24mA | | 0.55 | |
| I _I | Input Leakage Current | 2.3–3.6 | $0 \le V_I \le 5.5V$ | | ±5.0 | μA |
| I _{OFF} | Power-Off Leakage Current | 0 | V_I or $V_O = 5.5V$ | | 10 | μA |
| I _{CC} | Quiescent Supply Current | 2.3–3.6 | $V_I = V_{CC}$ or GND | | 10 | μA |
| | | | $3.6V \le V_I \le 5.5V$ | | ±10 | |
| ΔI_{CC} | Increase in I _{CC} per Input | 2.3–3.6 | $V_{IH} = V_{CC} - 0.6V$ | | 500 | μA |

AC Electrical Characteristics

| | | $T_A = -40$ °C to +85°C, $R_L = 500\Omega$ | | | | | | |
|-------------------------------------|--------------------------------------|--|------|--|------|---|------|-------|
| | | $V_{CC} = 3.3V \pm 0.3V,$ $C_{L} = 50pF$ | | $egin{aligned} \mathbf{V_{CC}} &= \mathbf{2.7V,} \\ \mathbf{C_L} &= \mathbf{50pF} \end{aligned}$ | | $V_{CC} = 2.5V \pm 0.2V,$ $C_{L} = 30pF$ | | |
| Symbol | Parameter | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| t _{PHL} , t _{PLH} | Propagation Delay | 1.5 | 5.5 | 1.5 | 6.2 | 1.5 | 6.6 | ns |
| toshl, toslh | Output to Output Skew ⁽⁴⁾ | | 1.0 | | | | | ns |

Note:

4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

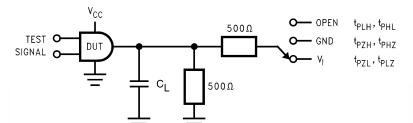
Dynamic Switching Characteristics

| | | | | $T_A = 25^{\circ}C$ | |
|------------------|---|---------------------|---|---------------------|------|
| Symbol | Parameter | V _{CC} (V) | Conditions | Typical | Unit |
| V _{OLP} | Quiet Output Dynamic Peak V _{OL} | 3.3 | $C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V$ | 0.8 | V |
| | | 2.5 | $C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V$ | 0.6 | |
| V _{OLV} | Quiet Output Dynamic Valley V _{OL} | 3.3 | $C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V$ | -0.8 | V |
| | | 2.5 | $C_L = 30pF, V_{IH} = 2.5V, V_{IL} = 0V$ | -0.6 | |

Capacitance

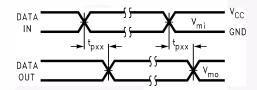
| Symbol | Parameter | Conditions | Typical | Units |
|------------------|-------------------------------|--|---------|-------|
| C _{IN} | Input Capacitance | $V_{CC} = Open, V_I = 0V \text{ or } V_{CC}$ | 7 | pF |
| C _{OUT} | Output Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC} | 8 | pF |
| C _{PD} | Power Dissipation Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC} , $f = 10MHz$ | 25 | pF |

AC Loading and Waveforms (Generic for LCX Family)

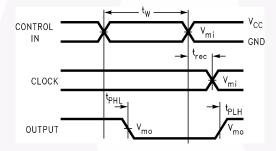


| Test | Switch |
|-------------------------------------|---|
| t _{PLH} , t _{PHL} | Open |
| t_{PZL}, t_{PLZ} | 6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$ |
| t_{PZH},t_{PHZ} | GND |

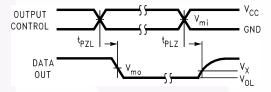
Figure 1. AC Test Circuit (C_L includes probe and jig capacitance)



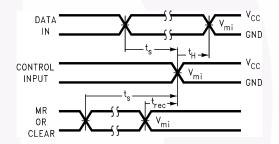
Waveform for Inverting and Non-Inverting Functions



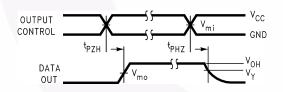
Propagation Delay. Pulse Width and t_{rec} Waveforms



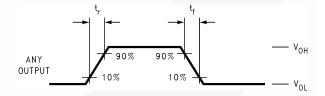
3-STATE Output Low Enable and Disable Times for Logic



Setup Time, Hold Time and Recovery Time for Logic



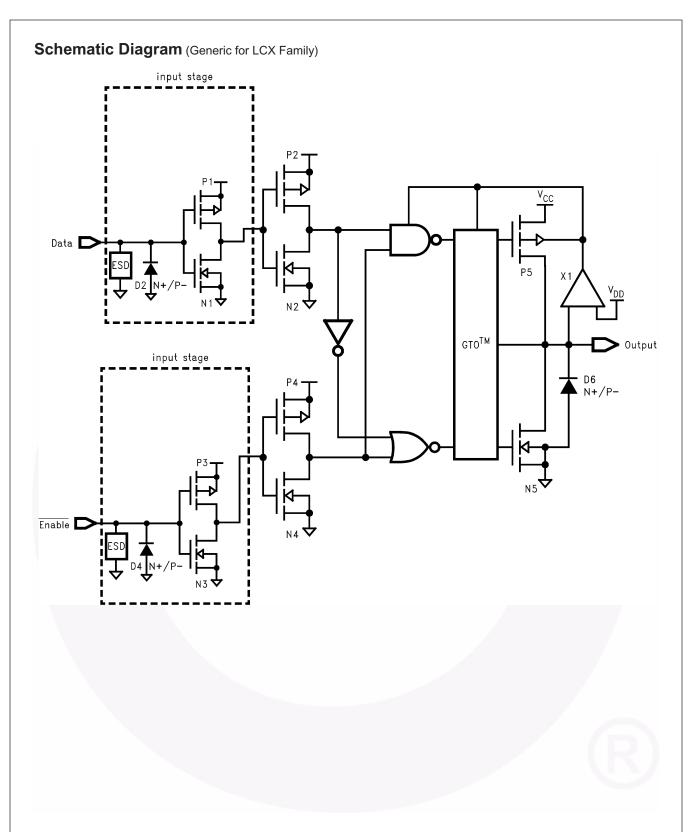




t_{rise} and t_{fall}

| | | V _{CC} | |
|-----------------|------------------------|------------------------|-------------------------|
| Symbol | 3.3V ± 0.3V | 2.7V | 2.5V ± 0.2V |
| V _{mi} | 1.5V | 1.5V | V _{CC} /2 |
| V _{mo} | 1.5V | 1.5V | V _{CC} /2 |
| V _x | V _{OL} + 0.3V | V _{OL} + 0.3V | V _{OL} + 0.15V |
| V _y | V _{OH} – 0.3V | V _{OH} – 0.3V | V _{OH} – 0.15V |

Figure 2. Waveforms (Input Characteristics; f = 1MHz, $t_r = t_f = 3ns$)

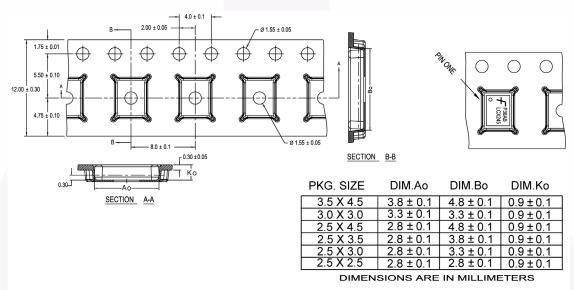


Tape and Reel Specification

Tape Format for DQFN

| Package Designator | Tape Section | Number of Cavities | Cavity Status | Cover Tape Status |
|--------------------|--------------------|--------------------|---------------|-------------------|
| BQX | Leader (Start End) | 125 (Typ.) | Empty | Sealed |
| | Carrier | 3000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (Typ.) | Empty | Sealed |

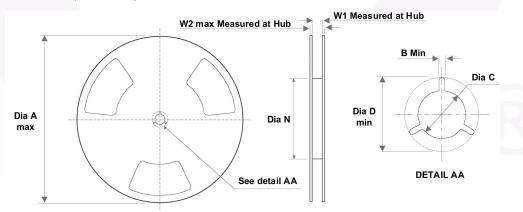
Tape Dimensions inches (millimeters)



NOTES: unless otherwise specified

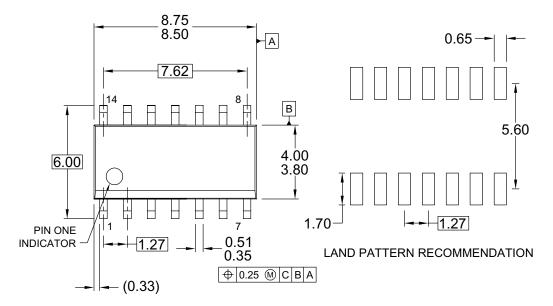
- 1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
- 2. Smallest allowable bending radius.
- 3. Thru hole inside cavity is centered within cavity.
- 4. Tolerance is $\pm 0.002[0.05]$ for these dimensions on all 12mm tapes.
- 5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
- 6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
- 7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
- 8. Controlling dimension is millimeter. Diemension in inches rounded.

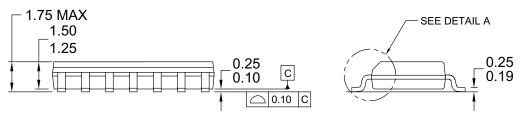
Reel Dimensions inches (millimeters)



| Tape Size | Α | В | С | D | N | W1 | W2 |
|-----------|--------------|--------------|---------------|---------------|---------------|--------------|--------------|
| 12mm | 13.0 (330.0) | 0.059 (1.50) | 0.512 (13.00) | 0.795 (20.20) | 2.165 (55.00) | 0.488 (12.4) | 0.724 (18.4) |

Physical Dimensions





NOTES: UNLESS OTHERWISE SPECIFIED

R0.10

R0.10

R0.10

Seating Plane

Seating Plane

DETAIL A

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

Figure 3. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

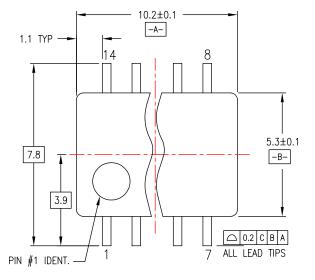
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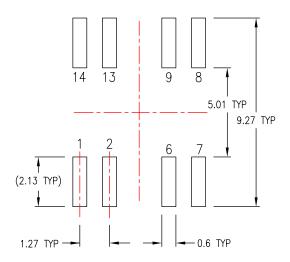
 ${\it Always\ visit\ Fairchild\ Semiconductor's\ online\ packaging\ area\ for\ the\ most\ recent\ package\ drawings:}$

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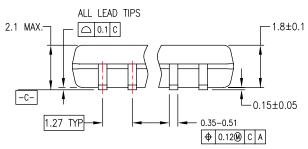
0.50 (1.04)

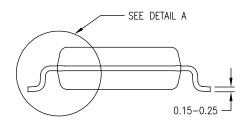
Physical Dimensions (Continued)





LAND PATTERN RECOMMENDATION



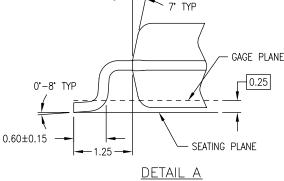


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.

- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



M14DREVC

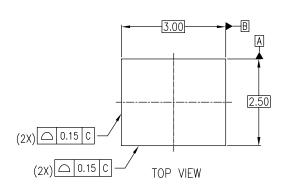
Figure 4. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

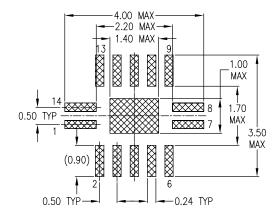
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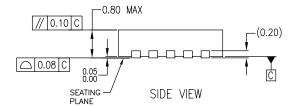
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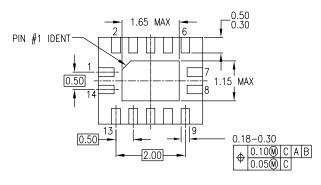
Physical Dimensions (Continued)







RECOMMENDED LAND PATTERN



BOTTOM VIEW

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP14ArevA

Figure 5. 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm

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Physical Dimensions (Continued) 5.0±0.1 -A-0.43 TYF 0.65 6.4 4.4±0.1 -B--1.65 3.2 □ 0.2 C B A PIN #1 IDENT. 6 10 LAND PATTERN RECOMMENDATION SEE DETAIL A ALL LEAD TIPS 0.90+0.15 1.2 MAX □ 0.1 C -0.10 0.09-0.20 -C-0.10±0.05 0.65 0.19 - 0.30⊕ 0.13M ABS CS 12.00°TOP & BOTTOM R0.09 min **GAGE PLANE** 0.25 0°-8° NOTES: A. CONFORMS TO JEDEC REGISTRATION MO-153. 0.6±0.1 SEATING PLANE R0.09min VARIATION AB, REF NOTE 6 1 00 **B. DIMENSIONS ARE IN MILLIMETERS DETAIL A**

- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 6. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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|---------------------------------|-----------------------|---|
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