

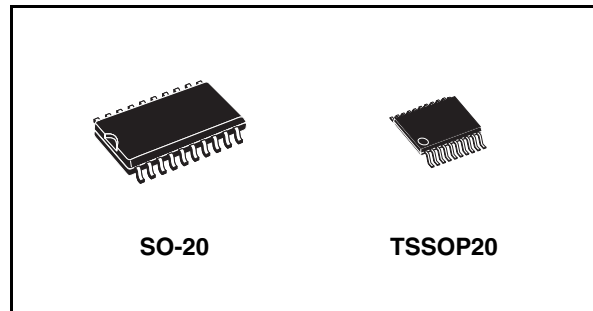


74LCX541

Low voltage CMOS octal bus buffer (3-state)
with 5V tolerant inputs and outputs

Features

- 5V tolerant inputs and outputs
- High speed:
 - $t_{PD} = 8.0\text{ns}$ (Max) at $V_{CC} = 3\text{V}$
- Power down protection on inputs and outputs
- Symmetrical output impedance:
 - $I_{OH} = I_{OL} = 24\text{mA}$ (Min) at $V_{CC} = 3\text{V}$
- PCI bus levels guaranteed at 24mA
- Balanced propagation delays:
 - $t_{PLH} \cong t_{PHL}$
- Operating voltage range:
 - $V_{CC}(\text{Opr}) = 2.0\text{V}$ to 3.6V
- Pin and function compatible with 74 series 541
- Latch-up performance exceeds 500mA (JESD 17)
- ESD performance:
 - HBM > 2000V (MIL STD 883 method 3015); MM > 200V



Description

The 74LCX541 is a low voltage CMOS octal bus buffer (non-inverted) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for both inputs and outputs.

The 3 STATE control gate operates as two input AND such that if either G1 and G2 are high, all eight outputs are in the high impedance state. In order to enhance PC board layout the 74LCX541 offers a pinout having inputs and outputs on opposite sides of the package.

It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Order codes

Part number	Package	Packaging
74LCX541MTR	SO-20	Tape and reel
74LCX541TTR	TSSOP20	Tape and reel

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1 Logic symbols and I/O equivalent circuit

Figure 1. IEC logic symbols

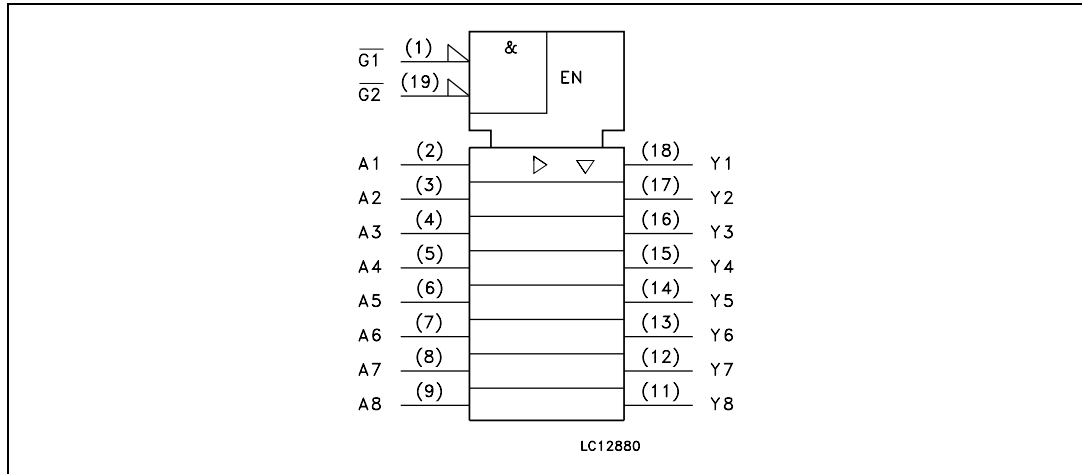
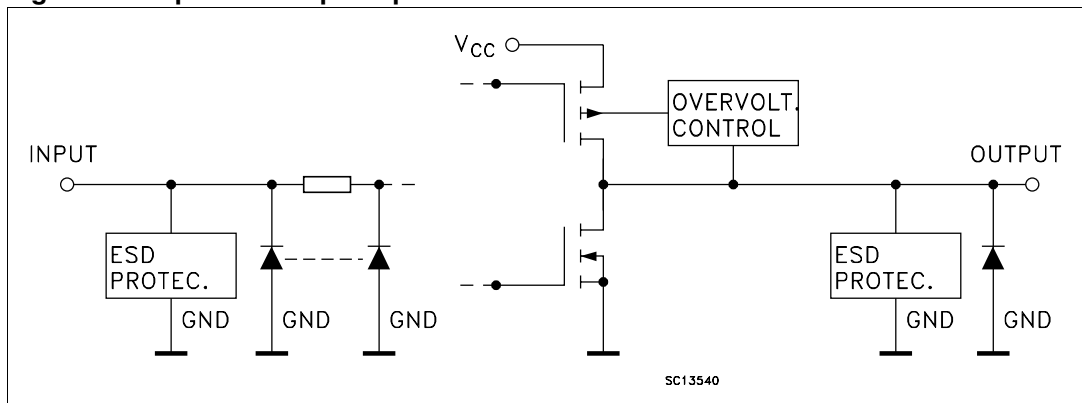


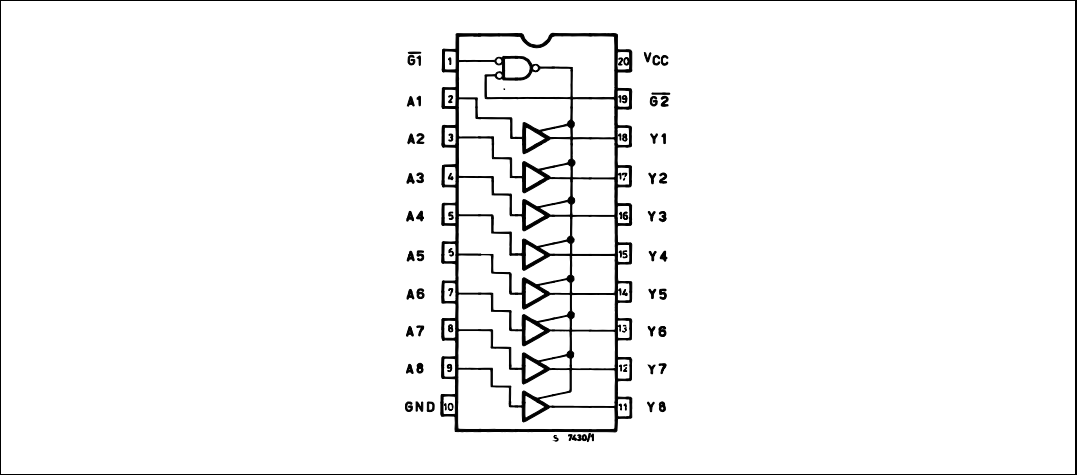
Figure 2. Input and output equivalent circuit



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top through view)



2.2 Pin description

Table 1. Pin description

Pin N°	Symbol	Name and function
1, 19	$\overline{G1}, \overline{G2}$	Output enable inputs
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data inputs
18, 17, 16, 15, 14, 13, 12, 11	$\overline{Y1}$ to $\overline{Y8}$	Data outputs
10	GND	Ground (0V)
20	V _{CC}	Positive supply voltage

3 Logic states

3.1 Truth table

Table 2. Truth table

Input			Output
$\overline{G1}$	$\overline{G2}$	An	$\overline{Yn}$
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

Note:

X : Do not care

Z : High impedance

4 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. these are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. exposure to absolute maximum rating conditions for extended periods may affect device reliability. refer also to the STMicroelectronics sure program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_I	DC input voltage	-0.5 to +7.0	V
V_O	DC output voltage (OFF state)	-0.5 to +7.0	V
V_O	DC output voltage (high or low state) ⁽¹⁾	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC input diode current	-50	mA
I_{OK}	DC output diode current ⁽²⁾	-50	mA
I_O	DC output current	±50	mA
I_{CC}	DC supply current per supply pin	± 100	mA
I_{GND}	DC ground current per supply pin	± 100	mA
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	300	°C

1. I_O absolute maximum rating must be observed

2. $V_O < GND$

4.1 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	2.0 to 3.6	V
V_I	Input voltage	0 to 5.5	V
V_O	Output voltage (OFF state)	0 to 5.5	V
V_O	Output voltage (high or low state)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or low level output current ($V_{CC} = 3.0$ to $3.6V$)	± 24	mA
I_{OH}, I_{OL}	High or low level output current ($V_{CC} = 2.7V$)	± 12	mA
T_{op}	Operating temperature	-40 to 85	°C
dt/dv	Input rise and fall time ⁽²⁾	0 to 10	ns/V

1. Truth table guaranteed: 1.5V to 3.6V

2. V_{IN} from 0.8V to 2V at $V_{CC} = 3.0V$

5 Electrical characteristics

Table 5. DC specifications

Symbol	Parameter	Test condition		Value		Unit
		V _{CC} (V)		-40 to 85°C		
				Min	Max	
V _{IH}	High level input voltage	2.7 to 3.6		2.0		V
V _{IL}	Low level input voltage				0.8	V
V _{OH}	High level output voltage	2.7 to 3.6	I _O = -100μA	V _{CC} -0.2		V
		2.7	I _O = -12mA	2.2		
		3.0	I _O = -18mA	2.4		
			I _O = -24mA	2.2		
V _{OL}	Low level output voltage	2.7 to 3.6	I _O = 100μA		0.2	V
		2.7	I _O = 12mA		0.4	
		3.0	I _O = 16mA		0.4	
			I _O = 24mA		0.55	
I _I	Input leakage current	2.7 to 3.6	V _I = 0 to 5.5V		± 5	μA
I _{off}	Power OFF leakage current	0	V _I or V _O = 5.5V		10	μA
I _{OZ}	High impedance output leakage current	2.7 to 3.6	V _I = V _{IH} or V _{IL} V _O = 0 to V _{CC}		± 5	μA
I _{CC}	Quiescent supply current	2.7 to 3.6	V _I = V _{CC} or GND		10	μA
			V _I or V _O = 3.6 to 5.5V		± 10	
ΔI _{CC}	I incr. per Input	2.7 to 3.6	V _{IH} = V _{CC} - 0.6V		500	μA

Table 6. Dynamic switching characteristics

Symbol	Parameter	Test condition		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min	Typ	Max	
V _{OLP}	Dynamic low level quiet output ⁽¹⁾	3.3	C _L = 50pF V _{IL} = 0V, V _{IH} = 3.3V		0.8		V
V _{OLV}					-0.8		

1. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

Table 7. AC electrical characteristics

Symbol	Parameter	Test condition				Value		Unit
		V _{CC} (V)	C _L (pF)	R _L (Ω)	t _s = t _r (ns)	-40 to 85 °C		
						Min	Max	
t _{PLH} t _{PHL}	Propagation delay time	2.7	50	500	2.5	1.5	9.0	ns
		3.0 to 3.6				1.5	8.0	
t _{PZL} t _{PZH}	Output enable time	2.7	50	500	2.5	1.5	9.5	ns
		3.0 to 3.6				1.5	8.5	
t _{PLZ} t _{PHZ}	Output disable time	2.7	50	500	2.5	1.5	8.5	ns
		3.0 to 3.6				1.5	7.5	
t _{OSLH} t _{OSHL}	output to output skew time ⁽¹⁾ ⁽²⁾	3.0 to 3.6	50	500	2.5		1.0	ns

- Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)
- Parameter guaranteed by design

Table 8. Capacitive characteristics

Symbol	Parameter	Test condition		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min	Typ	Max	
C _{IN}	Input capacitance	3.3	V _{IN} = 0 to V _{CC}		6		pF
C _{OUT}	Output capacitance	3.3	V _{IN} = 0 to V _{CC}		12		pF
C _{PD}	Power dissipation capacitance ⁽¹⁾	3.3	f _{IN} = 10MHz V _{IN} = 0 or V _{CC}		25		pF

- C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per buffer)

6 Test circuit

Figure 4. Test circuit

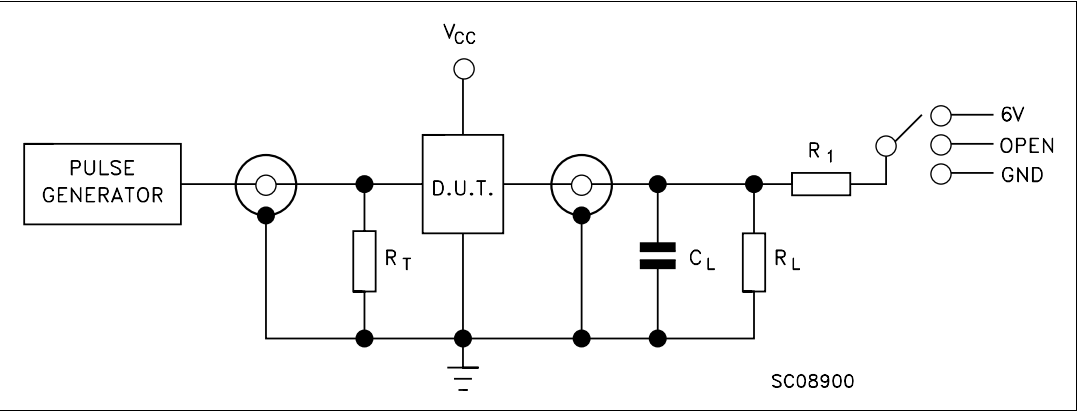


Figure 5. Test circuit

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
t_{PZH}, t_{PHZ}	GND

$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500\Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

7 Waveforms

Figure 6. Propagation delays ($f = 1\text{MHz}$; 50% duty cycle)

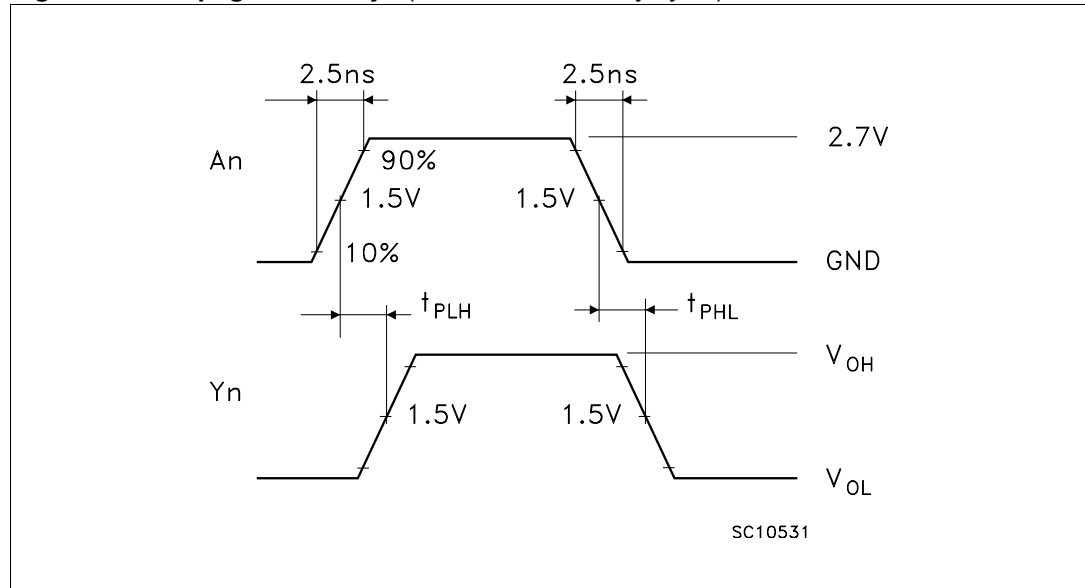
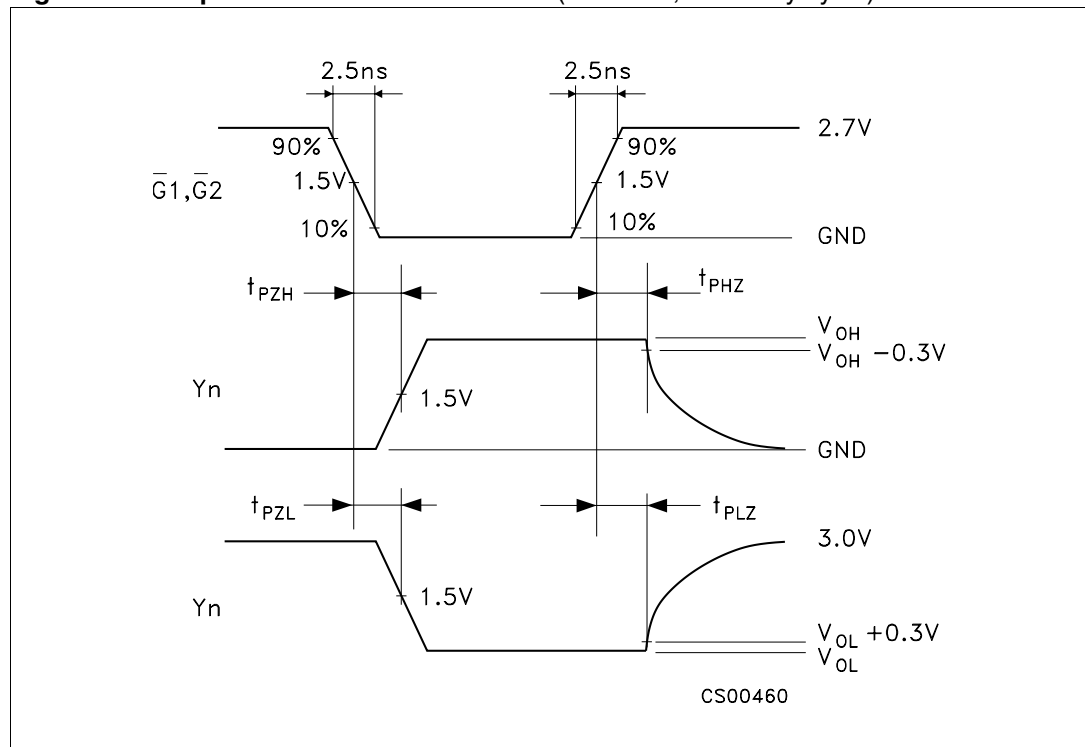
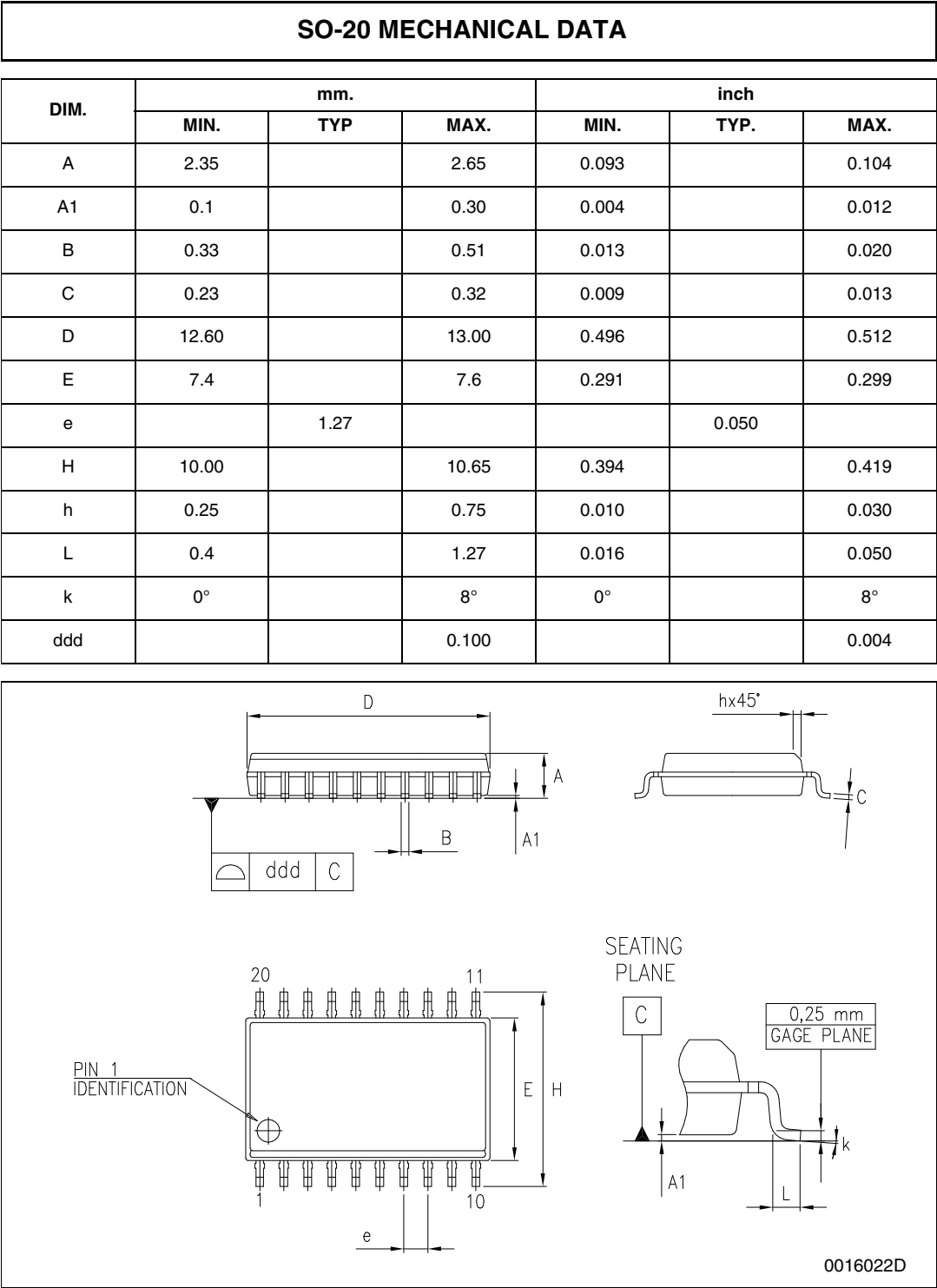


Figure 7. Output enable and disable time ($f = 1\text{MHz}$; 50% duty cycle)



8 Package mechanical data

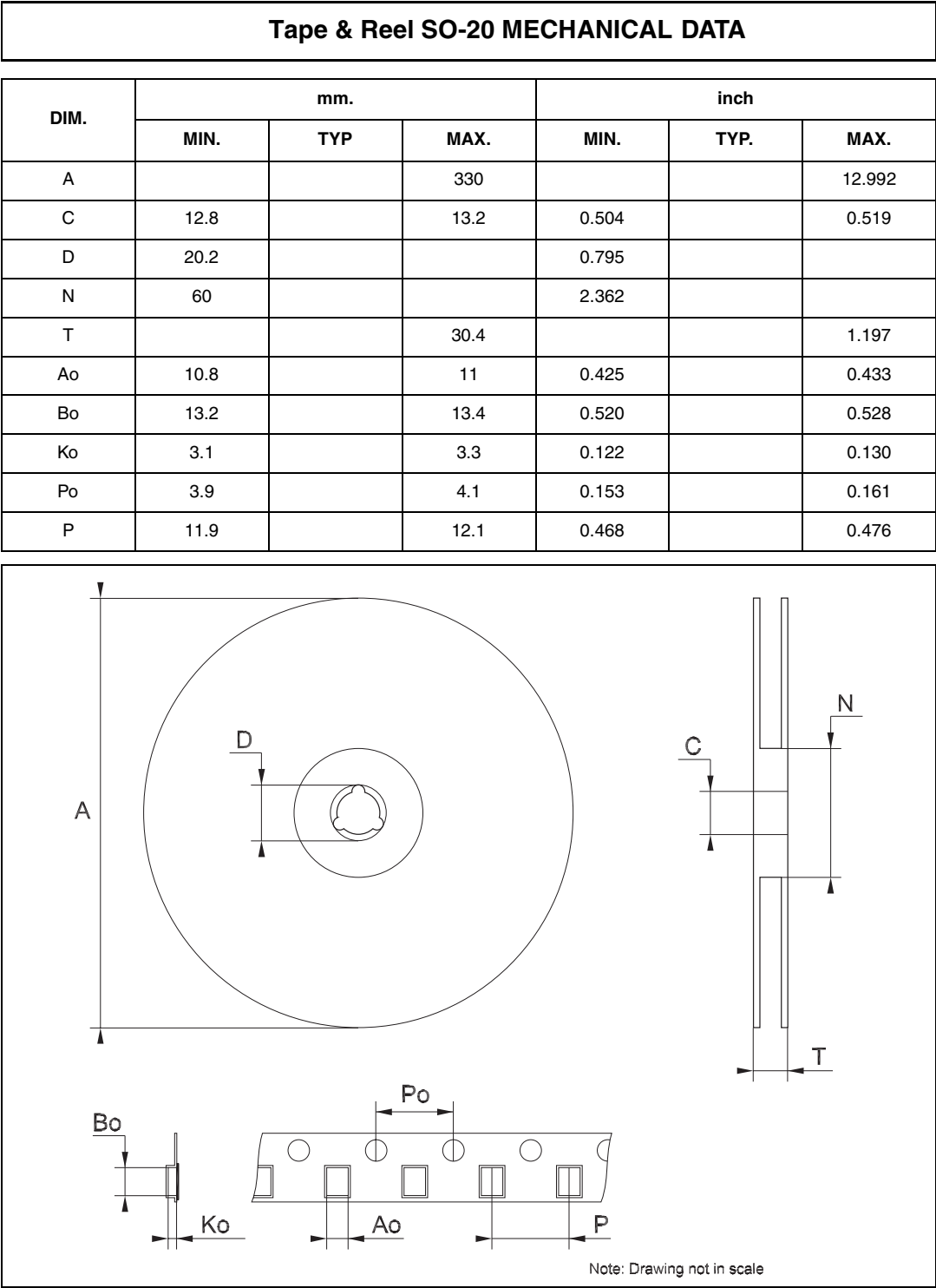
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com



TSSOP20 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

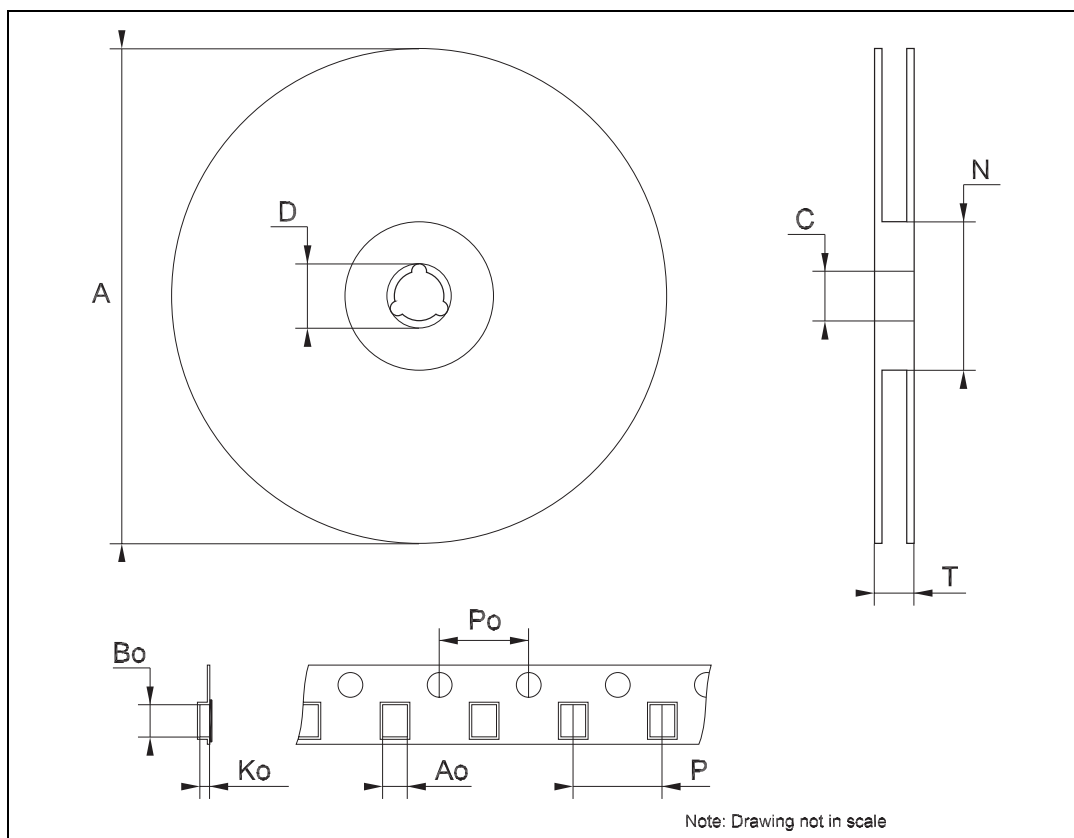
The diagram illustrates the mechanical specifications of the TSSOP20 package. It includes three views: a top view showing the package footprint with dimensions D (width) and E1 (height), a side view showing the profile with dimensions A (total height), A1 (lead height), A2 (lead length), b (lead width), c (lead thickness), and E (body width), and a detail view of the lead with dimensions K (lead angle) and L (lead thickness). A circular feature on the top view is labeled 'PIN 1 IDENTIFICATION' with a '1' indicating the starting point of the pin sequence.

0087225C



Tape & Reel TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	6.9		7.1	0.272		0.280
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



9 Revision history

Table 9. Revision history

Date	Revision	Changes
15-Sep-2004	4	Ordering Codes Revision - pag. 1.
24-Jan-2007	5	The document has been reformatted, temperature ranges updated

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