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Kind regards,

Team Nexperia

74LV393

Dual 4-bit binary ripple counter

Rev. 5 — 8 December 2015

Product data sheet

1. General description

The 74LV393 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC393 and 74HCT393.

The 74LV393 is a dual 4-stage binary ripple counter. Each counter features a clock input ($\overline{nCP}$), an overriding asynchronous master reset input ($\overline{nMR}$) and 4 buffered parallel outputs ($nQ0$ to $nQ3$). The counter advances on the HIGH-to-LOW transition of $\overline{nCP}$. A HIGH on $\overline{nMR}$ clears the counter stages and forces the outputs LOW, independent of the state of $\overline{nCP}$.

2. Features and benefits

- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical V_{OLP} (output ground bounce) 0.8 V at $V_{CC} = 3.3$ V, $T_{amb} = 25$ °C
- Typical V_{OHV} (output V_{OH} undershoot) 2 V at $V_{CC} = 3.3$ V, $T_{amb} = 25$ °C
- Two 4-bit binary counters with individual clocks
- Divide-by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

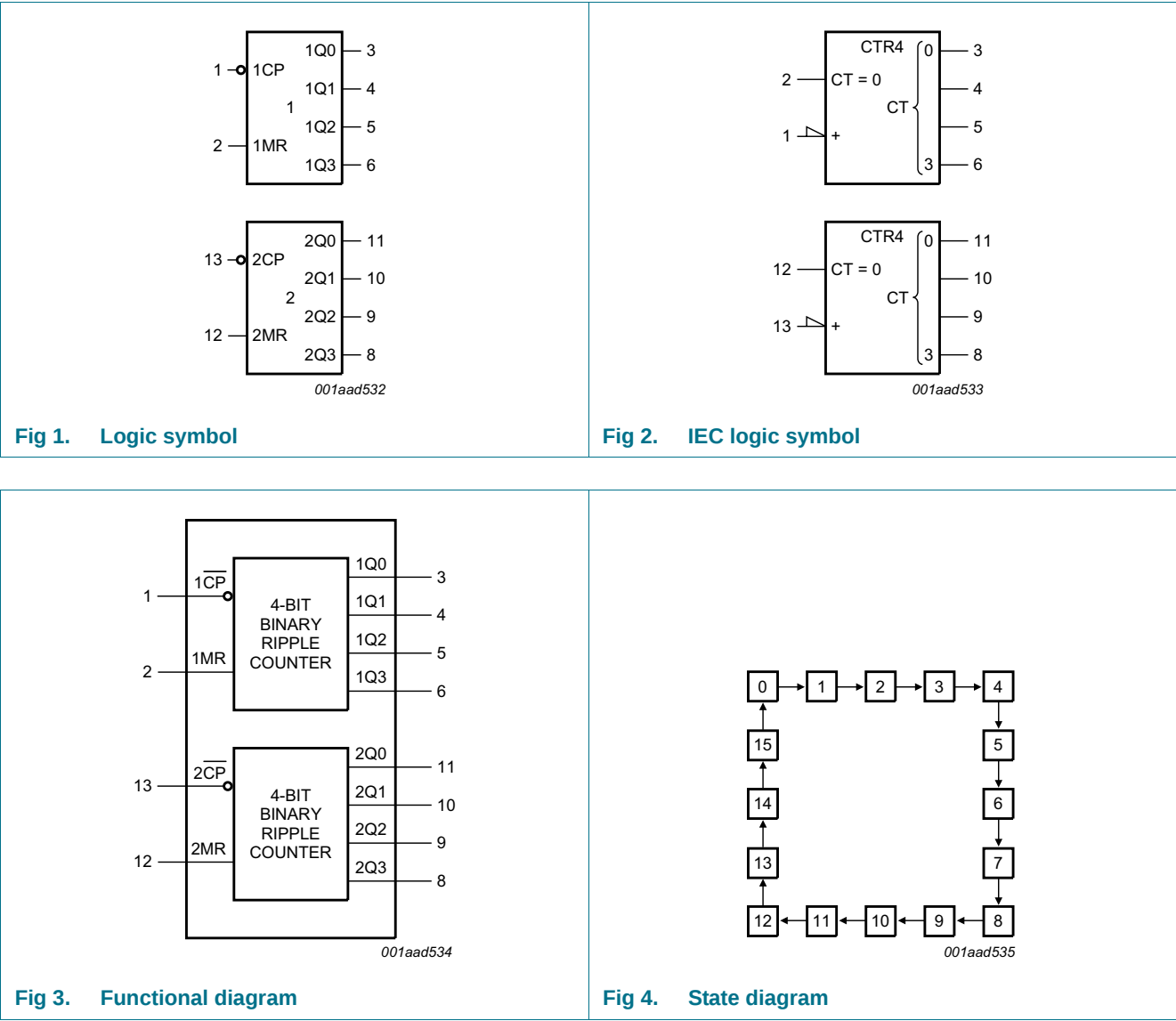
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV393D	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV393DB	−40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV393PW	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1



4. Functional diagram



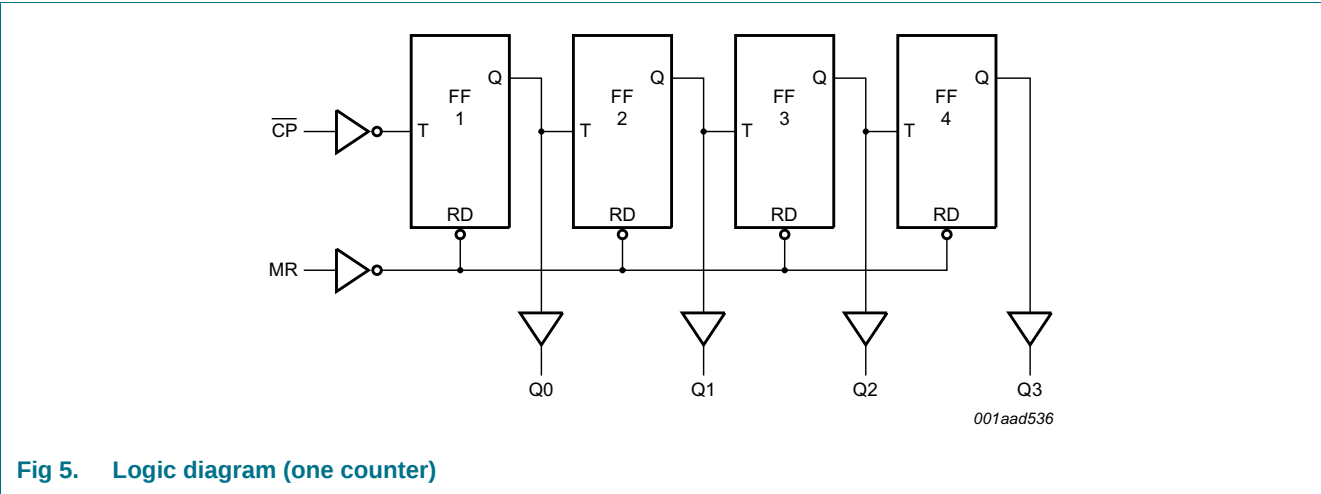


Fig 5. Logic diagram (one counter)

5. Pinning information

5.1 Pinning

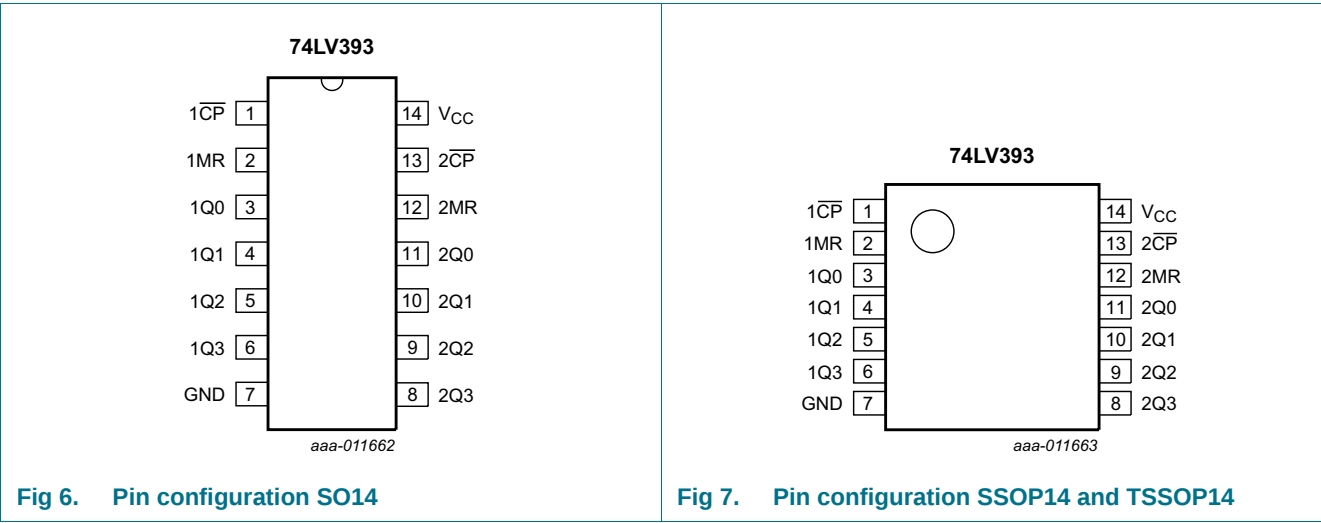


Fig 6. Pin configuration SO14

Fig 7. Pin configuration SSOP14 and TSSOP14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1CP, 2CP	1, 13	clock input (HIGH-to-LOW, edge-triggered)
1MR, 2MR	2, 12	asynchronous master reset input (active HIGH)
1Q0, 1Q1, 1Q2, 1Q3	3, 4, 5, 6	flip-flop output
GND	7	ground (0 V)
2Q0, 2Q1, 2Q2, 2Q3	11, 10, 9, 8	flip-flop output
VCC	14	supply voltage

6. Functional description

Table 3. Count sequence for one counter [1]

Count	Output			
	nQ0	nQ1	nQ2	nQ3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

[1] H = HIGH voltage level; L = LOW voltage level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 50	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		SO14 package [1]	-	500	mW
		(T)SSOP14 package [2]	-	400	mW

[1] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[2] For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.0	3.3	3.6	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V _{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V _{CC} = 2.7 V to 3.6 V	-	-	100	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V _{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V _{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.2 V	-	1.2	-	-	-	V
		I _O = -100 μA; V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I _O = -100 μA; V _{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I _O = -100 μA; V _{CC} = 3.0 V	2.80	3.0	-	2.8	-	V
		I _O = -6 mA; V _{CC} = 3.0 V	2.40	2.82	-	2.20	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.2 V	-	0	-	-	-	V
		I _O = 100 μA; V _{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I _O = 100 μA; V _{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I _O = 100 μA; V _{CC} = 3.0 V	-	0	0.2	-	0.2	V
		I _O = 6 mA; V _{CC} = 3.0 V	-	0.25	0.40	-	0.50	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 3.6 V	-	-	1.0	-	1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 3.6 V	-	-	20.0	-	160	μA
ΔI _{CC}	additional quiescent supply current per input	V _I = V _{CC} - 0.6 V; V _{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C _I	input capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 10](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	$\overline{nCP}$ to $nQ0$; see Figure 8 ^[3]						
		$V_{CC} = 1.2$ V	-	75	-	-	-	ns
		$V_{CC} = 2.0$ V	-	26	49	-	60	ns
		$V_{CC} = 2.7$ V	-	19	36	-	44	ns
		$V_{CC} = 3.3$ V, $C_L = 15$ pF	-	12	-	-	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	-	14	29	-	35	ns
		nQ to $nQn+1$; see Figure 8 ^[3]						
		$V_{CC} = 1.2$ V	-	25	-	-	-	ns
		$V_{CC} = 2.0$ V	-	9	17	-	20	ns
		$V_{CC} = 2.7$ V	-	6	13	-	15	ns
		$V_{CC} = 3.3$ V, $C_L = 15$ pF	-	4	-	-	-	ns
		$V_{CC} = 3.0$ V to 3.6 V ^[2]	-	5	10	-	12	ns
t_{PHL}	HIGH to LOW propagation delay	nMR to nQx ; see Figure 9						
		$V_{CC} = 1.2$ V	-	70	-	-	-	ns
		$V_{CC} = 2.0$ V	-	24	44	-	54	ns
		$V_{CC} = 2.7$ V	-	18	33	-	40	ns
		$V_{CC} = 3.3$ V, $C_L = 15$ pF	-	11	-	-	-	ns
		$V_{CC} = 3.0$ V to 3.6 V ^[2]	-	13	26	-	32	ns
t_t	transition time	nQx ; see Figure 8 ^[4]						
		$V_{CC} = 2.0$ V	-	-	-	-	-	ns
		$V_{CC} = 2.7$ V	-	-	-	-	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	-	-	-	-	-	ns
t_w	pulse width	$\overline{nCP}$ HIGH or LOW; see Figure 8						
		$V_{CC} = 2.0$ V	34	10	-	41	-	ns
		$V_{CC} = 2.7$ V	25	8	-	30	-	ns
		$V_{CC} = 3.0$ V to 3.6 V ^[2]	20	6	-	24	-	ns
		nMR HIGH; see Figure 9						
		$V_{CC} = 2.0$ V	34	12	-	41	-	ns
		$V_{CC} = 2.7$ V	25	9	-	30	-	ns
		$V_{CC} = 3.0$ V to 3.6 V ^[2]	20	7	-	24	-	ns
t_{rec}	recovery time	nMR to $\overline{nCP}$; see Figure 9						
		$V_{CC} = 1.2$ V	-	5	-	-	-	ns
		$V_{CC} = 2.0$ V	5	2	-	5	-	ns
		$V_{CC} = 2.7$ V	5	2	-	5	-	ns
		$V_{CC} = 3.0$ V to 3.6 V ^[2]	5	1	-	5	-	ns

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 10](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
$f_{\max}$	maximum frequency	see Figure 8						
		$V_{CC} = 2.0$ V	14	53	-	12	-	MHz
		$V_{CC} = 2.7$ V	19	72	-	16	-	MHz
		$V_{CC} = 3.3$ V, $C_L = 15$ pF	-	99	-	-	-	MHz
		$V_{CC} = 3.0$ V to 3.6 V ^[2]	24	90	-	20	-	MHz
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$ ^[2] ^[5]	-	23	-	-	-	pF

[1] All typical values are measured at $T_{\text{amb}} = 25$ °C.

[2] Typical values are measured at $V_{CC} = 3.3$ V.

[3] t_{pd} is the same as t_{PLH} and t_{PHL} .

[4] t_t is the same as t_{THL} and t_{TLH} .

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1 Waveforms

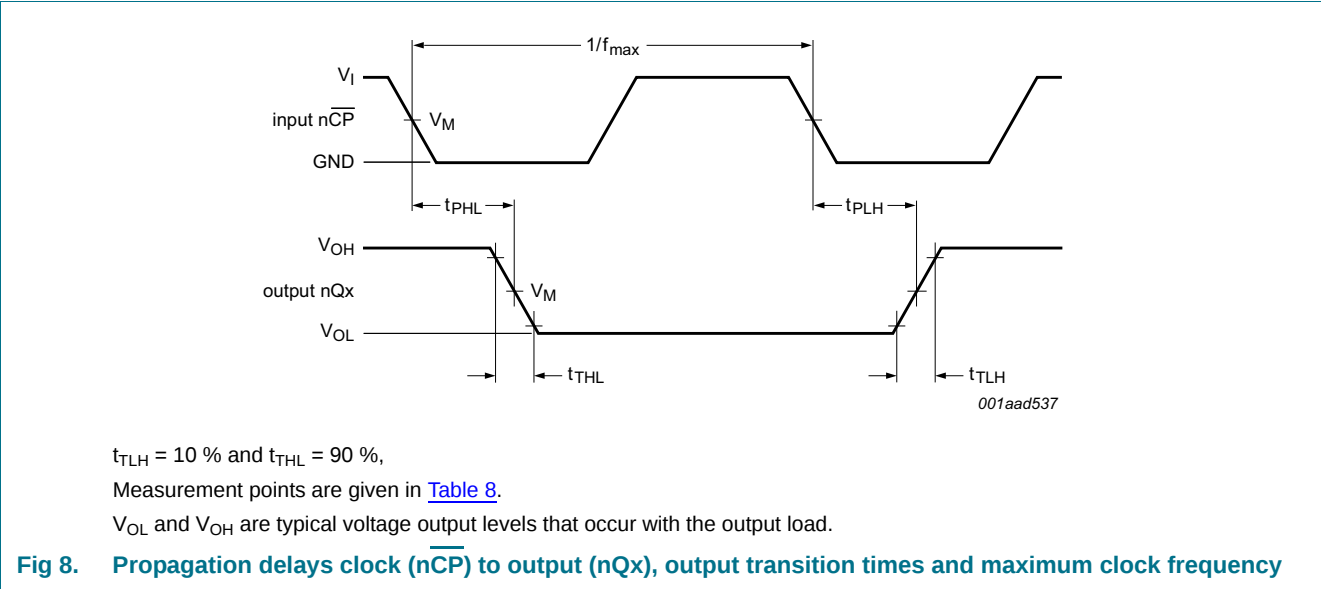
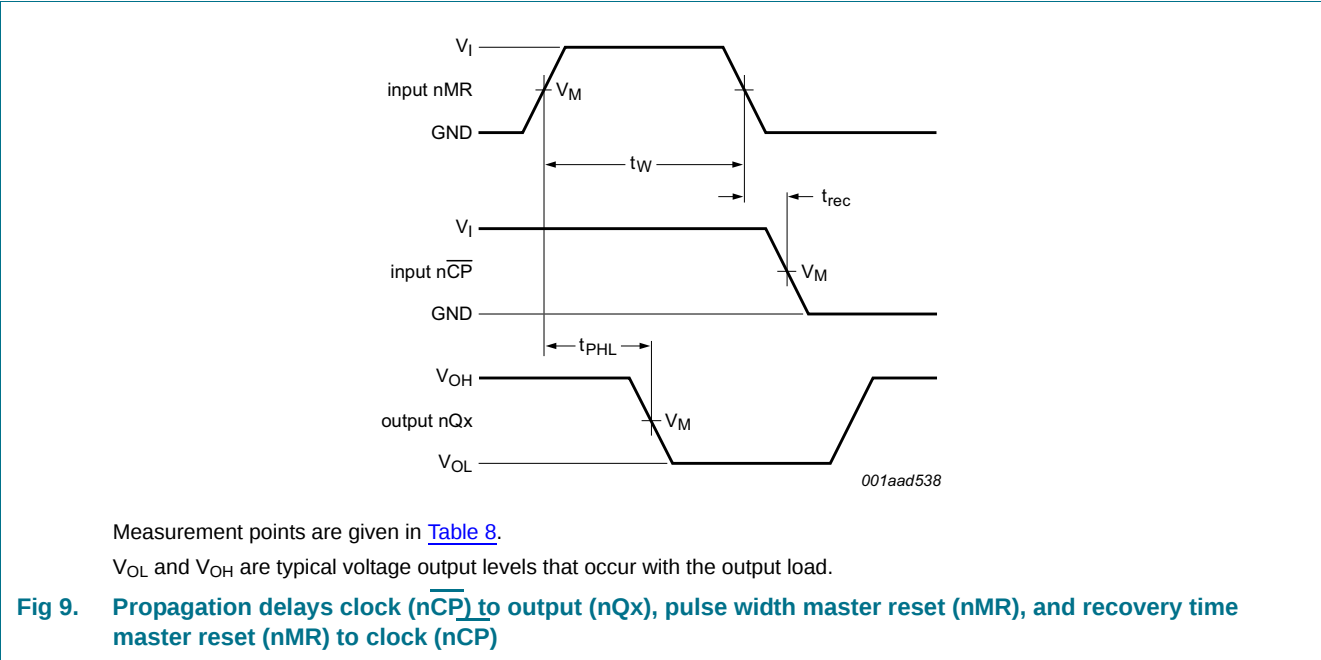
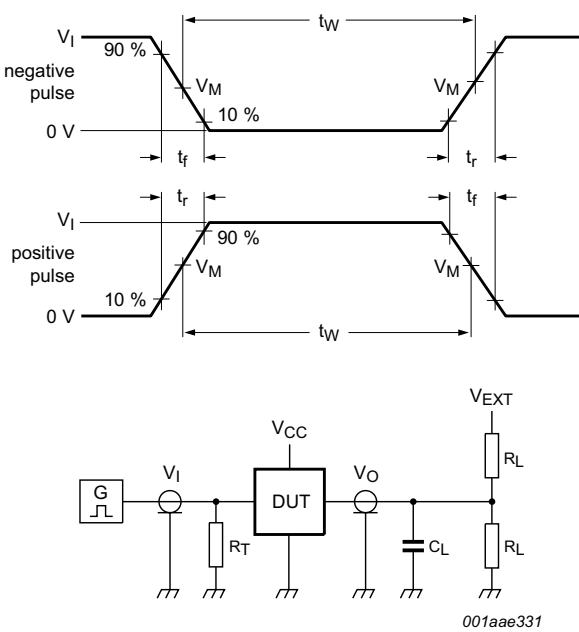


Table 8. Measurement points

Supply voltage V_{CC}	Input	Output		
	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	$1.5V_{CC}$	$1.5V_{CC}$	$V_{OL} + 0.3V_{CC}$	$V_{OH} - 0.3V_{CC}$





Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 k Ω	open
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	15 pF, 50 pF	1 k Ω	open

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

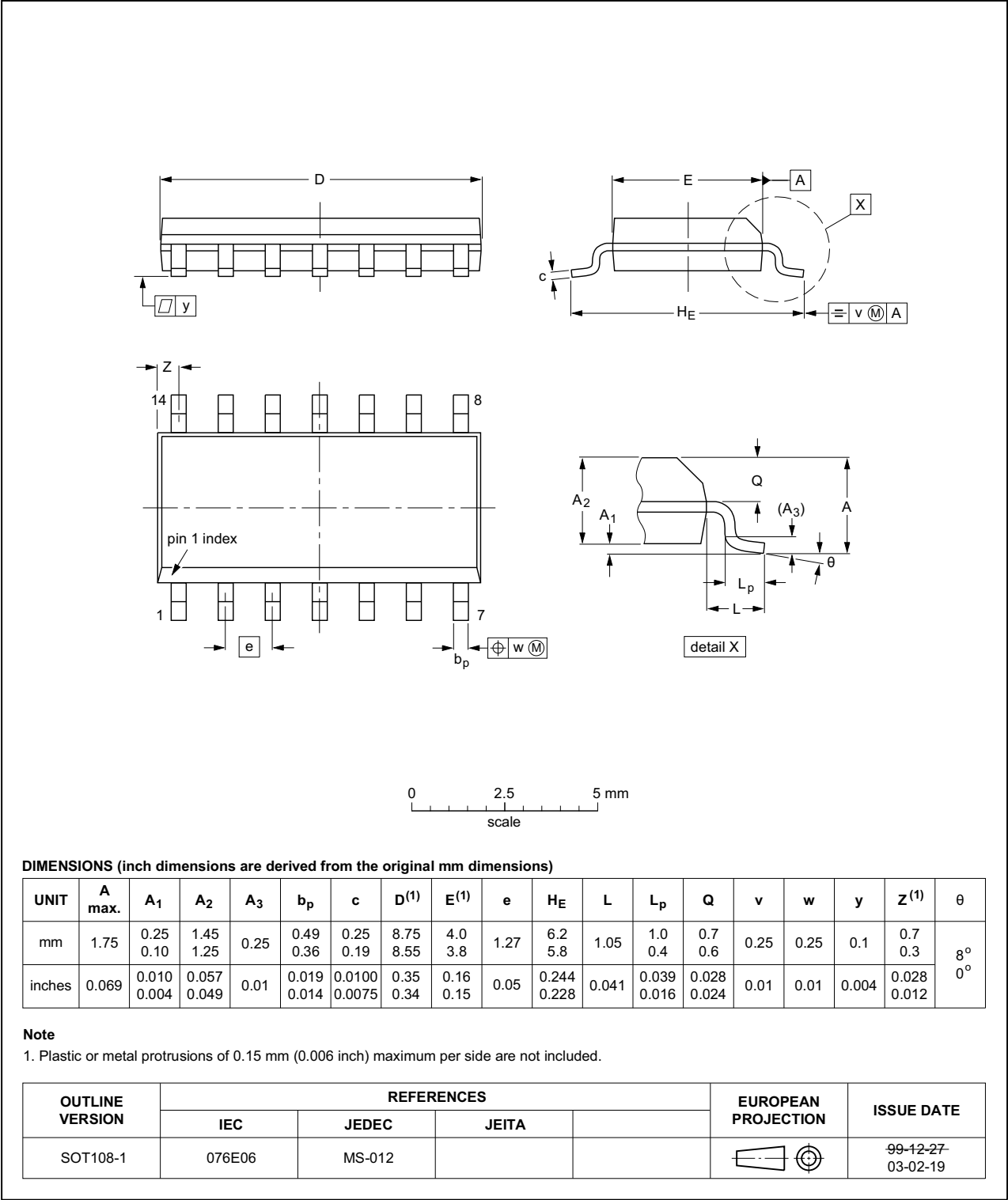


Fig 11. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

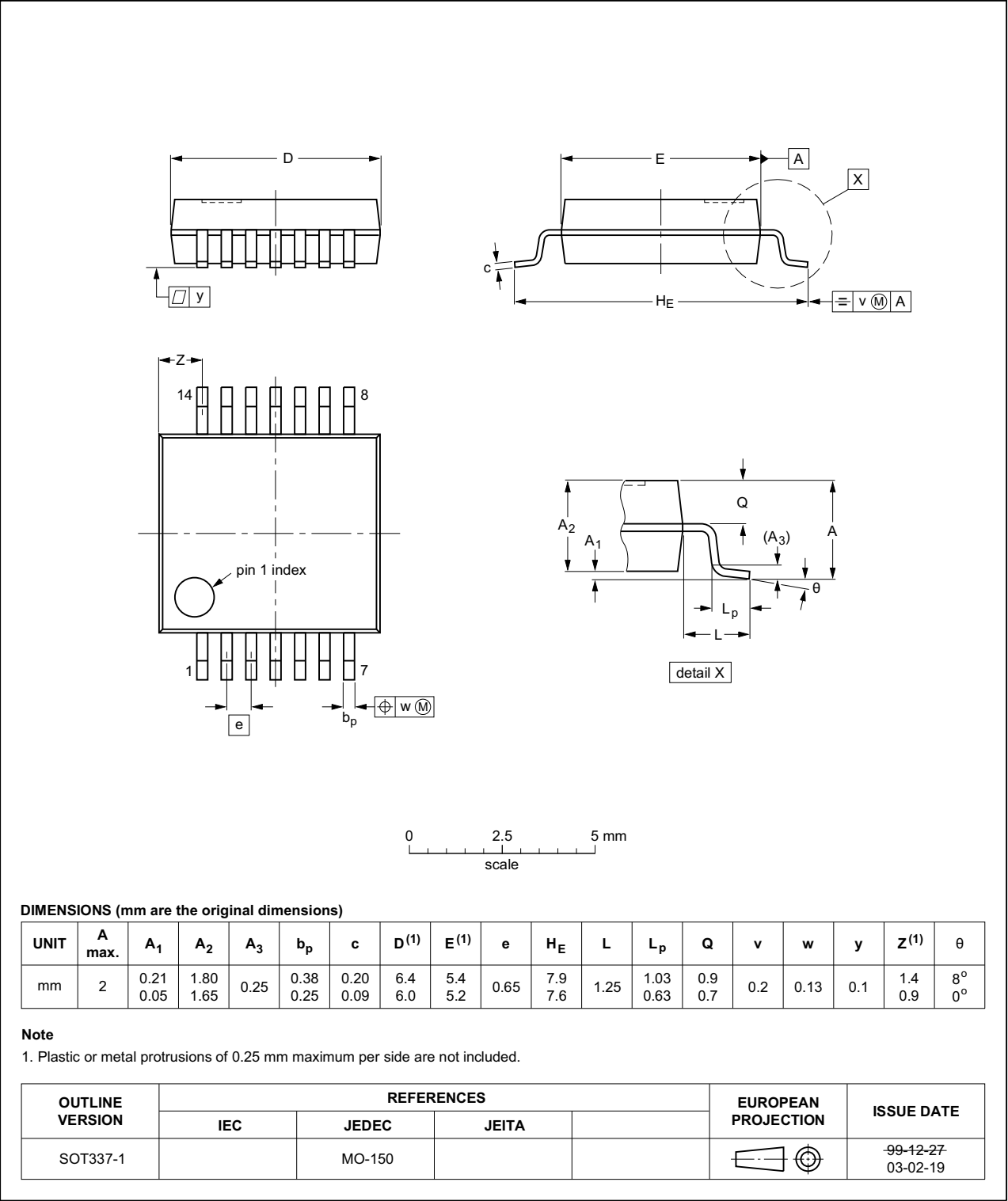


Fig 12. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

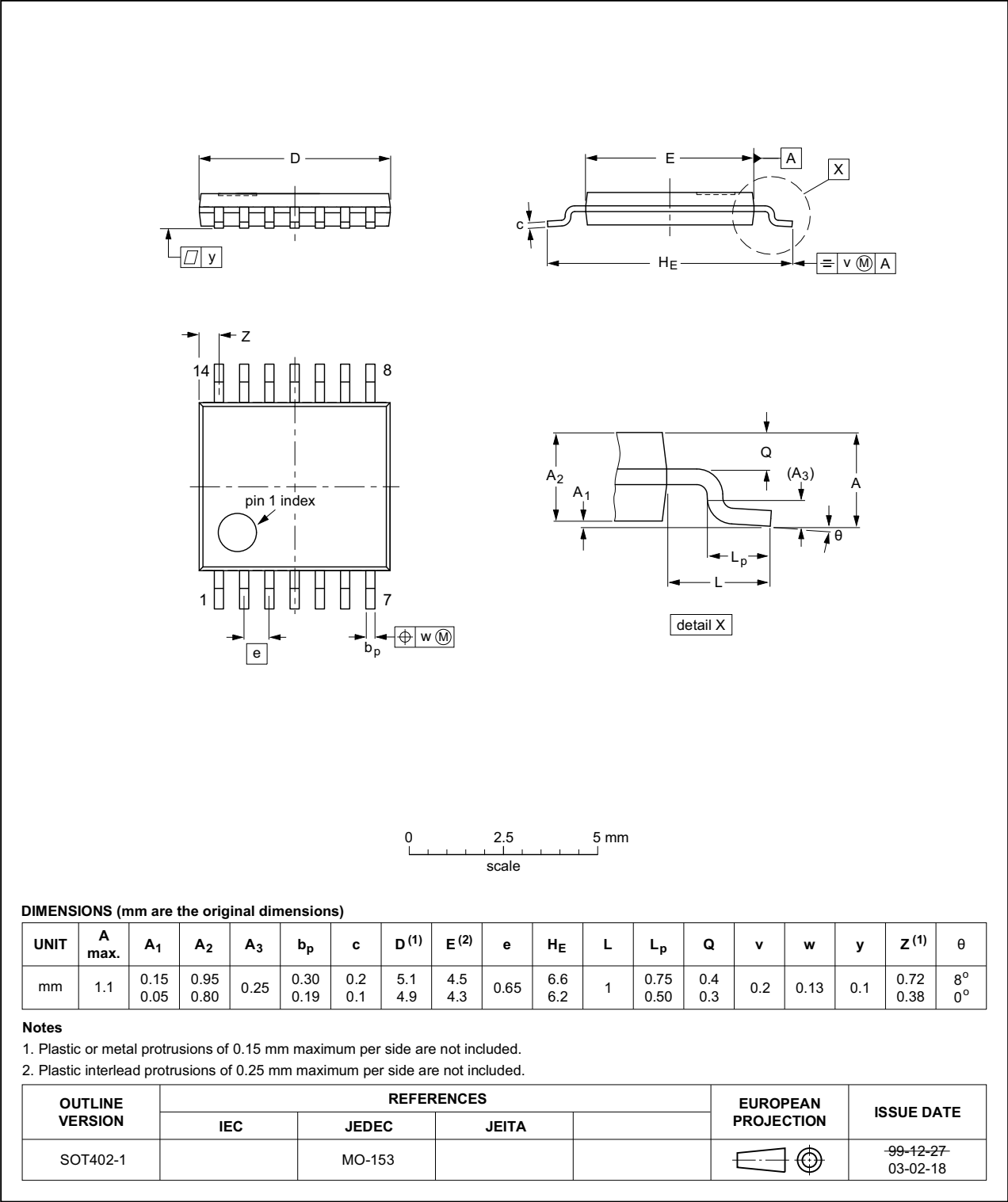


Fig 13. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV393 v.5	20151208	Product data sheet	-	74LV393 v.4
Modifications:	Type number 74LV393N (SOT27-1) removed.			
74LV393 v.4	20140918	Product data sheet	-	74LV393 v.3
Modifications:	Table 4 minus sign added to the minimum ground current. Figure 10 and Table 9 updated because of a missing load resistance in the test circuit.			
74LV393 v.3	20140428	Product data sheet	-	74LV393 v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate.			
74LV393 v.2	19970610	Product specification	-	74LV393 v.1
74LV393 v.1	19970304	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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