

74LV4060

14-stage binary ripple counter with oscillator

Rev. 3 — 28 July 2014

Product data sheet

1. General description

The 74LV4060 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC4060; 74HCT4060.

The 74LV4060 is a 14-stage ripple-carry counter/divider and oscillator with three oscillator terminals (RS, RTC and CTC). It has ten buffered outputs (Q3 to Q9 and Q11 to Q13) and an overriding asynchronous master reset (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator can be replaced by an external clock signal at input RS. In this case, keep the oscillator pins (RTC and CTC) floating.

The counter advances on the negative-going transition of RS. A HIGH-level on MR resets the counter (Q3 to Q9 and Q11 to Q13 = LOW), independent of the other input conditions.

2. Features and benefits

- Wide operating voltage range from 1.0 V to 5.5 V
- Optimized for low voltage applications from 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical V_{OLP} (output ground bounce) < 0.8 V at $V_{CC} = 3.3$ V; $T_{amb} = 25$ °C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at $V_{CC} = 3.3$ V; $T_{amb} = 25$ °C
- All active components on-chip
- RC or crystal oscillator configuration
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115A exceeds 200 V

3. Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits



4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4060N	−40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74LV4060D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4060DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LV4060PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

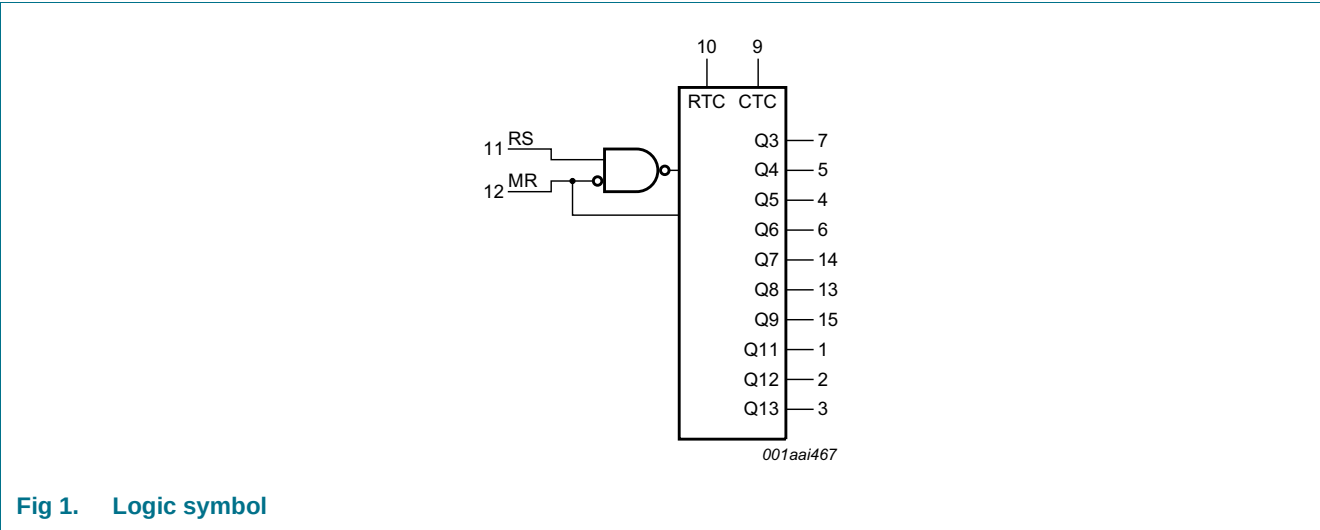


Fig 1. Logic symbol

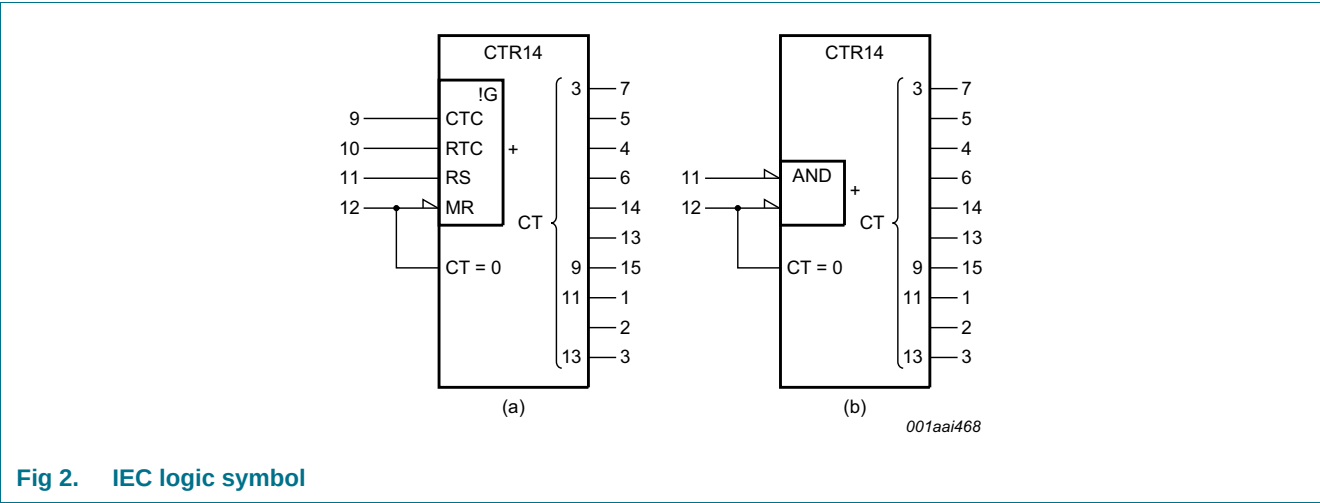


Fig 2. IEC logic symbol

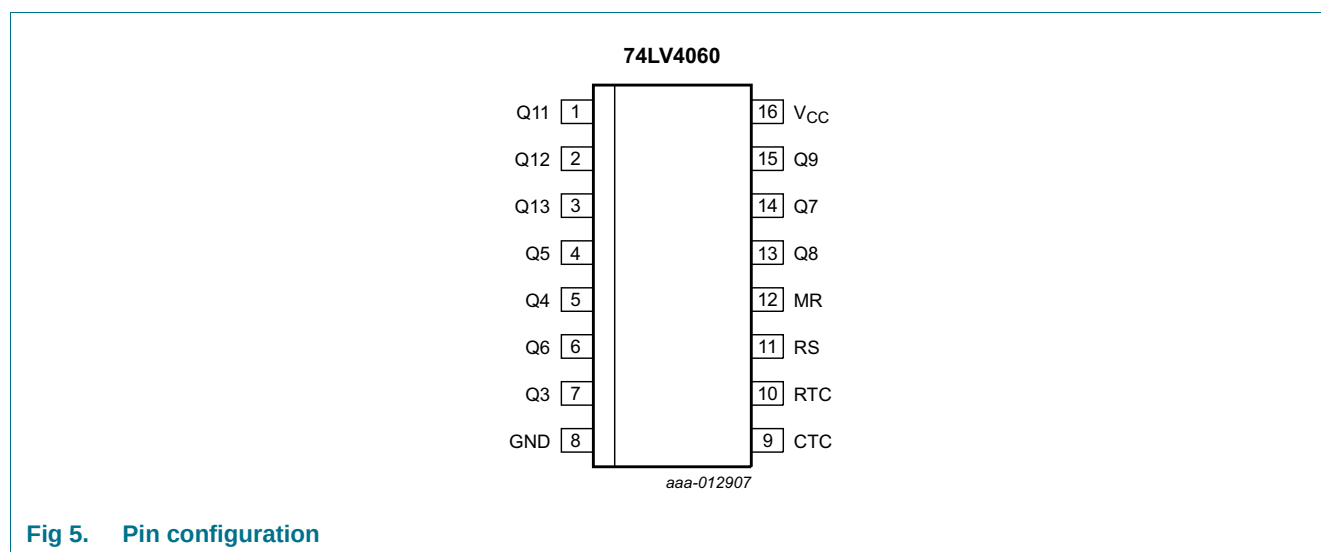
The diagram shows a 14-stage binary counter with the following inputs and outputs:

- Inputs:**
 - RS (Reset Set):** Input 11, connected to the RS input of an RS flip-flop.
 - MR (Master Reset):** Input 12, connected to the MR input of the 14-stage binary counter.
 - CTC (Counter Terminal Count):** Input 9, connected to the CTC input of the 14-stage binary counter.
 - RTC (Reset Terminal Count):** Input 10, connected to the RTC input of the 14-stage binary counter.
- Outputs:**
 - Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q11, Q12, Q13:** The 10 outputs of the 14-stage binary counter, labeled with their respective pin numbers (7, 5, 4, 6, 14, 13, 15, 1, 2, 3).

The counter is a 14-stage binary counter, and the outputs are labeled Q3 through Q13. The pin numbers for the outputs are 7, 5, 4, 6, 14, 13, 15, 1, 2, and 3 respectively.

6. Pinning information

6.1 Pinning



74LV4060

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q11 to Q13	1, 2, 3	counter output
Q3 to Q9	7, 5, 4, 6, 14, 13, 15	counter output
GND	8	ground (0 V)
CTC	9	external capacitor connection
RTC	10	external resistor connection
RS	11	clock input/oscillator pin
MR	12	master reset
V _{CC}	16	supply voltage

7. Functional description

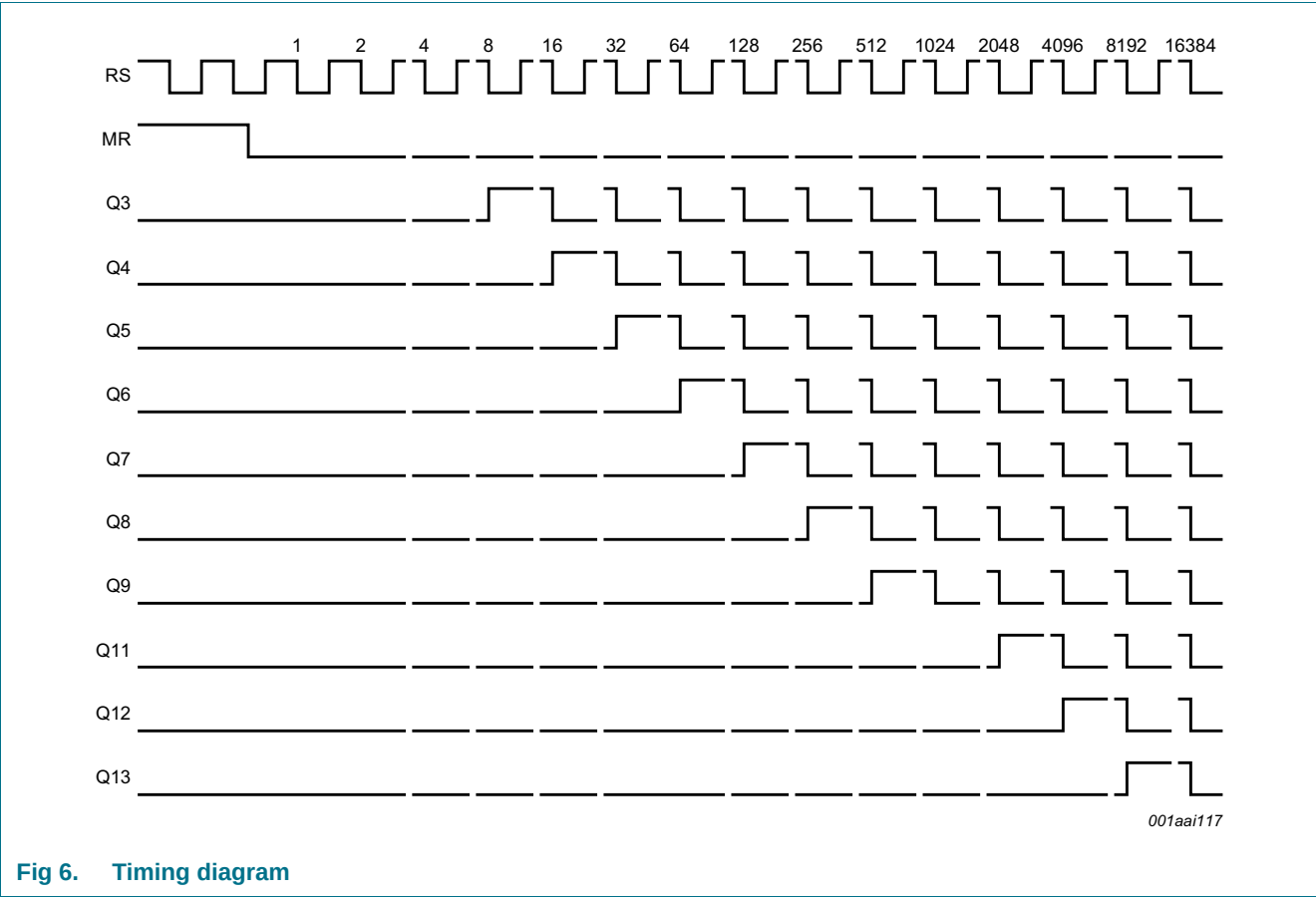


Fig 6. Timing diagram

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	± 50	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		DIP16package [2]	-	750	mW
		SO16 package [3]	-	500	mW
		SSOP16 package [4]	-	400	mW
		TSSOP16 package [4]	-	400	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V}$ to 2.0 V	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V}$ to 2.7 V	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	-	-	100	ns/V
		$V_{CC} = 3.6\text{ V}$ to 5.5 V	-	-	50	ns/V

[1] The 74LV4060 is guaranteed to function down to $V_{CC} = 1.0\text{ V}$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 5.5\text{ V}$.

10. Static characteristics

Table 5. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	MR input						
		V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V _{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	V
		RS input						
		V _{CC} = 1.2 V	1.0	-	-	1.0	-	V
		V _{CC} = 2.0 V	1.6	-	-	1.6	-	V
		V _{CC} = 2.7 V to 3.6 V	2.4	-	-	2.4	-	V
		V _{CC} = 4.5 V to 5.5 V	0.8V _{CC}	-	-	0.8V _{CC}	-	V
V _{IL}	LOW-level input voltage	MR input						
		V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V _{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	V
		RS input						
		V _{CC} = 1.2 V	-	-	0.2	-	0.2	V
		V _{CC} = 2.0 V	-	-	0.4	-	0.4	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.5	-	0.5	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.2V _{CC}	-	0.2V _{CC}	V
V _{OH}	HIGH-level output voltage	RTC output; RS = MR = GND						
		V _{CC} = 1.2 V; I _O = –3.4 mA	-	-	-	-	-	V
		V _{CC} = 2.0 V; I _O = –3.4 mA	-	-	-	-	-	V
		V _{CC} = 2.7 V; I _O = –3.4 mA	-	-	-	-	-	V
		V _{CC} = 3.0 V; I _O = –3.4 mA	2.40	2.82	-	2.20	-	V
		V _{CC} = 4.5 V; I _O = –3.4 mA	-	-	-	-	-	V
		RTC output; RS = MR = V _{CC}						
		V _{CC} = 1.2 V; I _O = –0.8 mA	-	-	-	-	-	V
		V _{CC} = 2.0 V; I _O = –0.8 mA	-	-	-	-	-	V
		V _{CC} = 2.7 V; I _O = –0.8 mA	-	-	-	-	-	V
		V _{CC} = 3.0 V; I _O = –0.8 mA	2.40	2.82	-	2.20	-	V
		V _{CC} = 4.5 V; I _O = –0.8 mA	-	-	-	-	-	V

Table 5. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{OH}	HIGH-level output voltage	RTC output; RS = MR = GND						
		V _{CC} = 1.2 V; I _O = -100 µA	1.0	1.2	-	1.0	-	V
		V _{CC} = 2.0 V; I _O = -100 µA	1.8	2.0	-	1.8	-	V
		V _{CC} = 2.7 V; I _O = -100 µA	-	-	-	-	-	V
		V _{CC} = 3.0 V; I _O = -100 µA	2.8	3.0	-	2.8	-	V
		V _{CC} = 4.5 V; I _O = -100 µA	-	-	-	-	-	V
		RTC output; RS = MR = V _{CC}						
		V _{CC} = 1.2 V; I _O = -100 µA	1.0	1.2	-	1.0	-	V
		V _{CC} = 2.0 V; I _O = -100 µA	1.8	2.0	-	1.8	-	V
		V _{CC} = 2.7 V; I _O = -100 µA	-	-	-	-	-	V
		V _{CC} = 3.0 V; I _O = -100 µA	2.8	3.0	-	2.8	-	V
		V _{CC} = 4.5 V; I _O = -100 µA	-	-	-	-	-	V
		CTC output; RS = V _{IH} and MR = V _{IL}						
		V _{CC} = 1.2 V; I _O = -3.8 mA	-	1.2	-	-	-	V
		V _{CC} = 2.0 V; I _O = -3.8 mA	-	-	-	-	-	V
		V _{CC} = 2.7 V; I _O = -3.8 mA	-	-	-	-	-	V
		V _{CC} = 3.0 V; I _O = -3.8 mA	2.40	2.82	-	2.20	-	V
		V _{CC} = 4.5 V; I _O = -3.8 mA	-	-	-	-	-	V
		except RTC output; V _I = V _{IH} or V _{IL}						
		V _{CC} = 1.2 V; I _O = -100 µA	1.0	1.2	-	1.0	-	V
		V _{CC} = 2.0 V; I _O = -100 µA	1.8	2.0	-	1.8	-	V
		V _{CC} = 2.7 V; I _O = -100 µA	-	-	-	-	-	V
		V _{CC} = 3.0 V; I _O = -100 µA	2.8	3.0	-	2.8	-	V
		V _{CC} = 4.5 V; I _O = -100 µA	-	-	-	-	-	V
		except RTC and CTC outputs; V _I = V _{IH} or V _{IL}						
		V _{CC} = 1.2 V; I _O = -6 mA	-	-	-	-	-	V
		V _{CC} = 2.0 V; I _O = -6 mA	-	-	-	-	-	V
		V _{CC} = 2.7 V; I _O = -6 mA	-	-	-	-	-	V
		V _{CC} = 3.0 V; I _O = -6 mA	2.40	2.82	-	2.20	-	V
		V _{CC} = 4.5 V; I _O = -6 mA	-	-	-	-	-	V
V _{OL}	LOW-level output voltage	RTC output; RS = V _{CC} and MR = GND						
		V _{CC} = 1.2 V; I _O = -3.4 mA	-	-	-	-	-	V
		V _{CC} = 2.0 V; I _O = -3.4 mA	-	-	-	-	-	V
		V _{CC} = 2.7 V; I _O = -3.4 mA	-	-	-	-	-	V
		V _{CC} = 3.0 V; I _O = -3.4 mA	-	0.25	0.40	-	0.50	V
		V _{CC} = 4.5 V; I _O = -3.4 mA	-	-	-	-	-	V

Table 5. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{OL}	LOW-level output voltage	RTC output; RS = V _{CC} and MR = GND;						
		V _{CC} = 1.2 V; I _O = –100 µA	-	0	0.2	-	0.2	V
		V _{CC} = 2.0 V; I _O = –100 µA	-	0	0.2	-	0.2	V
		V _{CC} = 2.7 V; I _O = –100 µA	-	-	-	-	-	V
		V _{CC} = 3.0 V; I _O = –100 µA	-	0	0.2	-	0.2	V
		V _{CC} = 4.5 V; I _O = –100 µA	-	-	-	-	-	V
		CTC output; RS = V _{IH} and MR = V _{IL} ;						
		V _{CC} = 1.2 V; I _O = –3.8 mA	-	-	-	-	-	V
		V _{CC} = 2.0 V; I _O = –3.8 mA	-	-	-	-	-	V
		V _{CC} = 2.7 V; I _O = –3.8 mA	-	-	-	-	-	V
		V _{CC} = 3.0 V; I _O = –3.8 mA	-	0.25	-	0.40	0.50	V
		V _{CC} = 4.5 V; I _O = –3.8 mA	-	-	-	-	-	V
		except RTC output; V _I = V _{IH} or V _{IL} ;						
		V _{CC} = 1.2 V; I _O = –100 µA	-	0	0.2	-	0.2	V
		V _{CC} = 2.0 V; I _O = –100 µA	-	0	0.2	-	0.2	V
		V _{CC} = 2.7 V; I _O = –100 µA	-	-	-	-	-	V
		V _{CC} = 3.0 V; I _O = –100 µA	-	0	0.2	-	0.2	V
		V _{CC} = 4.5 V; I _O = –100 µA	-	-	-	-	-	V
		except RTC and CTC output; V _I = V _{IH} or V _{IL} ;						
		V _{CC} = 1.2 V; I _O = –6 mA	-	-	-	-	-	V
		V _{CC} = 2.0 V; I _O = –6 mA	-	-	-	-	-	V
		V _{CC} = 2.7 V; I _O = –6 mA	-	0.25	0.40	-	0.50	V
		V _{CC} = 3.0 V; I _O = –6 mA	-	-	-	-	-	V
		V _{CC} = 4.5 V; I _O = –6 mA	-	-	-	-	-	V
I _I	input leakage current	V _{CC} = 5.5 V; V _I = V _{CC} or GND	-	-	1.0	-	1.0	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	-	20	-	160	µA
		V _{CC} = 5.5 V; V _I = V _{CC} or GND; I _O = 0 A	-	-	-	-	80	µA
ΔI _{CC}	additional supply current	V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} – 0.6 V; I _O = 0 A	-	-	500	-	850	µA
C _I	input capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 6. Dynamic characteristics

$GND = 0\text{ V}$; for test circuit, see [Figure 10](#).

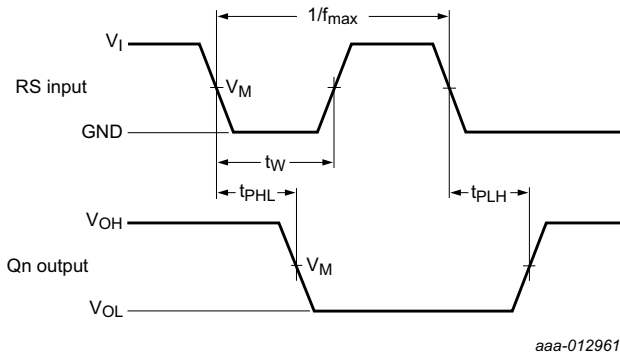
Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	RS to Q3; see Figure 7 and Figure 9 ^[2]						
		$V_{CC} = 1.2\text{ V}$	-	180	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	52	84	-	105	ns
		$V_{CC} = 2.7\text{ V}$	-	42	66	-	83	ns
		$V_{CC} = 3.3\text{ V}$; $C_L = 15\text{ pF}$	-	29	-	-	-	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V ^[3]	-	33	53	-	66	ns
		$V_{CC} = 4.5\text{ V}$ to 5.5 V ^[4]	-	24	39	-	49	ns
		Qn to Qn+1; see Figure 8 and Figure 9						
		$V_{CC} = 1.2\text{ V}$	-	40	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	14	23	-	29	ns
		$V_{CC} = 2.7\text{ V}$	-	10	16	-	20	ns
		$V_{CC} = 3.3\text{ V}$; $C_L = 15\text{ pF}$	-	6	-	-	-	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V ^[3]	-	8	13	-	16	ns
		$V_{CC} = 4.5\text{ V}$ to 5.5 V ^[4]	-	6	9	-	11	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Figure 8 and Figure 9						
		$V_{CC} = 1.2\text{ V}$	-	100	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	29	46	-	58	ns
		$V_{CC} = 2.7\text{ V}$	-	24	39	-	49	ns
		$V_{CC} = 3.3\text{ V}$; $C_L = 15\text{ pF}$	-	16	-	-	-	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V ^[3]	-	19	31	-	39	ns
		$V_{CC} = 4.5\text{ V}$ to 5.5 V ^[4]	-	14	23	-	29	ns
t_w	pulse width	RS HIGH or LOW; see Figure 7						
		$V_{CC} = 2.0\text{ V}$	34	9	-	38	-	ns
		$V_{CC} = 2.7\text{ V}$	25	6	-	30	-	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V ^[3]	20	5	-	24	-	ns
		$V_{CC} = 4.5\text{ V}$ to 5.5 V ^[4]	16	4	-	20	-	ns
		MR HIGH; see Figure 9						
		$V_{CC} = 2.0\text{ V}$	34	10	-	38	-	ns
		$V_{CC} = 2.7\text{ V}$	25	8	-	30	-	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V ^[3]	20	6	-	24	-	ns
		$V_{CC} = 4.5\text{ V}$ to 5.5 V ^[4]	16	4	-	20	-	ns

Table 6. Dynamic characteristicsGND = 0 V; for test circuit, see [Figure 10](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{rec}	recovery time	MR to RS; see Figure 9						
		V _{CC} = 2.0 V	29	18	-	37	-	ns
		V _{CC} = 2.7 V	26	16	-	32	-	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	18	11	-	23	-	ns
		V _{CC} = 4.5 V to 5.5 V ^[4]	12	7	-	15	-	ns
f _{max}	maximum frequency	see Figure 7						
		V _{CC} = 2.0 V	14	40	-	9	-	MHz
		V _{CC} = 2.7 V	19	70	-	12	-	MHz
		V _{CC} = 3.3 V; C _L = 15 pF	-	99	-	-	-	MHz
		V _{CC} = 3.0 V to 3.6 V ^[3]	24	90	-	15	-	MHz
		V _{CC} = 4.5 V to 5.5 V ^[4]	30	100	-	19	-	MHz
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ^[5]	-	40	-	-	-	pF

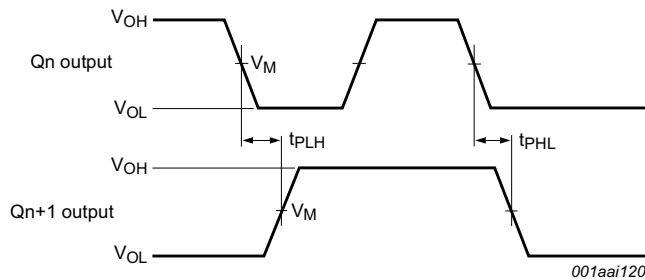
- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] Typical value measured at V_{CC} = 3.3 V.
- [4] Typical value measured at V_{CC} = 5.0 V.
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



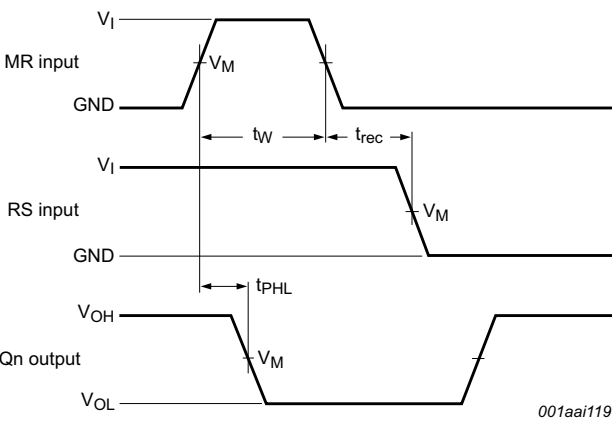
Measurement points are given in [Table 7](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Waveforms showing the clock (RS) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum frequency



Measurement points are given in [Table 7](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Waveforms showing the output Qn to output Qn+1 propagation delays

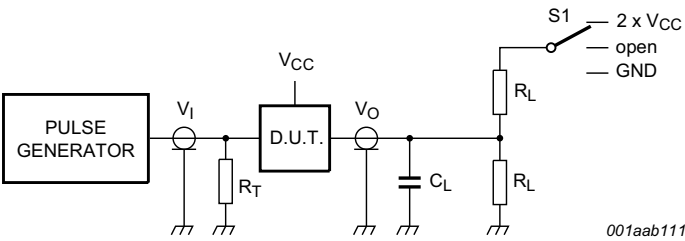


Measurement points are given in [Table 7](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Waveforms showing the master reset (MR) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (RS) recovery time

Table 7. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in [Table 8](#).
Definitions test circuit:
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 C_L = Load capacitance including jig and probe capacitance.
 R_L = Load resistance.

Fig 10. Test circuit for measuring switching times

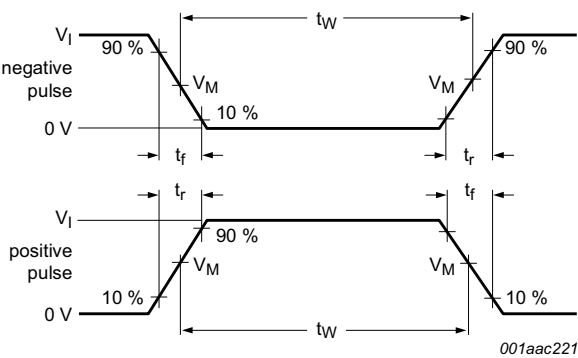
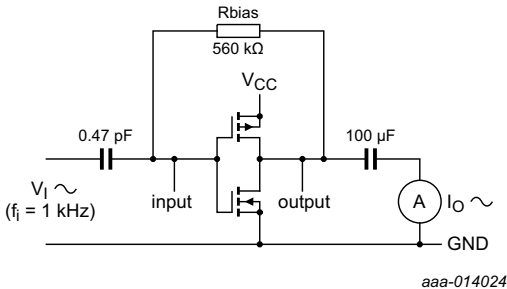


Fig 11. Input pulse definition

Table 8. Test data

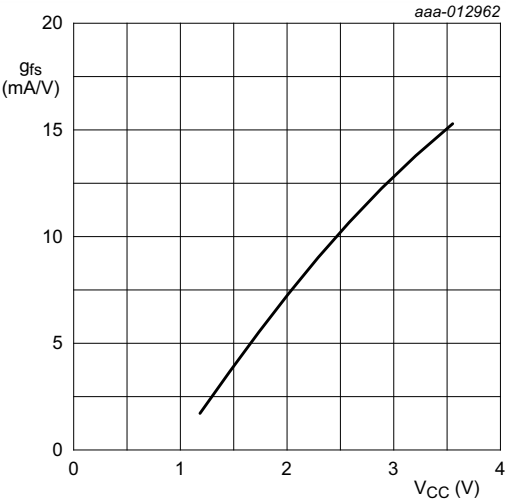
Supply voltage	Input		Load		S1
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}
$V_{CC} < 2.7\text{ V}$	V_{CC}	2.5 ns	50 pF	1 kΩ	open
$2.7\text{ V} < V_{CC} < 3.6\text{ V}$	2.7 V	2.5 ns	15 pF, 50 pF	1 kΩ	open
$V_{CC} \geq 4.5\text{ V}$	V_{CC}	2.5 ns	50 pF	1 kΩ	open

13. Typical forward transconductance



$g_{fs} = \Delta I_O / \Delta V_I$ at V_O is constant; MR = LOW.
See [Figure 13](#).

Fig 12. Test setup for measuring forward transconductance



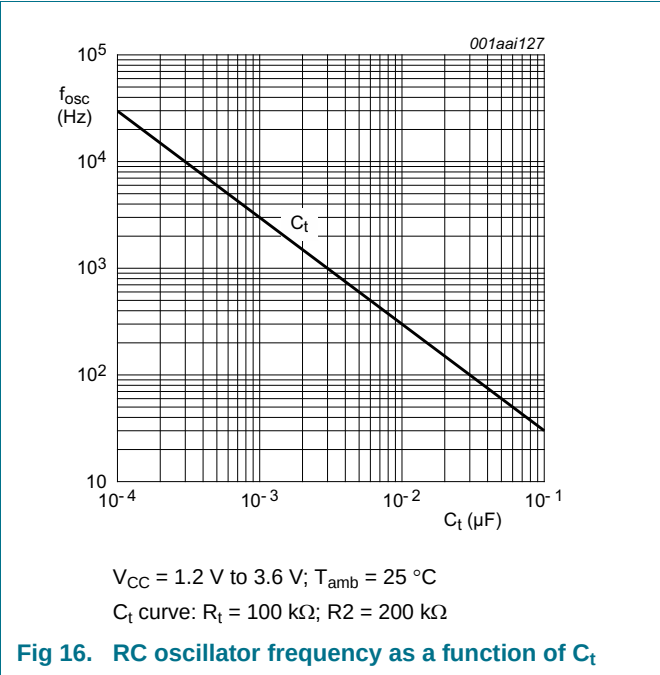
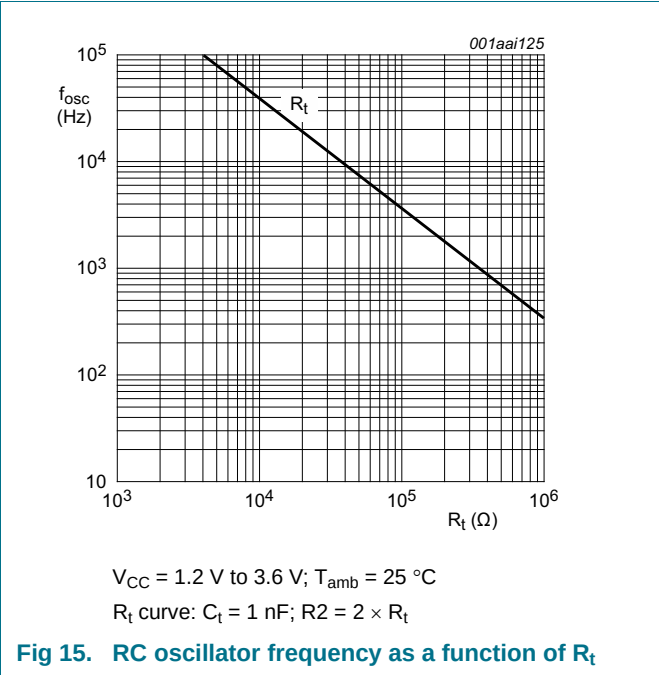
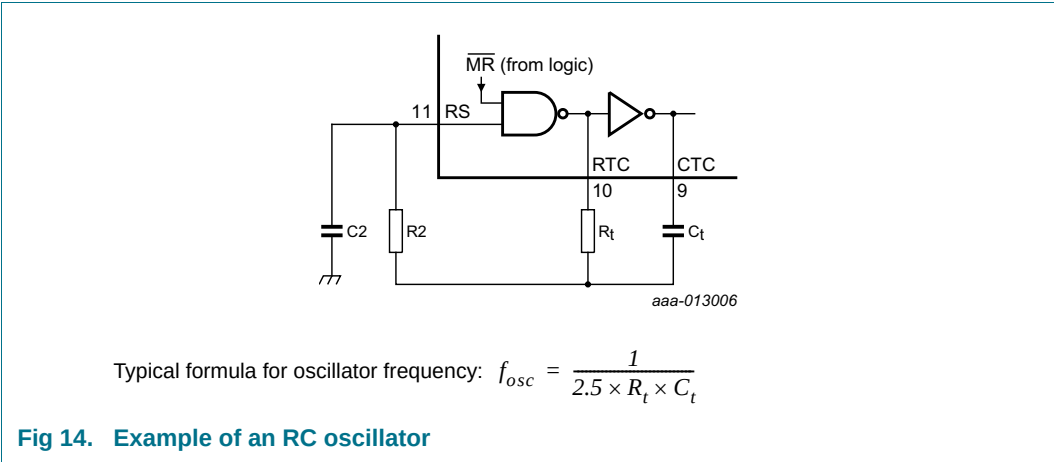
$T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig 13. Typical forward transconductance as function of the supply voltage

14. RC oscillator

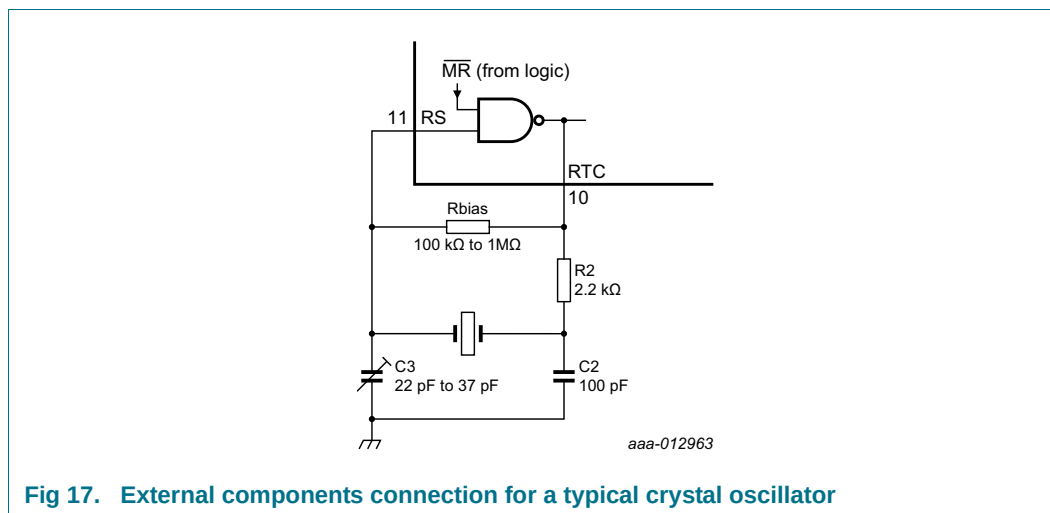
14.1 Timing component limitations

The oscillator frequency is mainly determined by $R_t \times C_t$, provided $R_2 \approx 2R_t$ and $R_2 \times C_2$ is much less than $R_t \times C_t$. The function of R_2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C_2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the 'ON' resistance in series with it, which typically is 280 Ω at $V_{CC} = 1.2$ V, 130 Ω at $V_{CC} = 2.0$ V and 100 Ω at $V_{CC} = 3.0$ V. The recommended values for these components to maintain agreement with the typical oscillation formula are: $C_t > 50$ pF, up to any practical value, $10\text{ k}\Omega < R_t < 1\text{ M}\Omega$. In order to avoid start-up problems, $R_t \geq 1\text{ k}\Omega$.



14.2 Typical crystal oscillator circuit

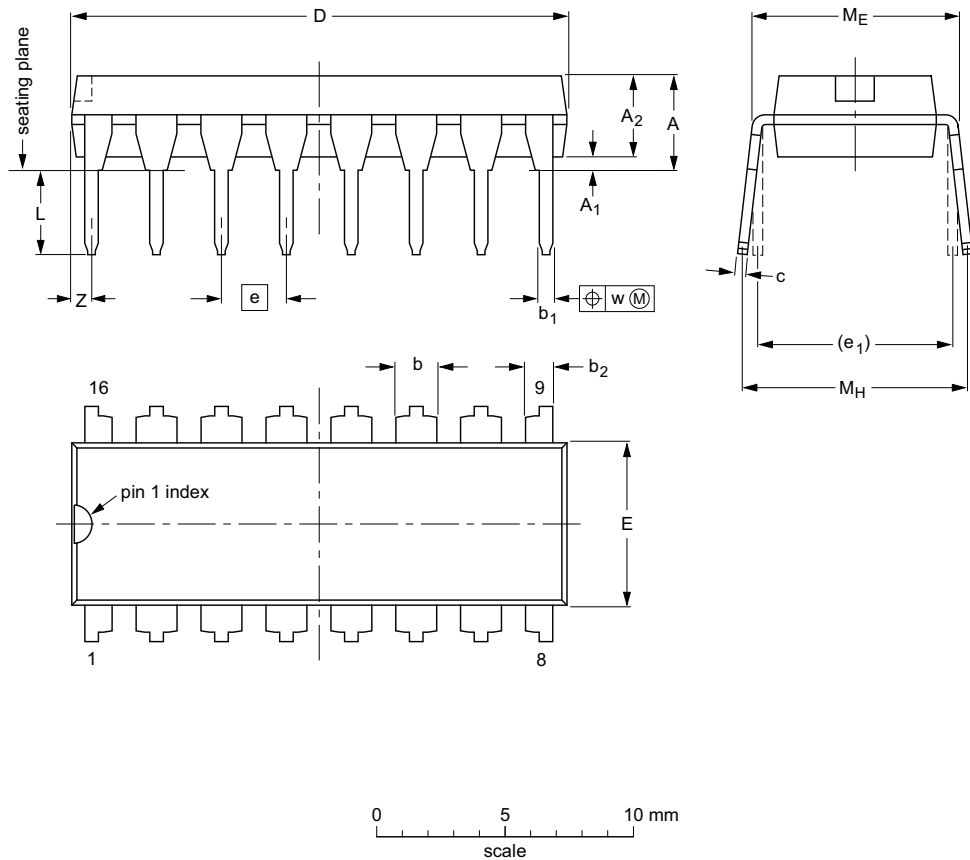
In [Figure 17](#), R2 is the power limiting resistor. For starting and maintaining oscillation, a minimum transconductance is necessary, so R2 must not be too large. A practical value for R2 is 2.2 k Ω .



15. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

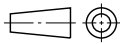
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						95-01-14 03-02-13

Fig 18. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

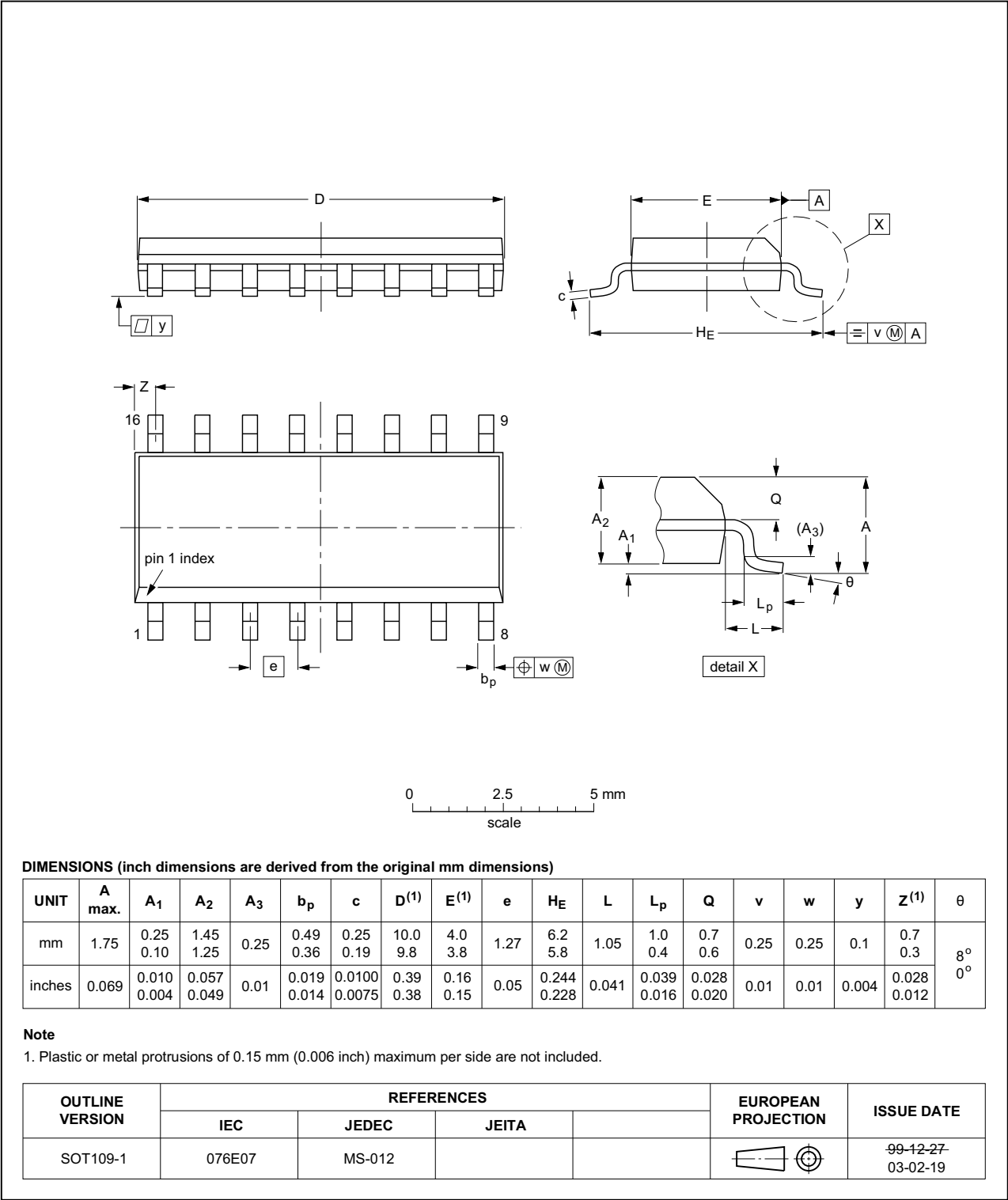


Fig 19. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

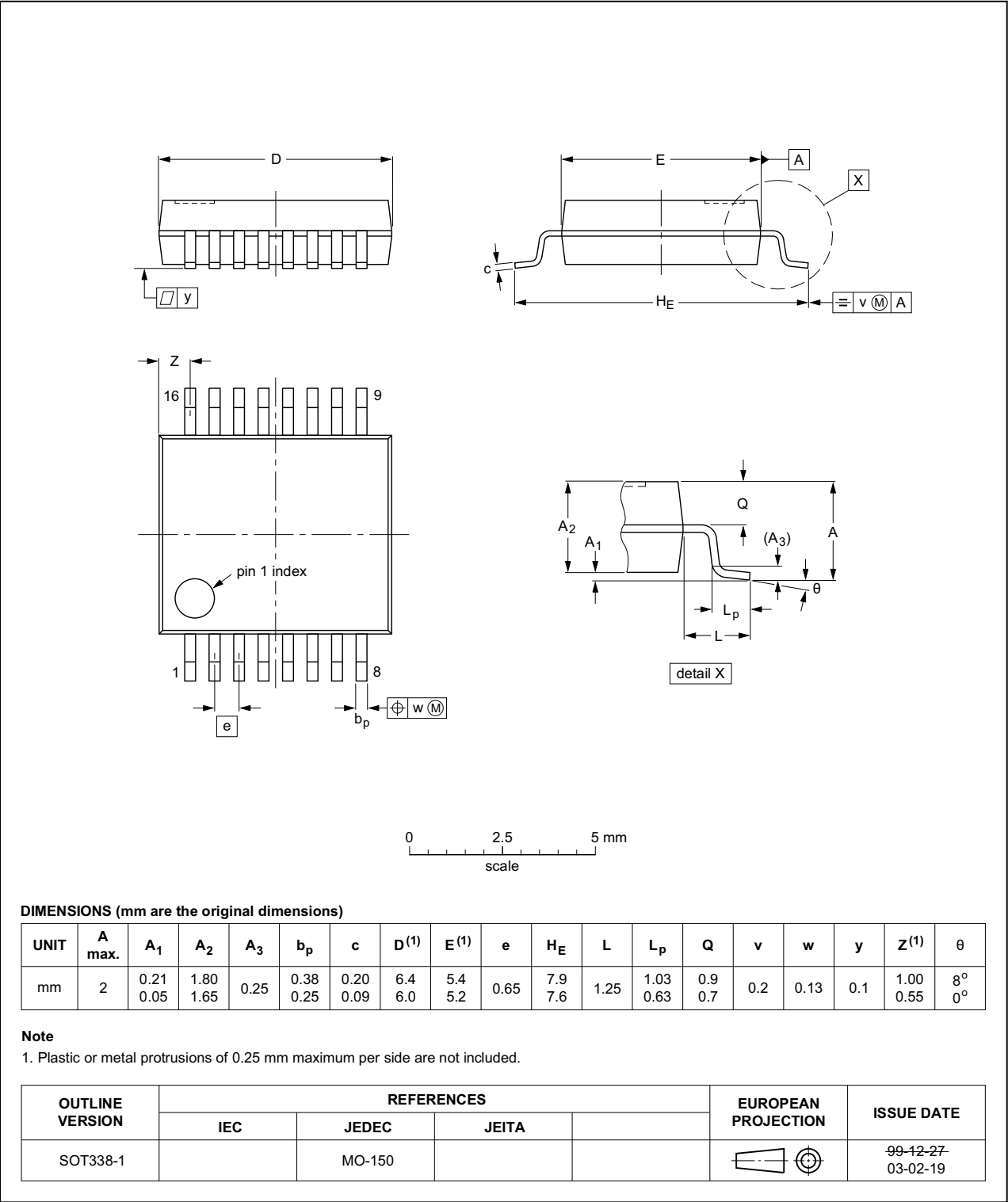


Fig 20. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

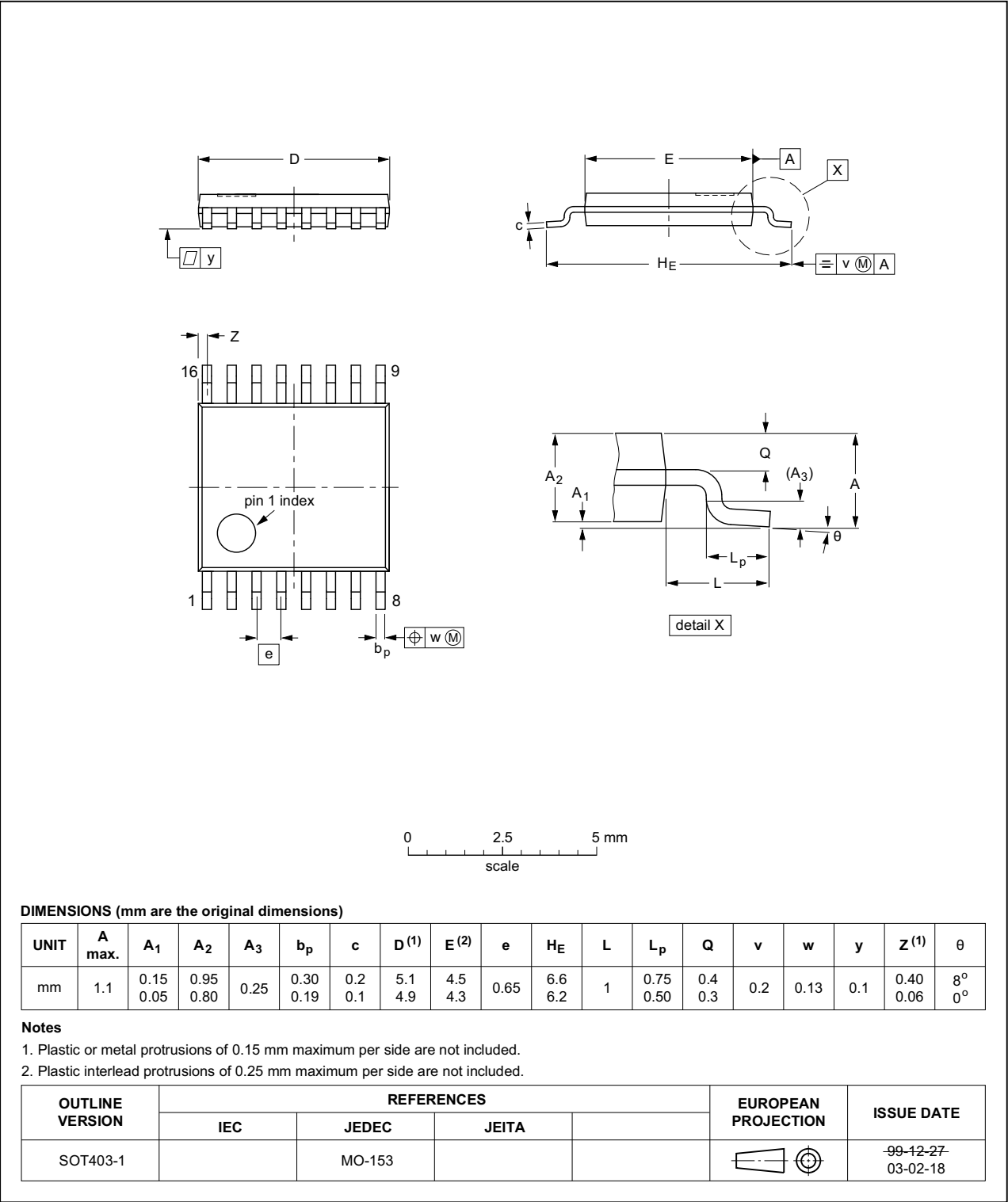


Fig 21. Package outline SOT403-1 (TSSOP16)

16. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

17. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4060 v.3	20140728	Product data sheet	-	74LV4060 v.2
Modifications:	Minimum value V_{OH} and V_{OL} corrected (errata).			
74LV4060 v.2	20140703	Product data sheet	-	74LV4060 v.1
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate.			
74LV4060 v.1	19980623	Product specification	-	-

18. Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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20. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Ordering information	2
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	4
7	Functional description	4
8	Limiting values	5
9	Recommended operating conditions	5
10	Static characteristics	6
11	Dynamic characteristics	9
12	Waveforms	11
13	Typical forward transconductance	13
14	RC oscillator	14
14.1	Timing component limitations	14
14.2	Typical crystal oscillator circuit	15
15	Package outline	16
16	Abbreviations	20
17	Revision history	20
18	Legal information	21
18.1	Data sheet status	21
18.2	Definitions	21
18.3	Disclaimers	21
18.4	Trademarks	22
19	Contact information	22
20	Contents	23

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