

74LVC04A

Hex inverter

Rev. 8 — 26 September 2011

Product data sheet

1. General description

The 74LVC04A provides six inverting buffers. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

2. Features and benefits

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40°C to $+85^{\circ}\text{C}$ and -40°C to $+125^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC04AD	-40°C to $+125^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC04ADB	-40°C to $+125^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVC04APW	-40°C to $+125^{\circ}\text{C}$	TSSOP14	plastic thin shrink outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC04ABQ	-40°C to $+125^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1

4. Functional diagram

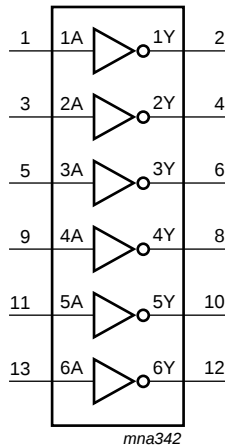


Fig 1. Logic symbol

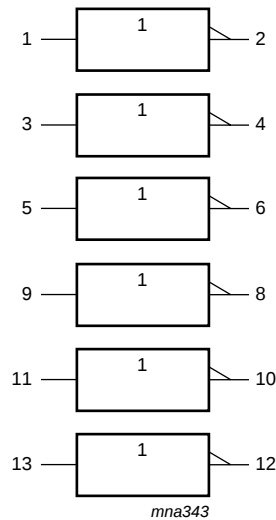


Fig 2. IEC logic symbol

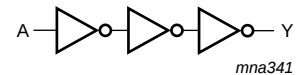


Fig 3. Logic diagram for one gate

5. Pinning information

5.1 Pinning

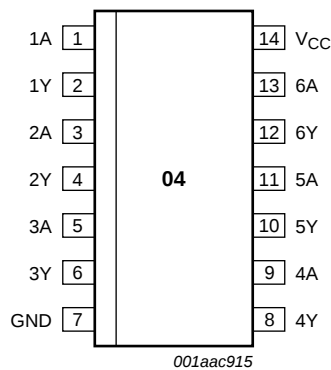


Fig 4. Pin configuration SO14 and (T)SSOP14

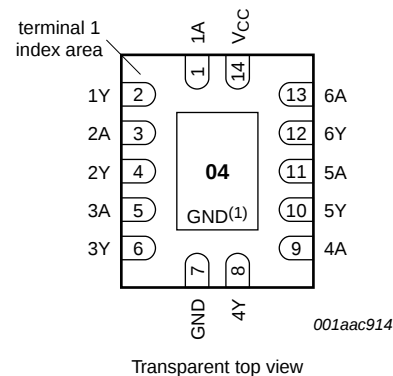


Fig 5. Pin configuration DHVQFN14

- (1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table^[1]

Input nA	Output nY
L	H
H	L

[1] H = HIGH voltage level; L = LOW voltage level

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		−0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0	−50	-	mA
V _I	input voltage		^[1] −0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0	-	±50	mA
V _O	output voltage		^[2] −0.5	V _{CC} + 0.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		−100	-	mA
T _{stg}	storage temperature		−65	+150	°C
P _{tot}	total power dissipation	T _{amb} = −40 °C to +125 °C	^[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.

For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ⁽¹⁾	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μA

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I_{CC}	supply current	$V_{CC} = 3.6 \text{ V}$; $V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$	-	0.1	10	-	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 1.65 \text{ V}$ to 3.6 V ; $V_I = V_{CC} - 0.6 \text{ V}$; $I_O = 0 \text{ A}$	-	5	500	-	5000	μA
C_i	input capacitance	$V_{CC} = 0 \text{ V}$ to 3.6 V ; $V_I = \text{GND}$ to V_{CC}	-	4.0	-	-	-	pF

[1] All typical values are measured at $V_{CC} = 3.3 \text{ V}$ (unless stated otherwise) and $T_{amb} = 25 \text{ °C}$.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Figure 6 ^[2]						
		$V_{CC} = 1.2 \text{ V}$	-	14	-	-	-	ns
		$V_{CC} = 1.65 \text{ V}$ to 1.95 V	0.3	3.7	8.8	0.3	10.2	ns
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	0.5	2.2	5.0	0.5	5.8	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	2.1	5.5	1.0	7.0	ns
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	1.0	2.0	4.5	1.0	6.0	ns
$t_{sk(o)}$	output skew time	$V_{CC} = 3.0 \text{ V}$ to 3.6 V ^[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per buffer; $V_I = \text{GND}$ to V_{CC} ^[4]						
		$V_{CC} = 1.65 \text{ V}$ to 1.95 V	-	3.9	-	-	-	pF
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	-	7.1	-	-	-	pF
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	-	9.9	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25 \text{ °C}$ and $V_{CC} = 1.2 \text{ V}$, 1.8 V , 2.5 V , 2.7 V , and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

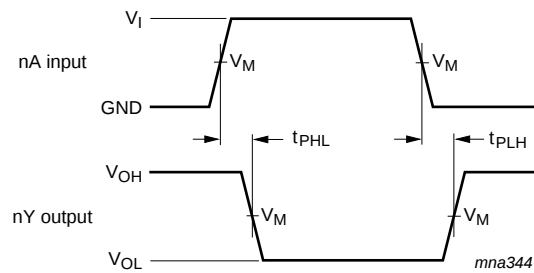
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

11. Waveforms

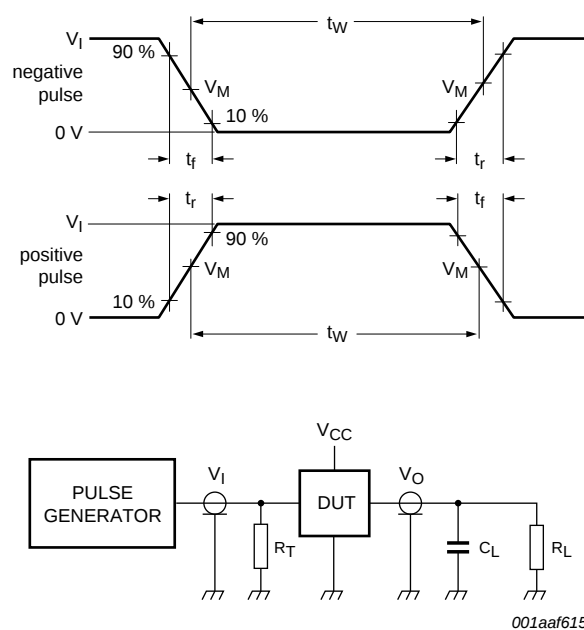


$V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. The input (nA) to output (nY) propagation delays



Test data is given in [Table 8](#).

Definitions for test circuit:

R_L = Load resistance

C_L = Load capacitance including jig and probe capacitance

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 7. Load circuitry for measuring switching times

Table 8. Test data

Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

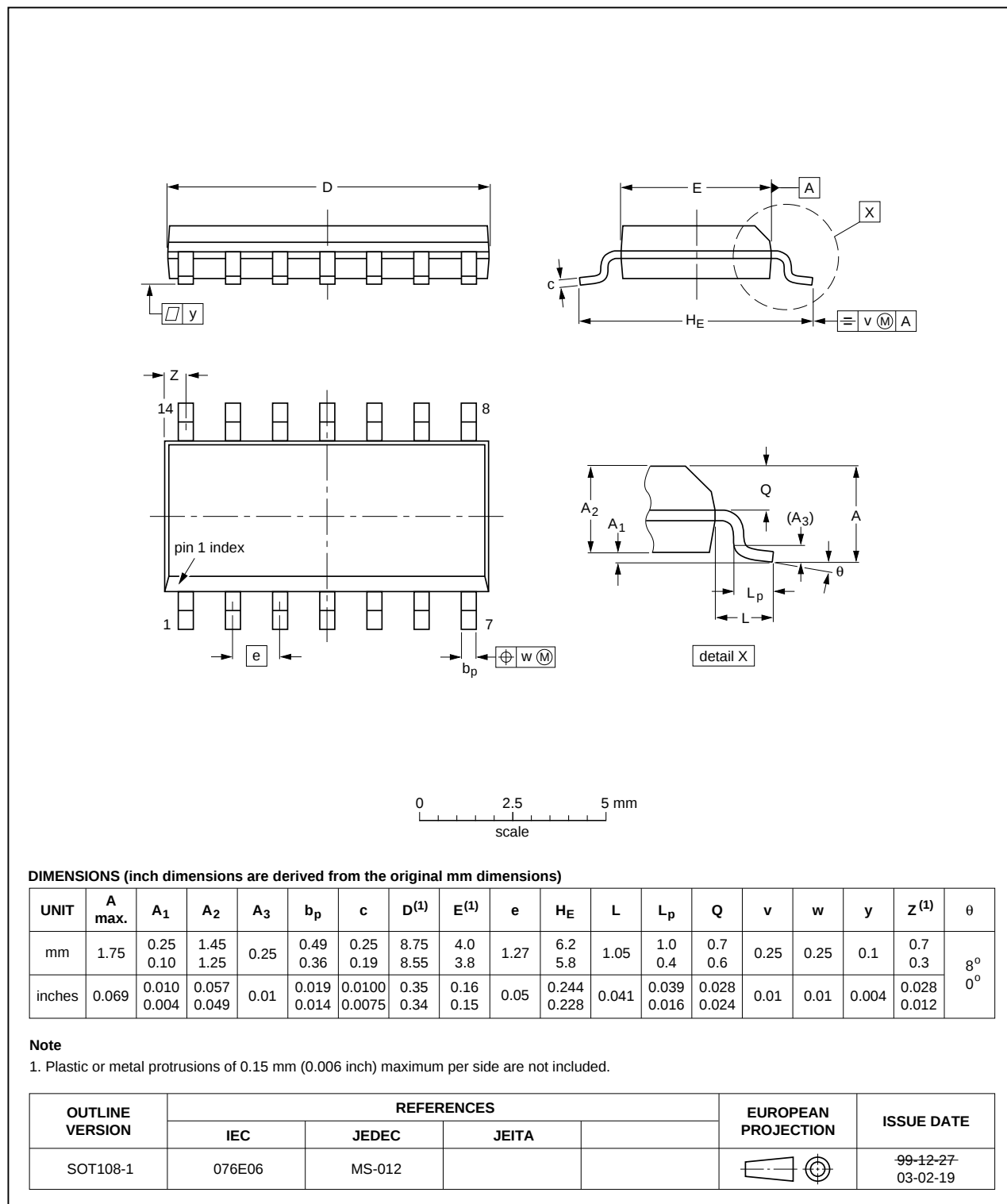


Fig 8. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

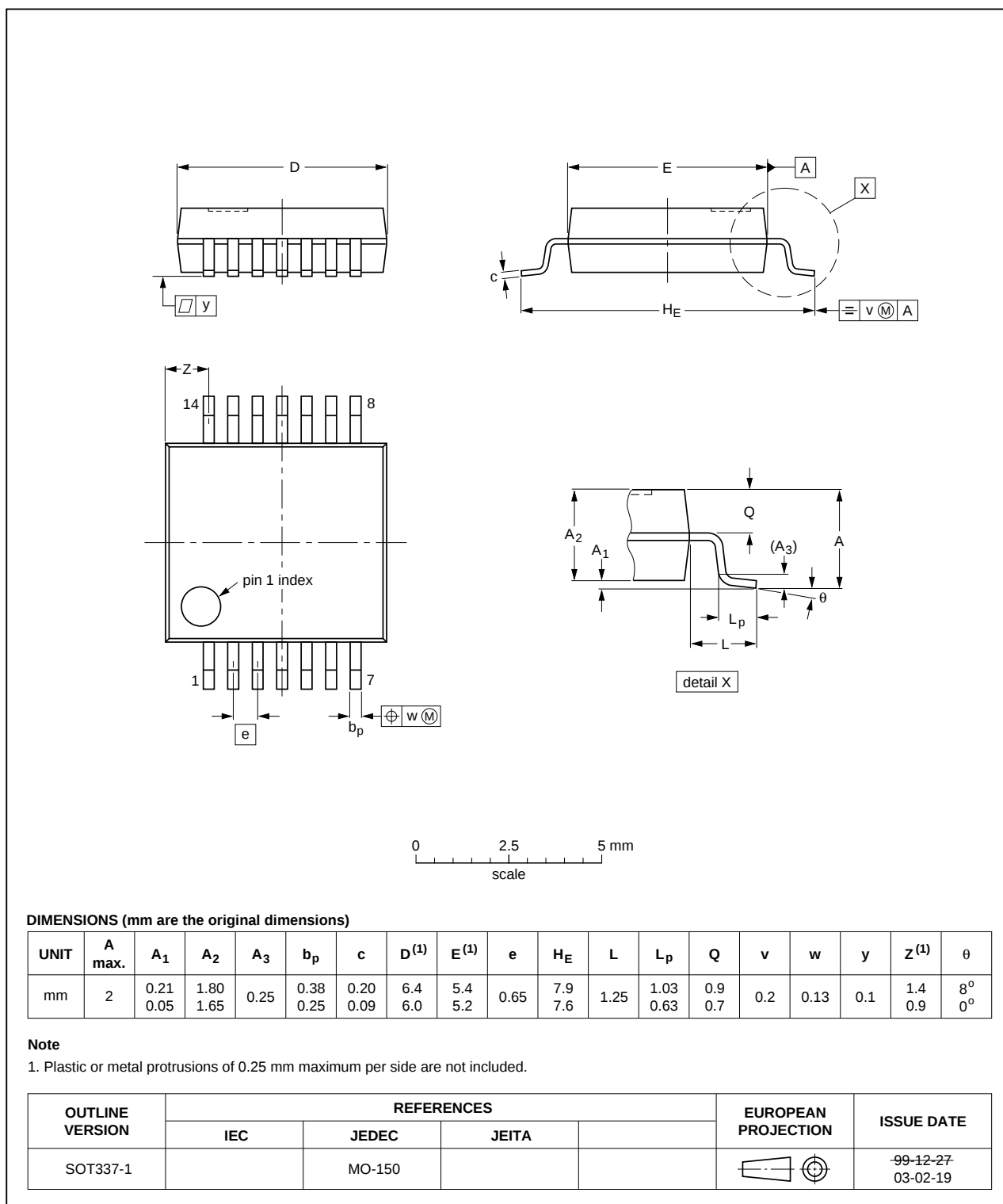
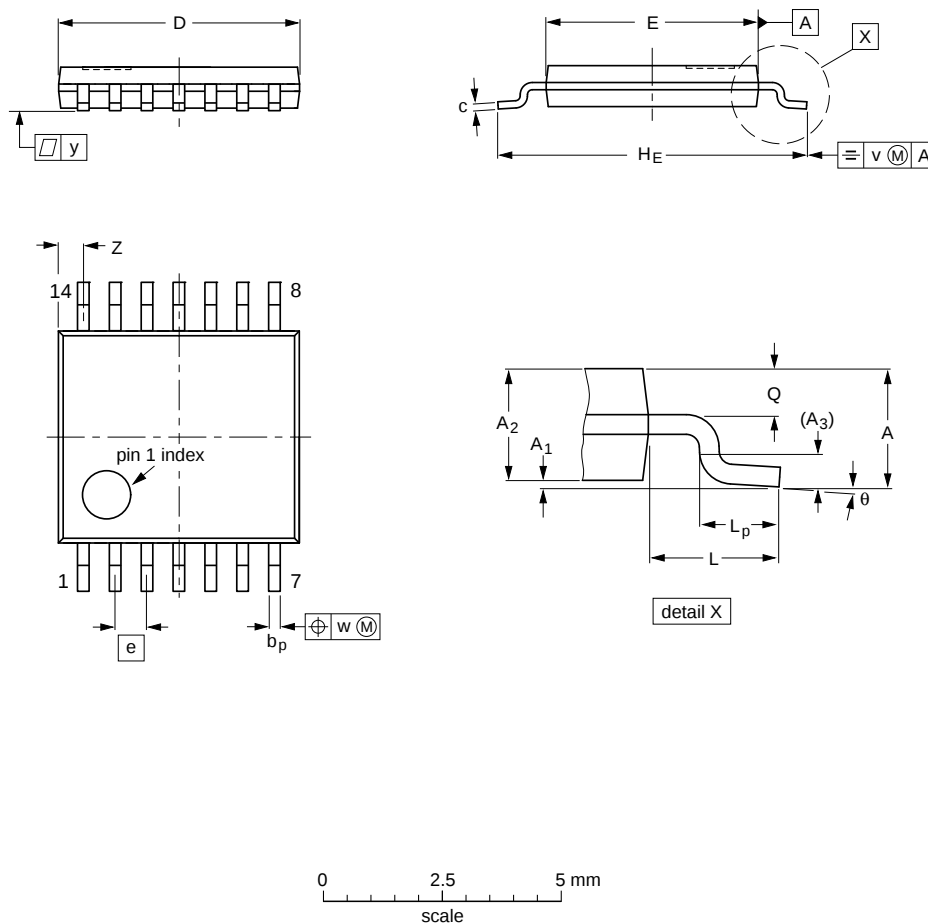


Fig 9. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				99-12-27 03-02-18

Fig 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

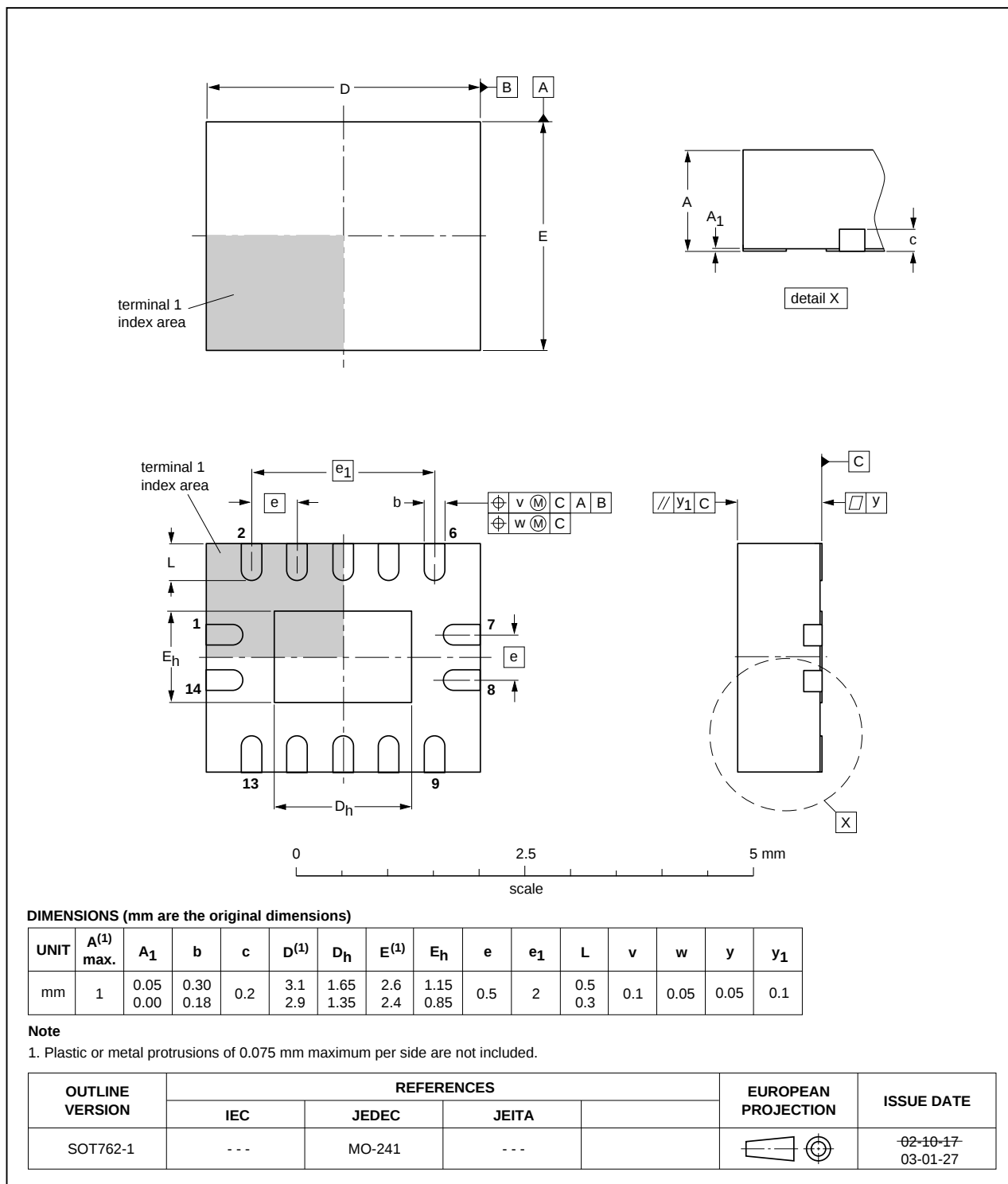


Fig 11. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC04A v.8	20110926	Product data sheet	-	74LVC04A v.7
Modifications:	• Table 4 , Table 5 , Table 6 , Table 7 , and Table 8 : values added for lower voltage ranges.			
74LVC04A v.7	20110201	Product data sheet	-	74LVC04A v.6
74LVC04A v.6	20030904	Product specification	-	74LVC04A v.5
74LVC04A v.5	20030224	Product specification	-	74LVC04A v.4
74LVC04A v.4	20020308	Product specification	-	74LVC04A v.3
74LVC04A v.3	19970630	Product specification	-	74LVC04A v.2
74LVC04A v.2	19970630	Product specification	-	74LVC04A v.1
74LVC04A v.1	19970203	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 26 September 2011

Document identifier: 74LVC04A



74LVC04A



Hex inverter

Products / Packages

Type number	Orderable part number	Ordering code (12NC)	Product status	Package	Packing	Marking	ECCN
74LVC04ABQ	74LVC04ABQ,115	9352 736 75115	Volume production	SOT762-1 (DHVQFN14)	Reel Pack, SMD, 7"	Standard Marking	
74LVC04AD	74LVC04AD,112	9352 424 00112	Volume production	SOT108-1 (SO14)	Tube	Standard Marking	
74LVC04AD	74LVC04AD,118	9352 424 00118	Volume production	SOT108-1 (SO14)	Reel Pack, SMD, 13"	Standard Marking	
74LVC04ADB	74LVC04ADB,112	9352 424 10112	Volume production	SOT337-1 (SSOP14)	Tube	Standard Marking	
74LVC04ADB	74LVC04ADB,118	9352 424 10118	Volume production	SOT337-1 (SSOP14)	Reel Pack, SMD, 13"	Standard Marking	
74LVC04APW	74LVC04APW,112	9352 424 20112	Volume production	SOT402-1 (TSSOP14)	Tube	Standard Marking	
74LVC04APW	74LVC04APW,118	9352 424 20118	Volume production	SOT402-1 (TSSOP14)	Reel Pack, SMD, 13"	Standard Marking	

The variants in the table below are discontinued. See the table [Discontinuation information](#) at the bottom of this page for more information.

Type number	Orderable part number	Ordering code (12NC)	Product status	Package	Packing	Marking	ECCN
74LVC04AD/N	74LVC04AD/N,118	9352 770 11118	Withdrawn Replacement product	SOT108-1 (SO14)	Reel Pack, SMD, 13"	Standard Marking	

Discontinuation information

Type number	Ordering code (12NC)	Last-time buy date	Last-time delivery date	Replacement product	DN Notice	Status	Comments
74LVC04AD/N	935277011118				DN		