

74LVC2952A

Octal registered transceiver with 5 V tolerant inputs/outputs;
3-state

Rev. 02 — 29 June 2004

Product data sheet

1. General description

The 74LVC2952A is a high-performance, low power, low voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 V and 5 V environment.

The 74LVC2952A is an octal non-inverting registered transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the clock (CPAB, CPBA) provided that the clock enable ($\overline{\text{CEAB}}$, $\overline{\text{CEBA}}$) input is LOW. The data is then present at the 3-state output buffers, but is only accessible when the output enable ($\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$) input is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

2. Features

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Flow-through pin-out architecture
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
 - ◆ HBM EIA/JESD22-A114-B exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$.

PHILIPS

3. Quick reference data

Table 1: Quick reference data

$GND = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $t_r = t_f \leq 2.5\text{ ns}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL} , t_{PLH}	propagation delay CPAB, CPBA to An, Bn	$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	-	3.6	-	ns
f_{max}	maximum clock frequency	$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	-	250	-	MHz
C_I	input capacitance		-	5.0	-	pF
$C_{I/O}$	input/output capacitance		-	10.0	-	pF
C_{PD}	power dissipation capacitance per latch	outputs enabled; $V_{CC} = 3.3\text{ V}$	[1] [2]	15.0	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is $V_I = GND$ to V_{CC} .

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC2952AD	-40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVC2952ADB	-40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74LVC2952APW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1



5. Functional diagram

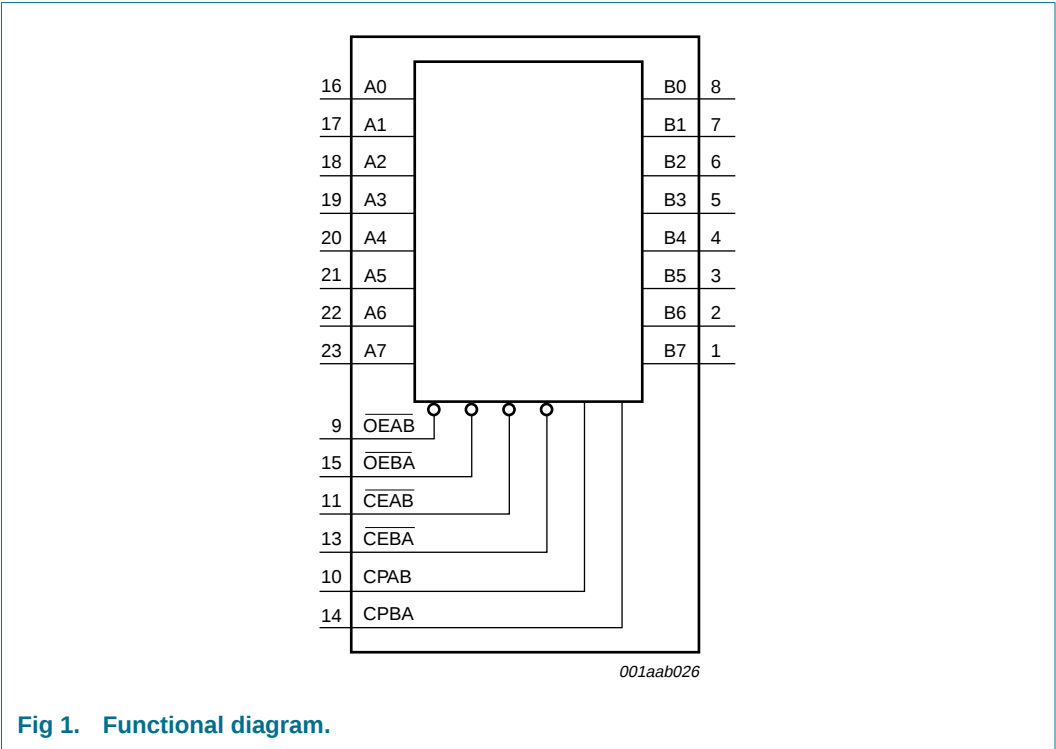




Fig 3. IEC logic symbol.



6.1 Pinning



9397 750 13251

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
B7	1	B data input/output
B6	2	B data input/output
B5	3	B data input/output
B4	4	B data input/output
B3	5	B data input/output
B2	6	B data input/output
B1	7	B data input/output
B0	8	B data input/output
$\overline{\text{OEAB}}$	9	A to B output enable input (active LOW)
CPAB	10	A to B clock input (LOW-to-HIGH, edge-triggered)
$\overline{\text{CEAB}}$	11	A to B clock enable input (active LOW)
GND	12	ground (0 V)
$\overline{\text{CEBA}}$	13	B to A clock enable input (active LOW)
CPBA	14	B to A clock input (LOW-to-HIGH, edge-triggered)
$\overline{\text{OEBA}}$	15	B to A output enable input (active LOW)
A0	16	A data input/output
A1	17	A data input/output
A2	18	A data input/output
A3	19	A data input/output
A4	20	A data input/output
A5	21	A data input/output
A6	22	A data input/output
A7	23	A data input/output
V _{CC}	24	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table for register An or Bn ^[1]

Operating mode	Input			Internal latch
	An or Bn	CPxx	CExx	
Hold data	X	X	H	NC
Load data	L	↑	L	L
Load data	H	↑	L	H

Table 5: Function table for output enable ^[1]

Operating mode	Input OE _{xx}	Internal latch	Output An or Bn
Disable outputs	H	X	Z
Enable outputs	L	L	L
Enable outputs	L	H	H

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 Z = high-impedance OFF-state;
 NC = no change;
 X = don't care;
 ↑ = LOW-to-HIGH level transition.

8. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input diode current	V _I < 0 V	-	-50	mA
V _I	input voltage		^[1] -0.5	+6.5	V
I _{OK}	output diode current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	output HIGH or LOW state	^[1] -0.5	V _{CC} + 0.5	V
		output 3-state	^[1] -0.5	+6.5	V
I _O	output source or sink current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC} , I _{GND}	V _{CC} or GND current		-	±100	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	power dissipation	T _{amb} = -40 °C to +125 °C	^[2] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

- [2] For SO24 packages: above 70 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For T(SSOP)24 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

9. Recommended operating conditions

Table 7: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	2.7	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	operating ambient temperature	in free air	-40	-	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 1.2 \text{ V to } 2.7 \text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	-	10	ns/V

10. Static characteristics

Table 8: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40 \text{ °C to } +85 \text{ °C}$ [1]						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.2 \text{ V}$	V_{CC}	-	-	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.2 \text{ V}$	-	-	GND	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = -100 \text{ }\mu\text{A}; V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ [2]	$V_{CC} - 0.2$	V_{CC}	-	V
		$I_O = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	$V_{CC} - 0.5$	-	-	V
		$I_O = -18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	$V_{CC} - 0.6$	-	-	V
		$I_O = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	$V_{CC} - 0.8$	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = 100 \text{ }\mu\text{A}; V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ [2]	-	GND	0.2	V
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.4	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	V
I_{LI}	input leakage current	$V_I = 5.5 \text{ V or GND}; V_{CC} = 3.6 \text{ V}$	-	± 0.1	± 5	μA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH} \text{ or } V_{IL}; V_O = 5.5 \text{ V or GND}; V_{CC} = 3.6 \text{ V}$ [3]	-	0.1	± 10	μA
I_{off}	power-off leakage current	$V_I \text{ or } V_O = 5.5 \text{ V}; V_{CC} = 0 \text{ V}$	-	0.1	± 10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC} \text{ or GND}; I_O = 0 \text{ A}; V_{CC} = 3.6 \text{ V}$	-	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ [2]	-	5	500	μA
C_I	input capacitance		-	5.0	-	pF
$C_{I/O}$	input/output capacitance		-	10.0	-	pF

Table 8: Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	V _{CC}	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = –100 µA; V _{CC} = 2.7 V to 3.6 V	V _{CC} – 0.3	-	-	V
		I _O = –12 mA; V _{CC} = 2.7 V	V _{CC} – 0.65	-	-	V
		I _O = –18 mA; V _{CC} = 3.0 V	V _{CC} – 0.75	-	-	V
		I _O = –24 mA; V _{CC} = 3.0 V	V _{CC} – 1	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 µA; V _{CC} = 2.7 V to 3.6 V	-	-	0.3	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.8	V
I _{LI}	input leakage current	V _I = 5.5 V or GND; V _{CC} = 3.6 V	-	-	±20	µA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; V _{CC} = 3.6 V	[3] -	-	±20	µA
I _{off}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	-	±20	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 3.6 V	-	-	40	µA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} – 0.6 V; I _O = 0 A; V _{CC} = 2.7 V to 3.6 V	-	-	5000	µA

[1] All typical values are measured at T_{amb} = 25 °C.[2] These typical values are measured at V_{CC} = 3.3 V.[3] For transceivers, the parameter I_{OZ} includes the input leakage current.

11. Dynamic characteristics

Table 9: Dynamic characteristicsGND = 0 V; see [Figure 8](#) for test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
t _{PHL} , t _{PLH}	propagation delay CPBA, CPAB to An and Bn	see Figure 5				
		V _{CC} = 1.2 V	-	16	-	ns
		V _{CC} = 2.7 V	1.5	4.4	8.6	ns
		V _{CC} = 3.0 V to 3.6 V	[2] 1.5	3.6	7.6	ns
t _{PZH} , t _{PZL}	3-state output enable time OEBA, OEAB to An and Bn	see Figure 7				
		V _{CC} = 1.2 V	-	16	-	ns
		V _{CC} = 2.7 V	1.5	4.7	8.6	ns
		V _{CC} = 3.0 V to 3.6 V	[2] 1.0	3.9	7.6	ns

Table 9: Dynamic characteristics ...continuedGND = 0 V; see [Figure 8](#) for test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}, t_{PLZ}	3-state output disable time OEBA, OEAB to An and Bn	see Figure 7				
		$V_{CC} = 1.2 \text{ V}$	-	8	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	3.8	7.6	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2] 1.5	3.4	6.6	ns
t_W	clock pulse width HIGH or LOW CPAB or CPBA	see Figure 5				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	ns
		$V_{CC} = 2.7 \text{ V}$	3.0	1.5	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2] 3.0	1.5	-	ns
t_{su}	set-up time HIGH or LOW An, Bn to CPAB, CPBA	see Figure 6				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.7	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2] +1.3	-0.5	-	ns
	set-up time HIGH or LOW CEAB, CEBA to CPAB, CPBA	see Figure 6				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.3	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2] +1.1	-0.5	-	ns
	hold time An, Bn to CPAB, CPBA	see Figure 6				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2] 1.5	0.6	-	ns
	hold time CEAB, CEBA to CPAB, CPBA	see Figure 6				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.4	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2] +1.1	-0.6	-	ns
f_{max}	maximum clock pulse frequency	see Figure 5				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	MHz
		$V_{CC} = 2.7 \text{ V}$	150	-	-	MHz
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2] 150	250	-	MHz
$t_{sk(0)}$	skew		[3] -	-	1.0	ns
C_{PD}	power dissipation capacitance per latch	outputs enabled; $V_{CC} = 3.3 \text{ V}$	[4] [5] -	15.0	-	pF
$T_{amb} = -40 \text{ }^{\circ}\text{C to } +125 \text{ }^{\circ}\text{C}$						
t_{PHL}, t_{PLH}	propagation delay CPBA, CPAB to An, Bn	see Figure 5				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	-	11	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	-	9.5	ns
t_{PZH}, t_{PZL}	3-state output enable time OEBA, OEAB to An, Bn	see Figure 7				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	-	11	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	-	9.5	ns

Table 9: Dynamic characteristics ...continuedGND = 0 V; see [Figure 8](#) for test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}, t_{PLZ}	3-state output disable time OEBA, OEAB to An, Bn	see Figure 7				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	-	9.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	-	8.5	ns
t_W	clock pulse width HIGH or LOW CPAB or CPBA	see Figure 5				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	ns
		$V_{CC} = 2.7 \text{ V}$	3.0	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.0	-	-	ns
t_{su}	set-up time HIGH or LOW An, Bn to CPAB, CPBA	see Figure 6				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.7	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.3	-	-	ns
	set-up time HIGH or LOW CEAB, CEBA to CPAB, CPBA	see Figure 6				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.3	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.1	-	-	ns
	hold time An, Bn to CPAB, CPBA	see Figure 6				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	-	-	ns
	hold time CEAB, CEBA to CPAB, CPBA	see Figure 6				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.4	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.1	-	-	ns
f_{max}	maximum clock pulse frequency	see Figure 5				
		$V_{CC} = 1.2 \text{ V}$	-	-	-	MHz
		$V_{CC} = 2.7 \text{ V}$	150	-	-	MHz
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	150	-	-	MHz
$t_{sk(0)}$	skew	[3]	-	-	1.5	ns

[1] All typical values are measured at $T_{amb} = 25 \text{ }^{\circ}\text{C}$.[2] These typical values are measured at $V_{CC} = 3.3 \text{ V}$.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{CC} = supply voltage in V; N = total load switching outputs; $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.[5] The condition is $V_i = \text{GND to } V_{CC}$.

12. Waveforms

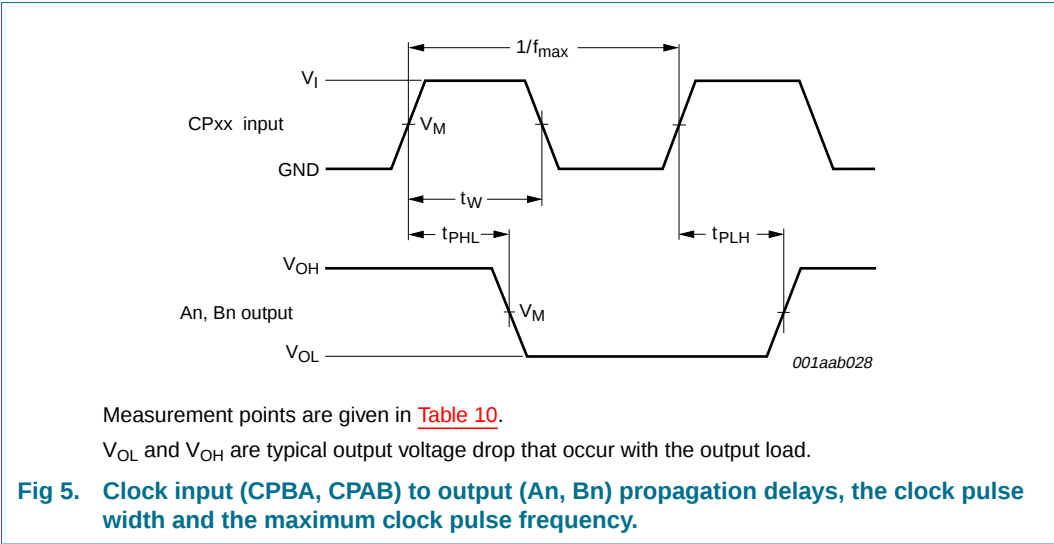


Table 10: Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
$< 2.7\text{ V}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
$\geq 2.7\text{ V}$	1.5 V	1.5 V

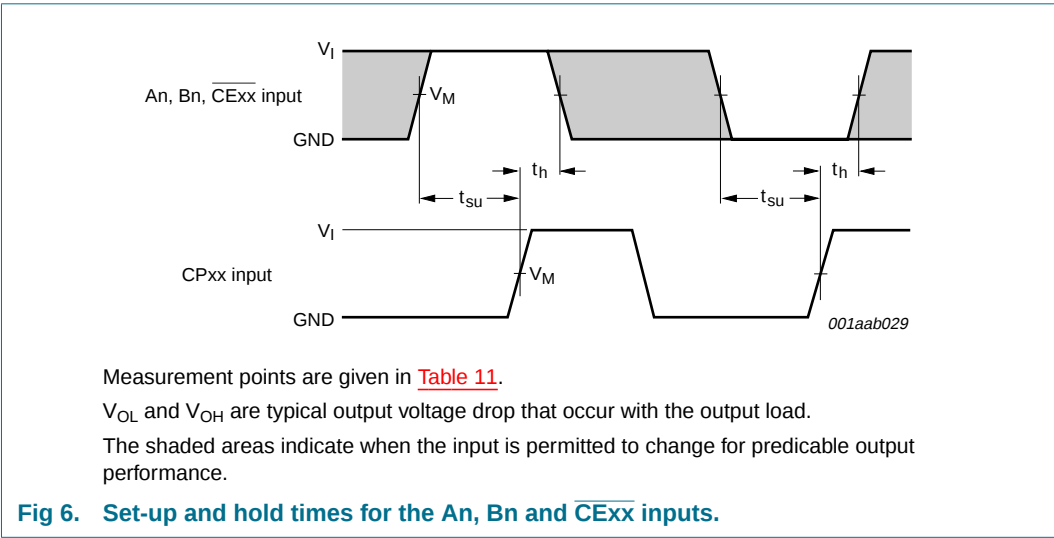


Table 11: Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
$< 2.7\text{ V}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
$\geq 2.7\text{ V}$	1.5 V	1.5 V

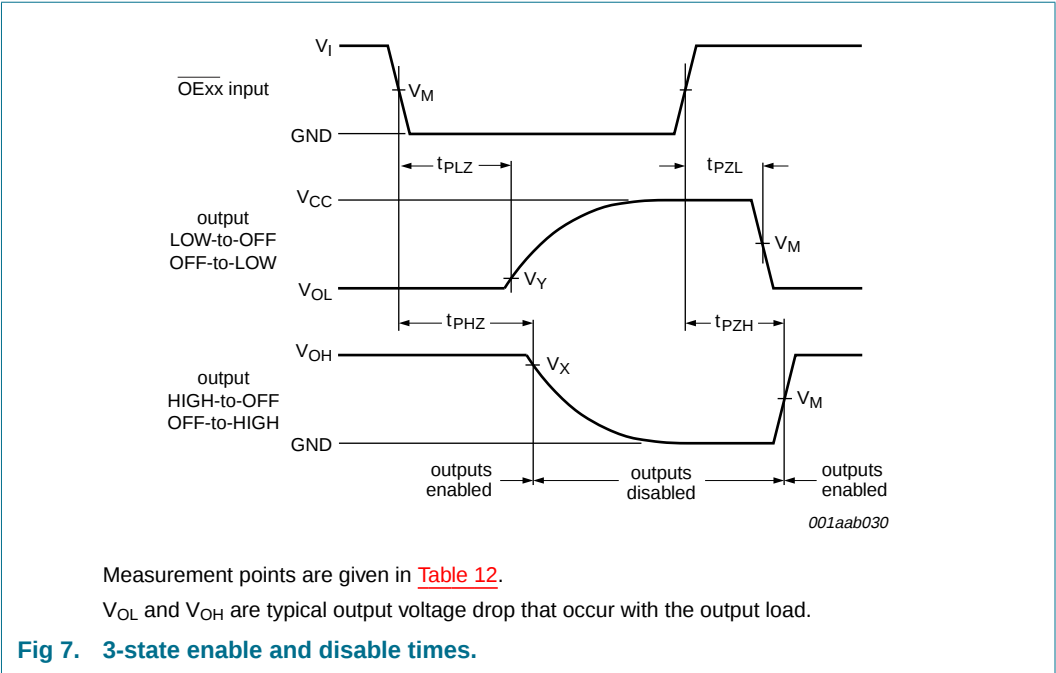


Table 12: Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
$< 2.7\text{ V}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \times V_{CC}$	$V_{OH} - 0.1 \times V_{CC}$
$\geq 2.7\text{ V}$	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

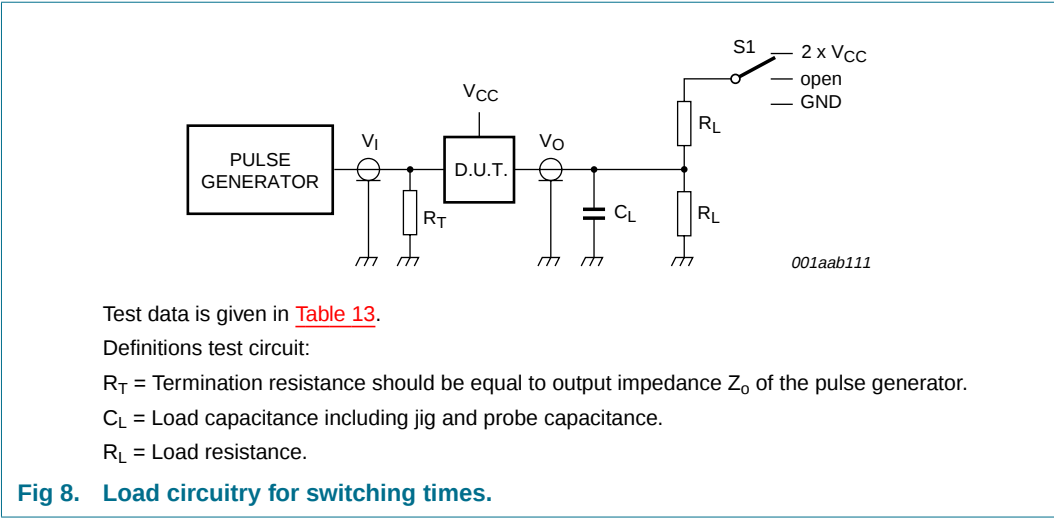


Table 13: Test data

Supply voltage	Input		Load		S1		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.2 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω ^[1]	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

[1] The circuit performs better when $R_L = 1000 \Omega$.

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

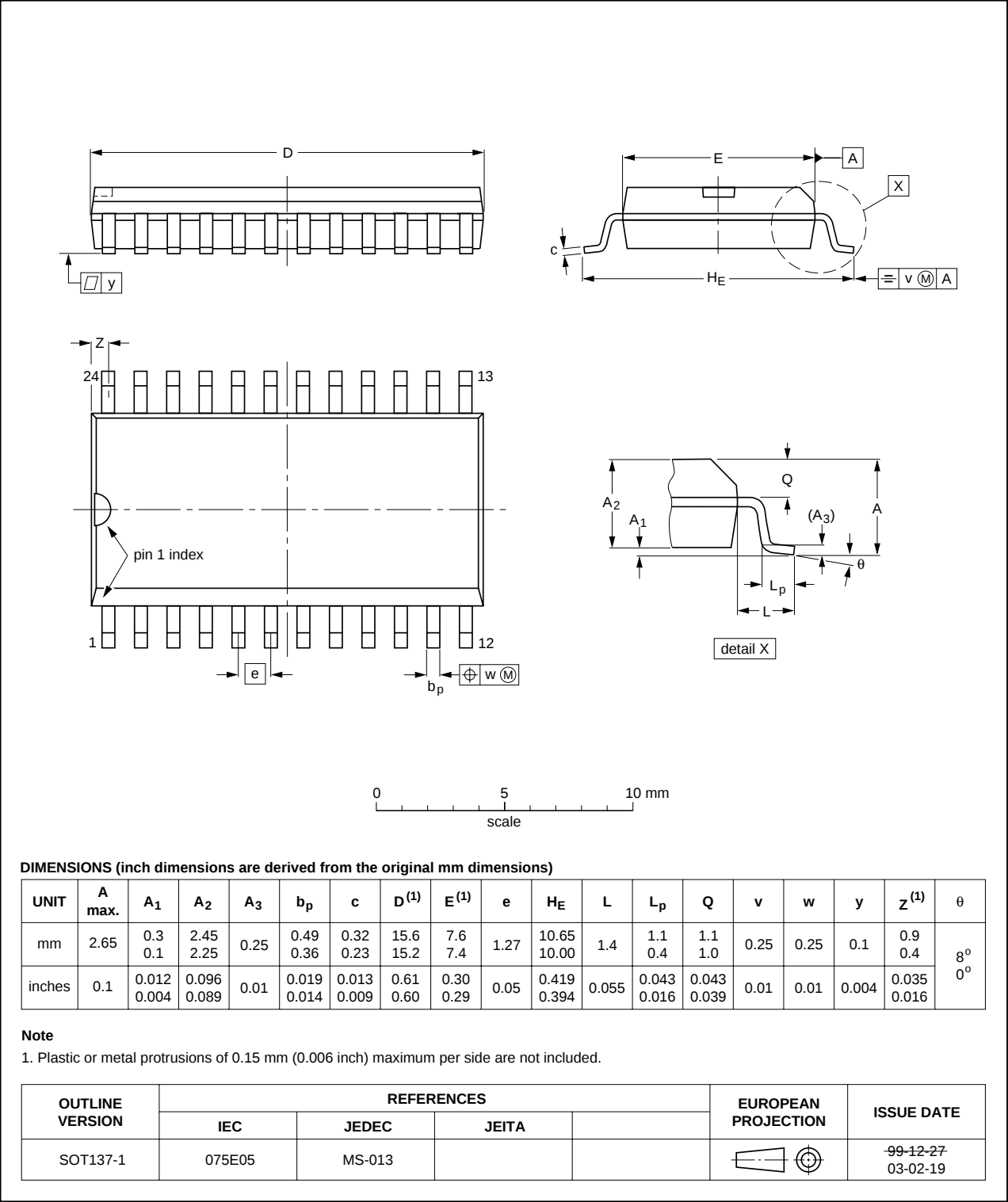


Fig 9. Package outline SO24.

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

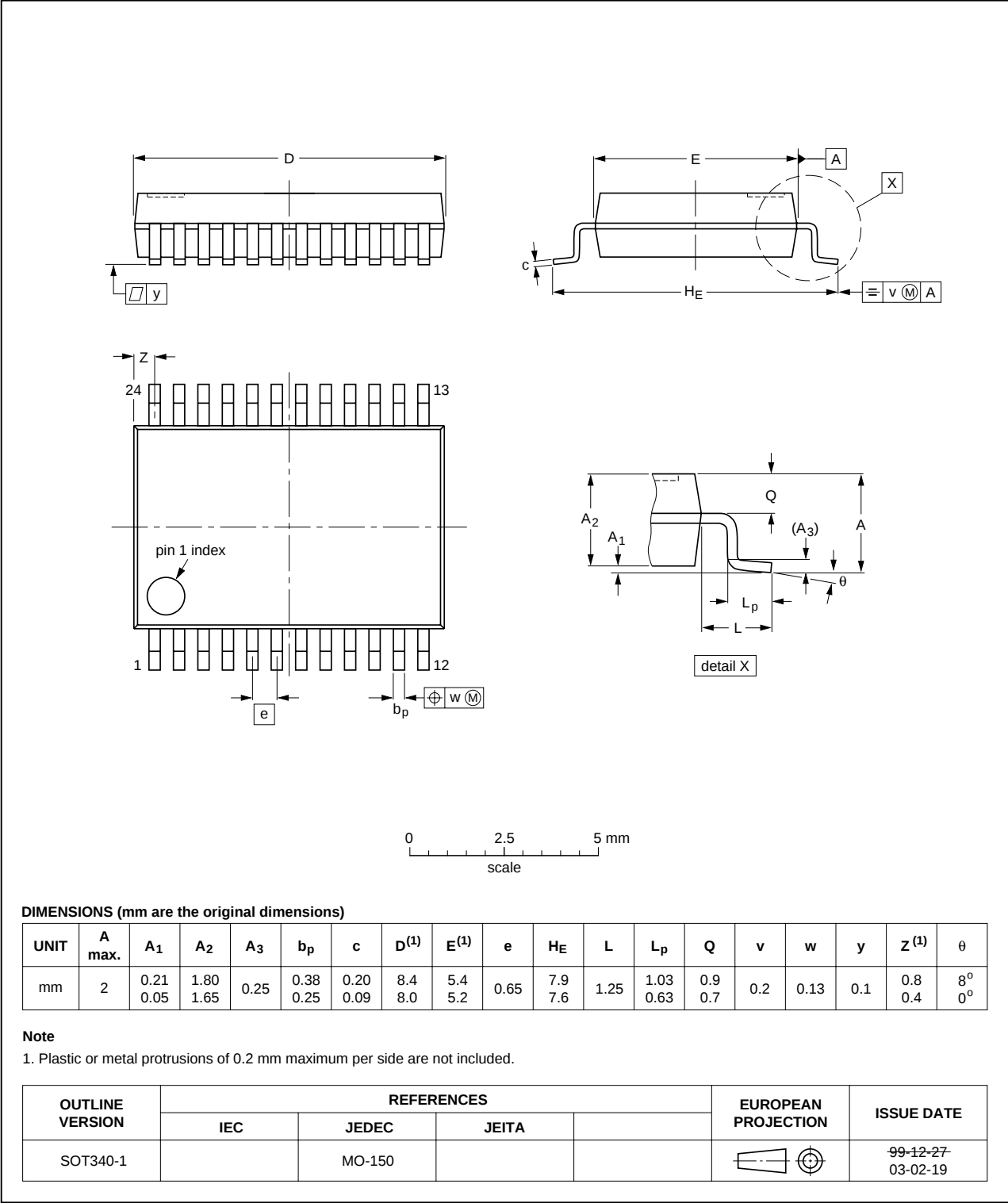


Fig 10. Package outline SSOP24.

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

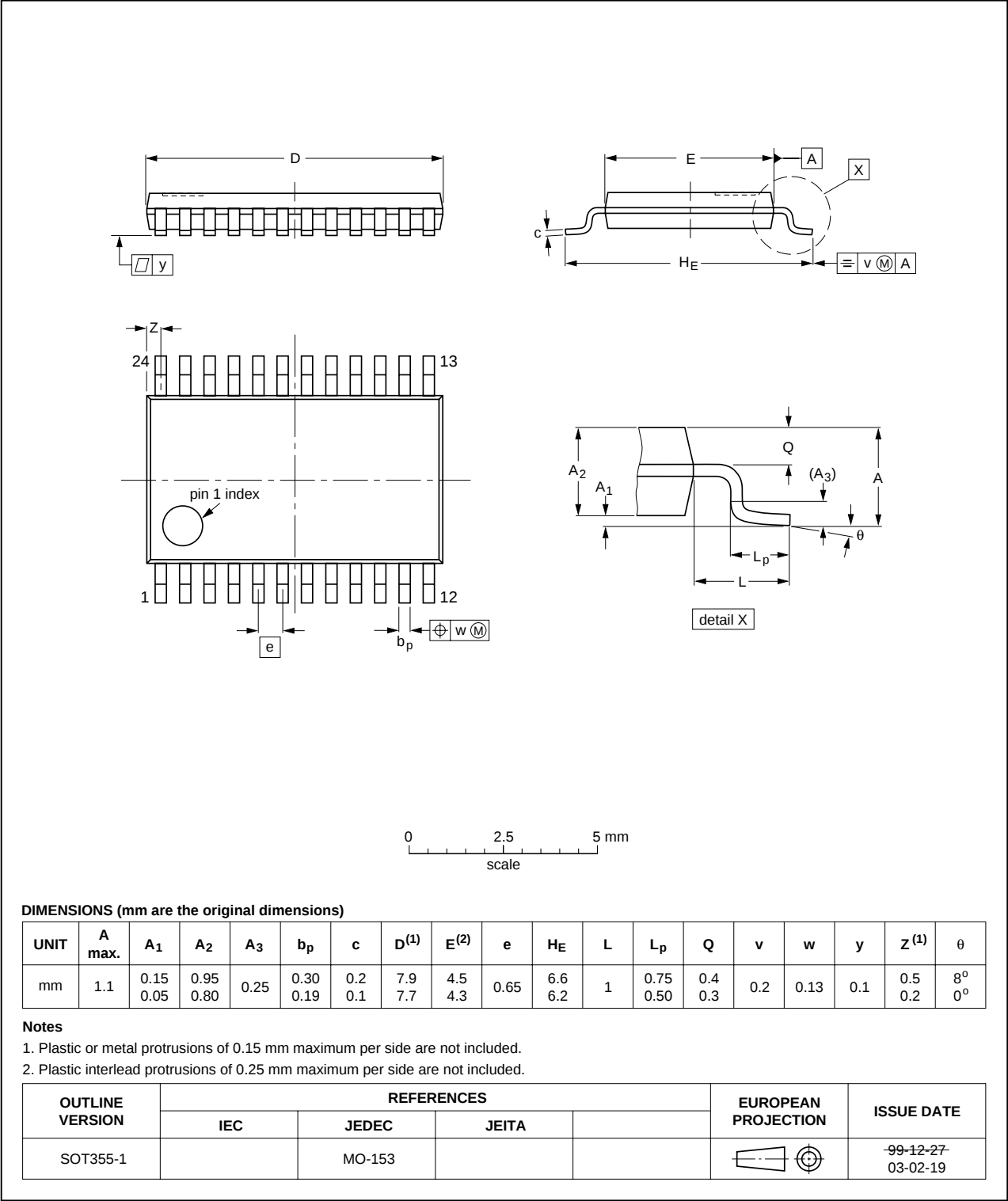


Fig 11. Package outline TSSOP24.

14. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74LVC2952A_2	20040629	Product data sheet	-	9397 750 13251	74LVC2952A_1
Modifications:					
• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors • Table 1: changed various values • Table 8: changed maximum value of I_{OZ} from $\pm 5 \mu A$ to $\pm 10 \mu A$ • Table 8: added values for $T_{amb} = -40^\circ C$ to $+125^\circ C$ • Table 9: changed various values • Table 9: added values for $T_{amb} = -40^\circ C$ to $+125^\circ C$.					
74LVC2952A_1	19980729	Product specification	-	9397 750 04524	-

15. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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