

74LVC157A

Quad 2-input multiplexer

Rev. 7 — 25 November 2011

Product data sheet

1. General description

The 74LVC157A is a quad 2-input multiplexer which select four bits of data from two sources under the control of a common select input (S). The four outputs present the selected data in the true (non-inverted) form. The enable input (\bar{E}) is active LOW. When pin \bar{E} is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all the other input conditions. Moving the data from two groups of registers to four common output buses is a common use of the 74LVC157A. The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

It is useful for implementing highly irregular logic by generating any 4 of the 16 different functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to pin S.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

2. Features and benefits

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40°C to $+85^{\circ}\text{C}$ and -40°C to $+125^{\circ}\text{C}$



3. Ordering information

Table 1. Ordering information

Type number	Package	Temperature range	Name	Description	Version
74LVC157AD	SO16	−40 °C to +125 °C		plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC157ADB	SSOP16	−40 °C to +125 °C		plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LVC157APW	TSSOP16	−40 °C to +125 °C		plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC157ABQ	DHVQFN16	−40 °C to +125 °C		plastic dual In-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

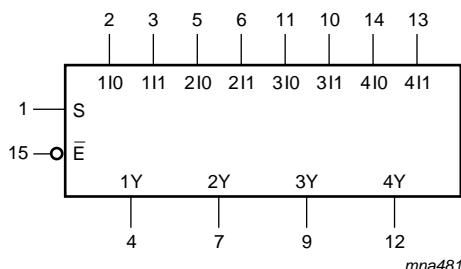


Fig 1. Logic symbol

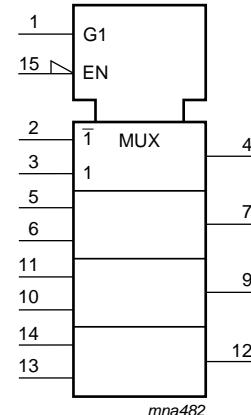


Fig 2. IEC logic symbol

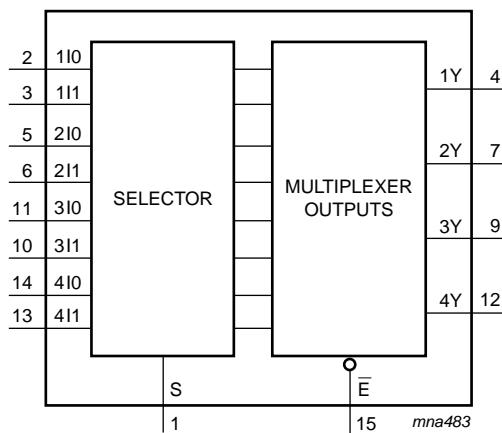


Fig 3. Functional diagram

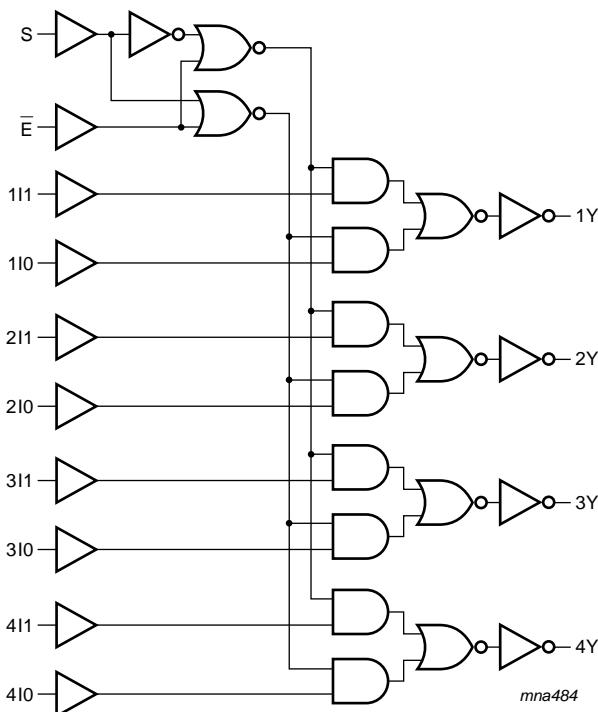


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

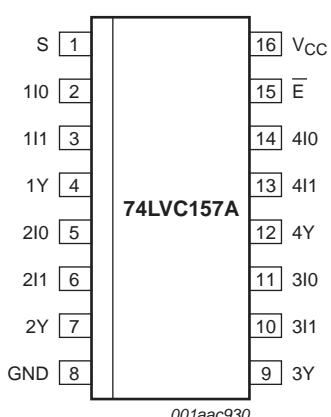


Fig 5. Pin configuration for SO16 and (T)SSOP16

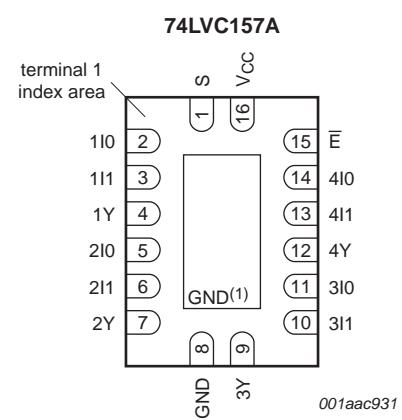


Fig 6. Pin configuration for DHVQFN16

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	common data select input
1I0	2	data input from source 0
1I1	3	data input from source 1
1Y	4	multiplexer output
2I0	5	data input from source 0
2I1	6	data input from source 1
2Y	7	multiplexer output
GND	8	ground (0 V)
3Y	9	multiplexer output
3I1	10	data input from source 1
3I0	11	data input from source 0
4Y	12	multiplexer output
4I1	13	data input from source 1
4I0	14	data input from source 0
\overline{E}	15	enable input (active LOW)
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table^[1]

Input				Output
\overline{E}	S	1I0	1I1	1Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0	-50	-	mA
V _I	input voltage		[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0	-	±50	mA
V _O	output voltage		[2] -0.5	V _{CC} + 0.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{STG}	storage temperature		-65	+150	°C
P _{TOT}	total power dissipation	T _{amb} = -40 °C to +125 °C	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO16 packages: above 70 °C the value of P_D derates linearly with 8 mW/K.

For (T)SSOP16 packages: above 60 °C the value of P_D derates linearly with 5.5 mW/K.

For DHVQFN16 packages: above 60 °C the value of P_D derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{AMB}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
I _I	input leakage current	I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
		V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	μA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	μA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	nl0, nl1 to nY; see Figure 8	[2]					
		$V_{CC} = 1.2 \text{ V}$	-	16	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	4.8	10.2	1.0	11.8	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.5	2.8	5.8	1.5	6.7	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	2.9	5.9	1.0	7.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.5	5.2	1.0	6.5	ns
		\bar{E} to nY; see Figure 7	[2]					
		$V_{CC} = 1.2 \text{ V}$	-	17	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.5	4.8	12.8	0.5	14.7	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.5	2.8	7.2	1.5	8.3	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	2.9	7.8	1.0	10.0	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.6	6.5	1.0	8.5	ns
		S to nY; see Figure 8	[2]					
		$V_{CC} = 1.2 \text{ V}$	-	16	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	5.1	12.4	1.0	14.3	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.5	3.0	7.0	1.5	8.1	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	3.1	7.3	1.0	9.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.7	6.3	1.0	8.0	ns
$t_{sk(o)}$	output skew time	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[3]		-	1.0	-	1.5 ns
C_{PD}	power dissipation capacitance	per input; $V_I = \text{GND to } V_{CC}$	[4]					
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	9.4	-	-	-	pF
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	12.8	-	-	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	15.9	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25 \text{ }^{\circ}\text{C}$ and $V_{CC} = 1.2 \text{ V}, 1.8 \text{ V}, 2.5 \text{ V}, 2.7 \text{ V}$, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

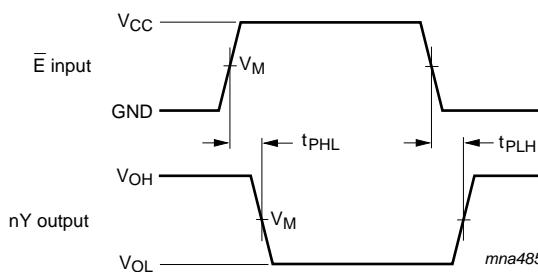
C_L = output load capacitance in pF

V_{CC} = supply voltage in V

N = number of inputs switching

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

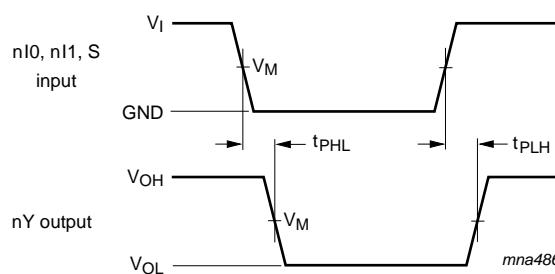
11. Waveforms



$V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$; $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

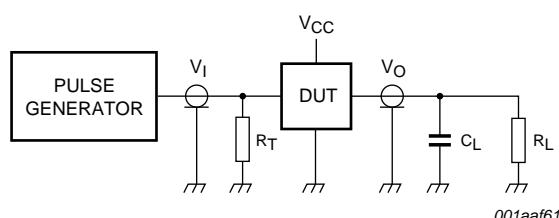
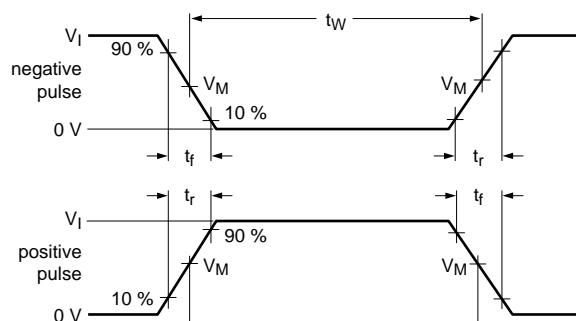
Fig 7. Enable input (\bar{E}) to output (nY) propagation delays



$V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$; $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. Data inputs ($nI0$, $nI1$) and common data select input (S) to output (nY) propagation delays



Test data is given in [Table 8](#). Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

Fig 9. Test circuit for measuring switching times

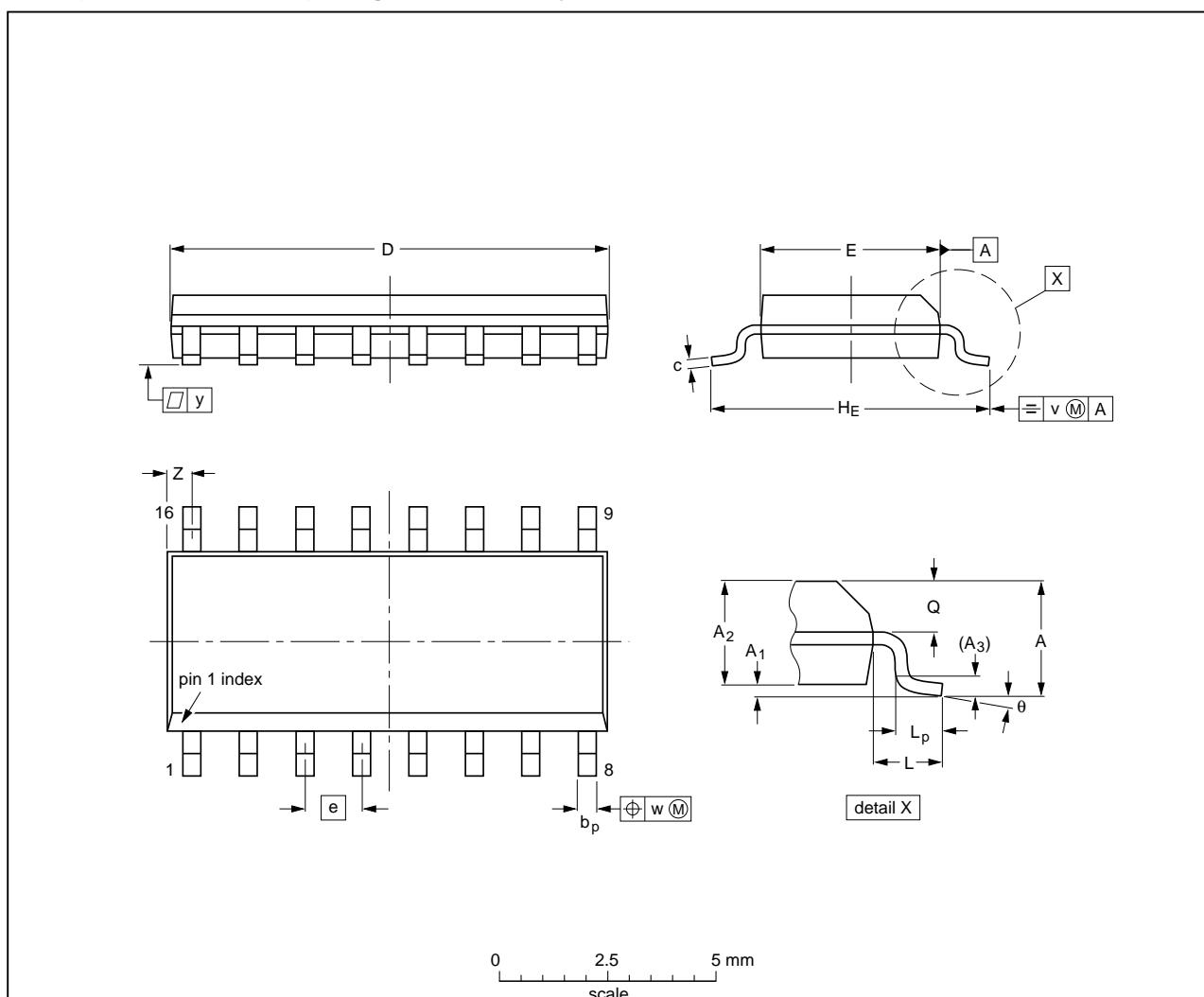
Table 8. Test data

Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75 0.10	0.25 0.125	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 10. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

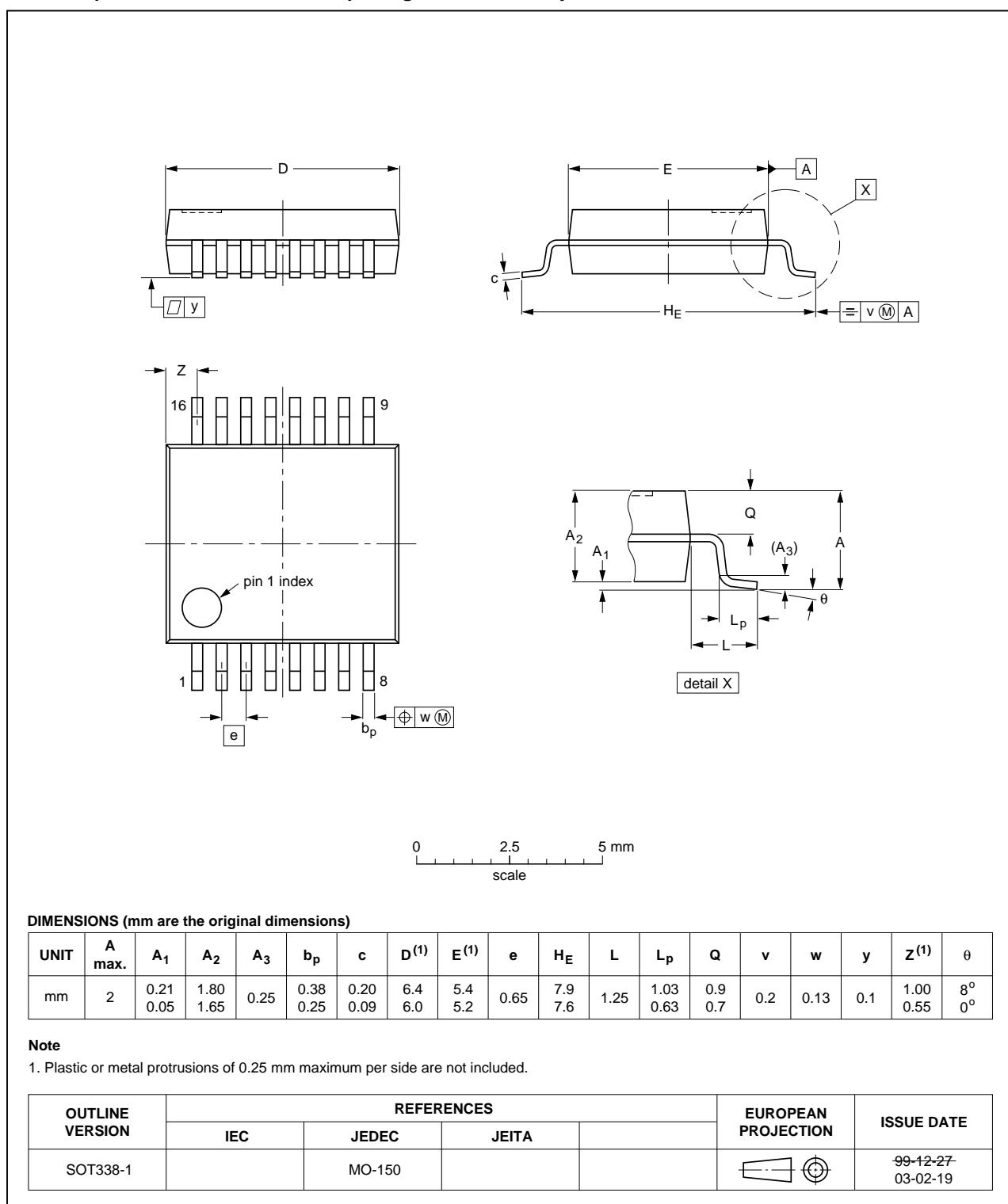


Fig 11. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

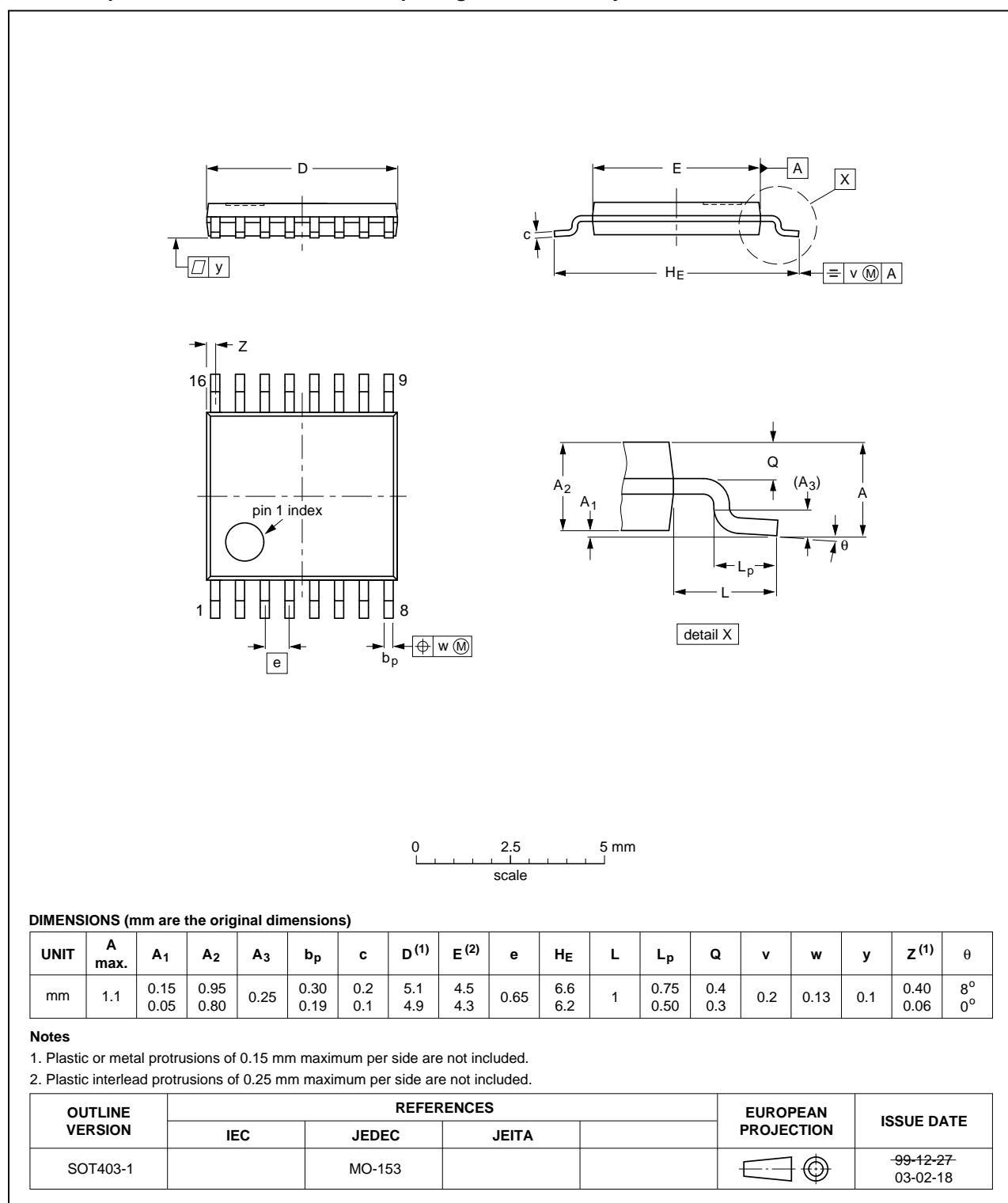


Fig 12. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

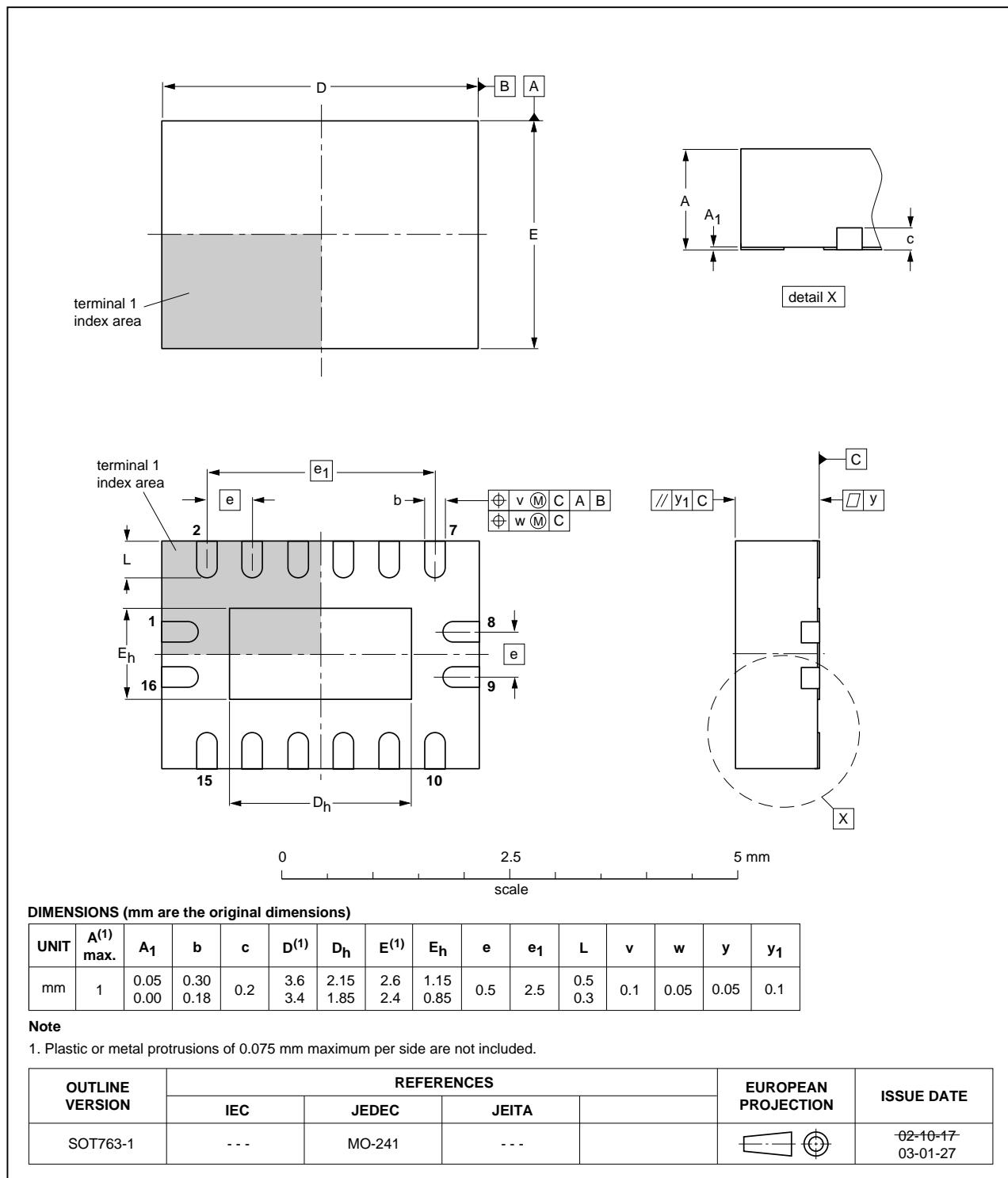


Fig 13. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC157A v.7	20111125	Product data sheet	-	74LVC157A v.6
Modifications:	<ul style="list-style-type: none"> • Table 7: maximum values for lower voltage ranges changed (errata). 			
74LVC157A v.6	20111027	Product data sheet	-	74LVC157A v.5
Modifications:	<ul style="list-style-type: none"> • The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 4, Table 5, Table 6, Table 7, and Table 8: values added for lower voltage ranges. 			
74LVC157A v.5	031202	Product specification	-	74LVC157A v.4
74LVC157A v.4	030617	Product specification	-	74LVC157A v.3
74LVC157A v.3	020315	Product specification	-	74LVC157A v.2
74LVC157A v.2	980729	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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