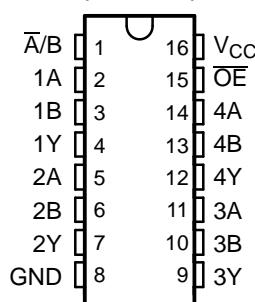


## FEATURES

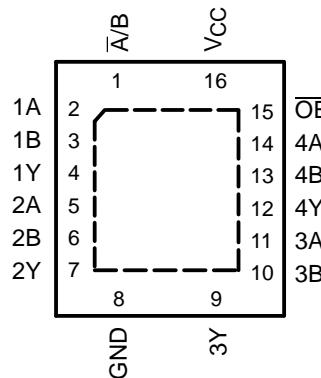
- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.6 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$

- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

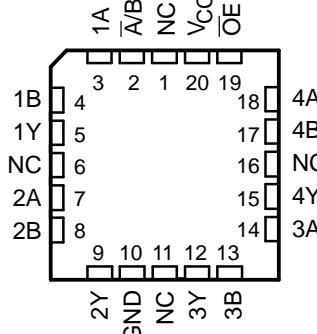
**SN54LVC257A...J OR W PACKAGE**  
**SN74LVC257A...D, DB, NS,**  
**OR PW PACKAGE**  
(TOP VIEW)



**SN74LVC257A...RGY PACKAGE**  
(TOP VIEW)



**SN54LVC257A...FK PACKAGE**  
(TOP VIEW)



NC – No internal connection

## DESCRIPTION/ORDERING INFORMATION

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The 'LVC257A devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ( $\overline{OE}$ ) input is at a high logic level.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
$-40^\circ\text{C}$ to $85^\circ\text{C}$	QFN – RGY	Reel of 1000	SN74LVC257ARGYR	LC257A	
	SOIC – D	Tube of 40	SN74LVC257AD	LVC257A	
		Reel of 2500	SN74LVC257ADR		
		Reel of 250	SN74LVC257ADT		
	SOP – NS	Reel of 2000	SN74LVC257ANSR	LVC257A	
	SSOP – DB	Reel of 2000	SN74LVC257ADBR	LC257A	
	TSSOP – PW	Tube of 90	SN74LVC257APW	LC257A	
$-55^\circ\text{C}$ to $125^\circ\text{C}$		Reel of 2000	SN74LVC257APWR		
		Reel of 250	SN74LVC257APWT		
CDIP – J	Tube of 25	SNJ54LVC257AJ	SNJ54LVC257AJ		
CFP – W	Tube of 150	SNJ54LVC257AW	SNJ54LVC257AW		
LCCC – FK	Tube of 55	SNJ54LVC257AFK	SNJ54LVC257AFK		

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

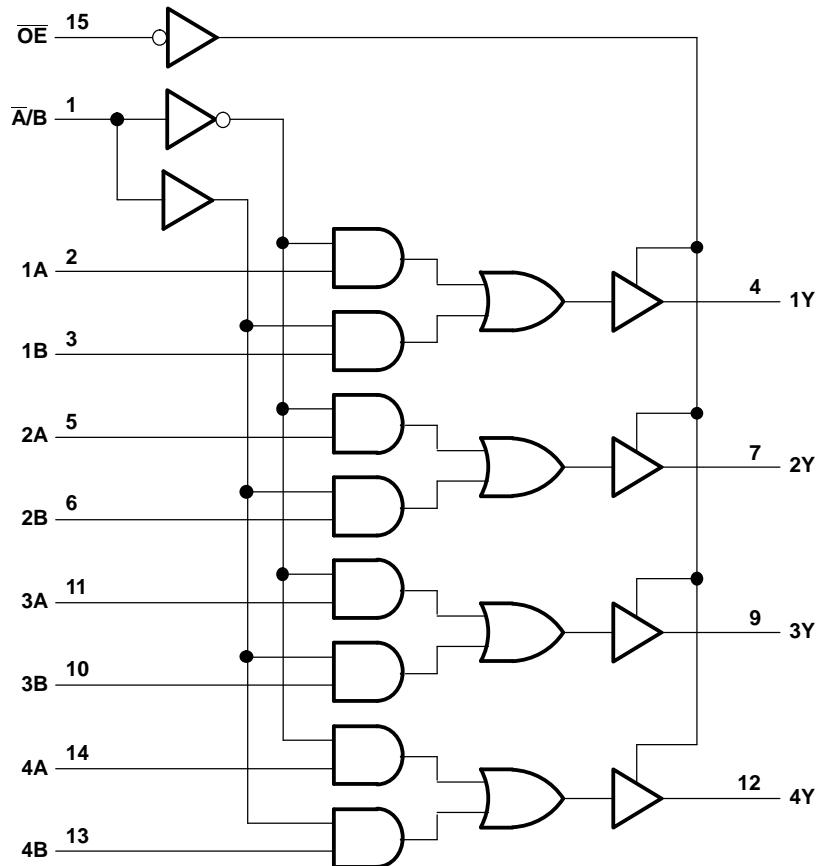
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**FUNCTION TABLE**

INPUTS				OUTPUT Y
$\overline{OE}$	$\overline{A}/B$	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the D, DB, J, NS, PW, RGY, and W packages.

**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	6.5
$V_I$	Input voltage range <sup>(2)</sup>		-0.5	6.5
$V_O$	Output voltage range <sup>(2)(3)</sup>		-0.5	$V_{CC} + 0.5$
$I_{IK}$	Input clamp current	$V_I < 0$		-50
$I_{OK}$	Output clamp current	$V_O < 0$		-50
$I_O$	Continuous output current			$\pm 50$
	Continuous current through $V_{CC}$ or GND			$\pm 100$
$\theta_{JA}$	Package thermal impedance	D package <sup>(4)</sup>		73
		DB package <sup>(4)</sup>		82
		NS package <sup>(4)</sup>		64
		PW package <sup>(4)</sup>		108
		RGY package <sup>(5)</sup>		39
$T_{stg}$	Storage temperature range		-65	150
				°C

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- The package thermal impedance is calculated in accordance with JESD 51-7.
- The package thermal impedance is calculated in accordance with JESD 51-5.

**Recommended Operating Conditions<sup>(1)</sup>**

		SN54LVC257A		SN74LVC257A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	Operating		2	3.6	V
		Data retention only		1.5	1.5	
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V			1.7	
		$V_{CC} = 2.7$ V to 3.6 V		2	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V			0.7	
		$V_{CC} = 2.7$ V to 3.6 V		0.8	0.8	
$V_I$	Input voltage	0	5.5	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 1.65$ V			-4	mA
		$V_{CC} = 2.3$ V			-8	
		$V_{CC} = 2.7$ V		-12	-12	
		$V_{CC} = 3$ V		-24	-24	
$I_{OL}$	Low-level output current	$V_{CC} = 1.65$ V			4	mA
		$V_{CC} = 2.3$ V			8	
		$V_{CC} = 2.7$ V		12	12	
		$V_{CC} = 3$ V		24	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

- All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54LVC257A, SN74LVC257A**  
**QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES**  
**WITH 3-STATE OUTPUTS**

SCAS294N—JANUARY 1993—REVISED JUNE 2005

 **TEXAS**  
**INSTRUMENTS**  
[www.ti.com](http://www.ti.com)

**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC257A			SN74LVC257A			UNIT
			MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 µA	1.65 V to 3.6 V				V <sub>CC</sub> - 0.2			V
	I <sub>OH</sub> = -100 µA	2.7 V to 3.6 V	V <sub>CC</sub> - 0.2						
	I <sub>OH</sub> = -4 mA	1.65 V				1.2			
	I <sub>OH</sub> = -8 mA	2.3 V				1.7			
	I <sub>OH</sub> = -12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	1.65 V to 3.6 V					0.2		V
		2.7 V to 3.6 V		0.2					
	I <sub>OL</sub> = 4 mA	1.65 V					0.45		
	I <sub>OL</sub> = 8 mA	2.3 V					0.7		
	I <sub>OL</sub> = 12 mA	2.7 V		0.4			0.4		
	I <sub>OL</sub> = 24 mA	3 V		0.55			0.55		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V		±5			±5	µA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V		±15			±10	µA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V		10			10	µA	
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V		500			500	µA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		5			5	pF	
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		5			5	pF	

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

**Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC257A				UNIT	
			V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			
			MIN	MAX	MIN	MAX		
t <sub>pd</sub>	A or B	Y			5.4	1	4.6	ns
	Ā/B				7.5	1	6.4	
t <sub>en</sub>	ĀĒ	Y			6.7	1	5.6	ns
t <sub>dis</sub>	ĀĒ	Y			4.7	0.5	4.3	ns
t <sub>sk(o)</sub>							1	ns

**Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

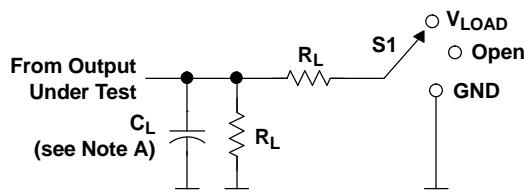
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC257A						UNIT		
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V				
			MIN	MAX	MIN	MAX	MIN	MAX			
t <sub>pd</sub>	A or B	Y	1	13.5	1	7.4	1	5.4	1	4.6	ns
	Ā/B		1	15.6	1	9.5	1	7.5	1	6.4	
t <sub>en</sub>	ĀĒ	Y	1	14.6	1	8.7	1	6.7	1	5.6	ns
t <sub>dis</sub>	ĀĒ	Y	1	15.4	1	6.7	1	4.7	1	4.3	ns
t <sub>sk(o)</sub>									1	ns	

## Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	UNIT
		TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance	$f = 10 \text{ MHz}$	13.5	14.5	15.5

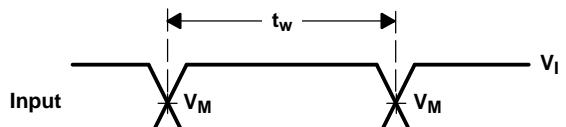
**PARAMETER MEASUREMENT INFORMATION**



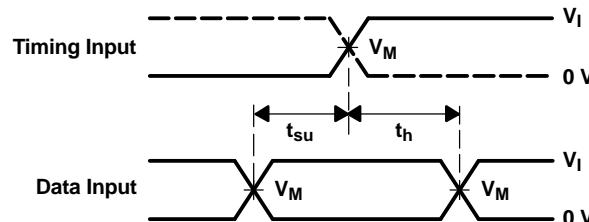
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

**LOAD CIRCUIT**

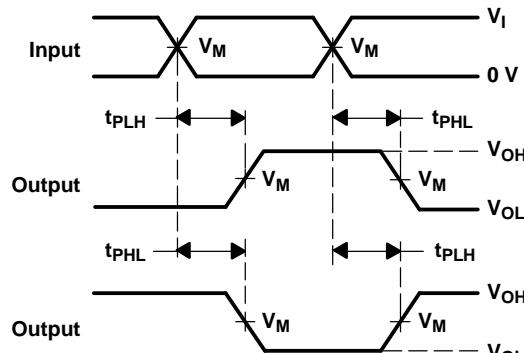
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_\Delta$
	$V_I$	$t_r/t_f$					
$1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



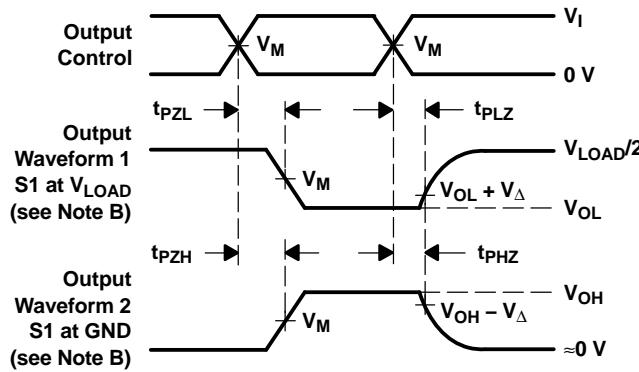
**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-0050901Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-0050901QEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
5962-0050901QFA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
SN74LVC257AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ADBLE	OBsolete	SSOP	DB	16		TBD	Call TI	Call TI	
SN74LVC257ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ADBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ADT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ADTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ADTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74LVC257ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257APWLE	OBsolete	TSSOP	PW	16		TBD	Call TI	Call TI	
SN74LVC257APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257APWRG3	PREVIEW	TSSOP	PW	16	2000	TBD	Call TI	Call TI	
SN74LVC257APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257APWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC257ARGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN74LVC257ARGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SNJ54LVC257AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LVC257AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LVC257AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC257A, SN74LVC257A :**

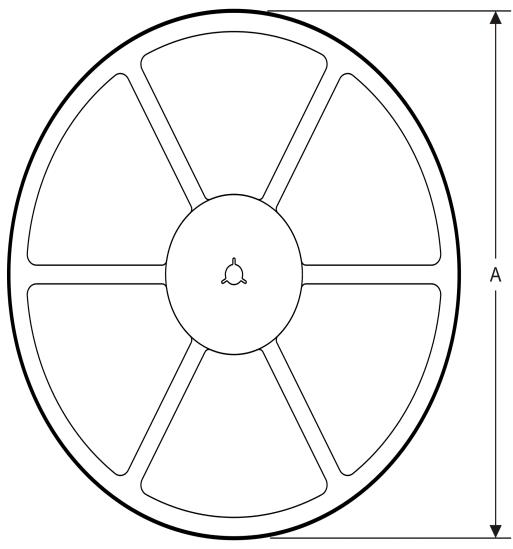
- Catalog: [SN74LVC257A](#)
- Automotive: [SN74LVC257A-Q1](#), [SN74LVC257A-Q1](#)
- Enhanced Product: [SN74LVC257A-EP](#), [SN74LVC257A-EP](#)
- Military: [SN54LVC257A](#)

NOTE: Qualified Version Definitions:

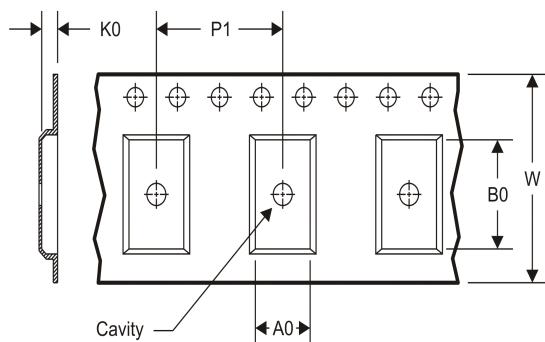
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

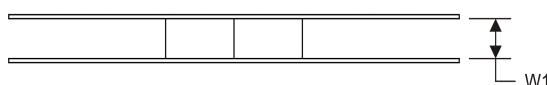
### REEL DIMENSIONS



### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



### TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC257ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LVC257ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC257ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC257APWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

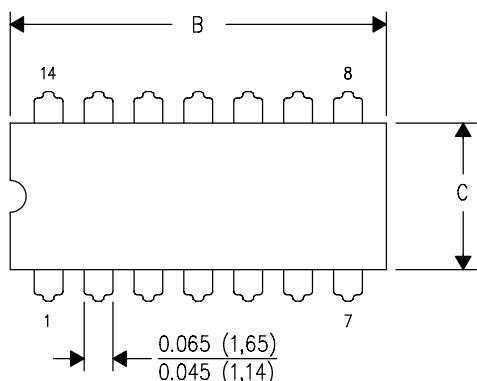

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC257ADBR	SSOP	DB	16	2000	346.0	346.0	33.0
SN74LVC257ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LVC257ANSR	SO	NS	16	2000	346.0	346.0	33.0
SN74LVC257APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LVC257APWR	TSSOP	PW	16	2000	346.0	346.0	29.0
SN74LVC257APWRG4	TSSOP	PW	16	2000	346.0	346.0	29.0
SN74LVC257APWT	TSSOP	PW	16	250	346.0	346.0	29.0
SN74LVC257ARGYR	VQFN	RGY	16	3000	346.0	346.0	29.0

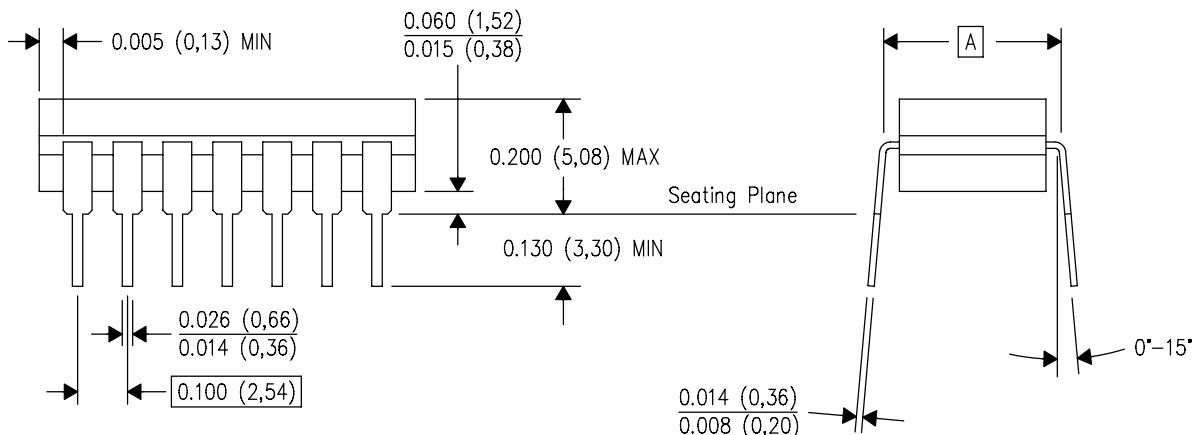
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

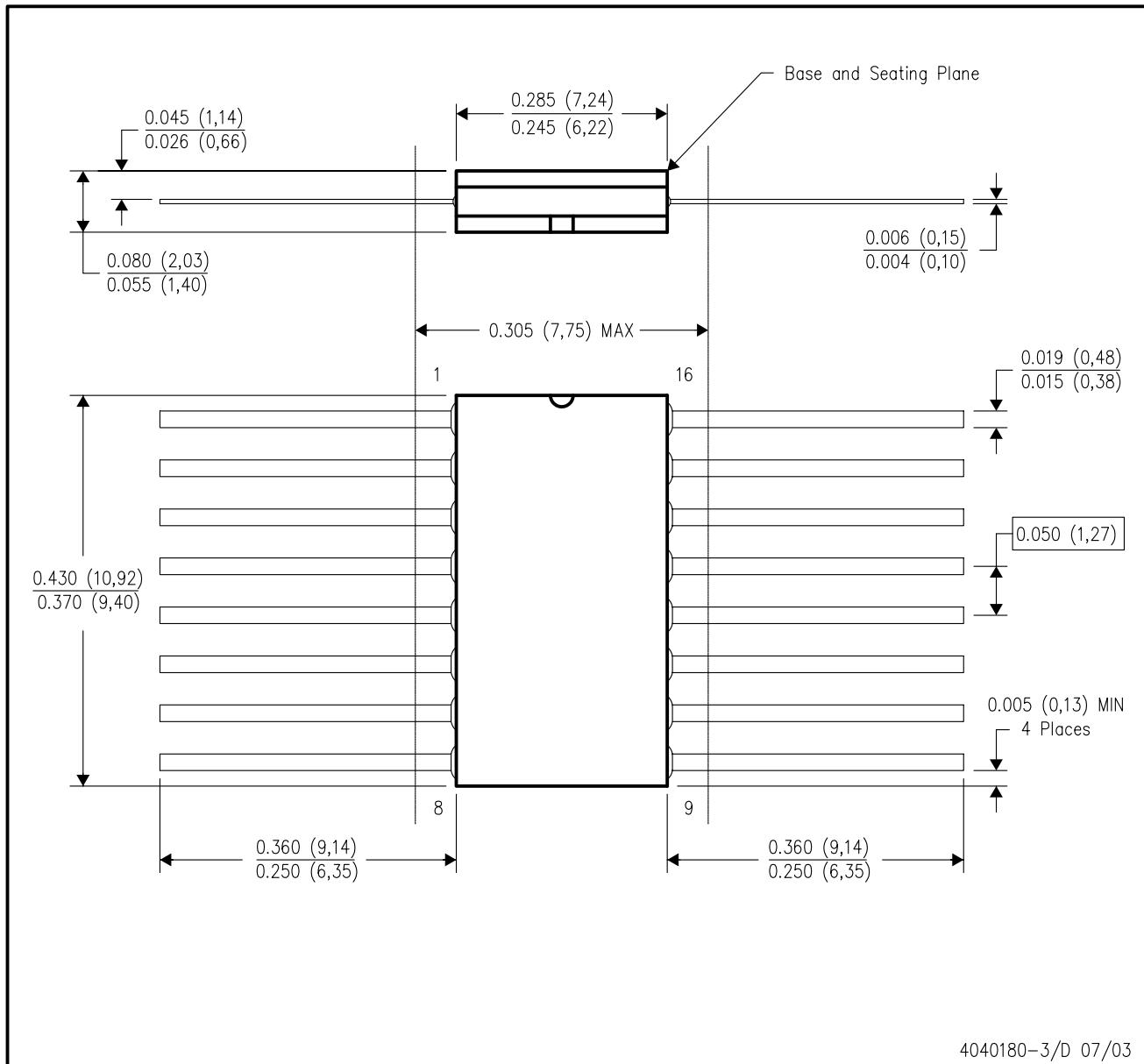


4040083/F 03/03

- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

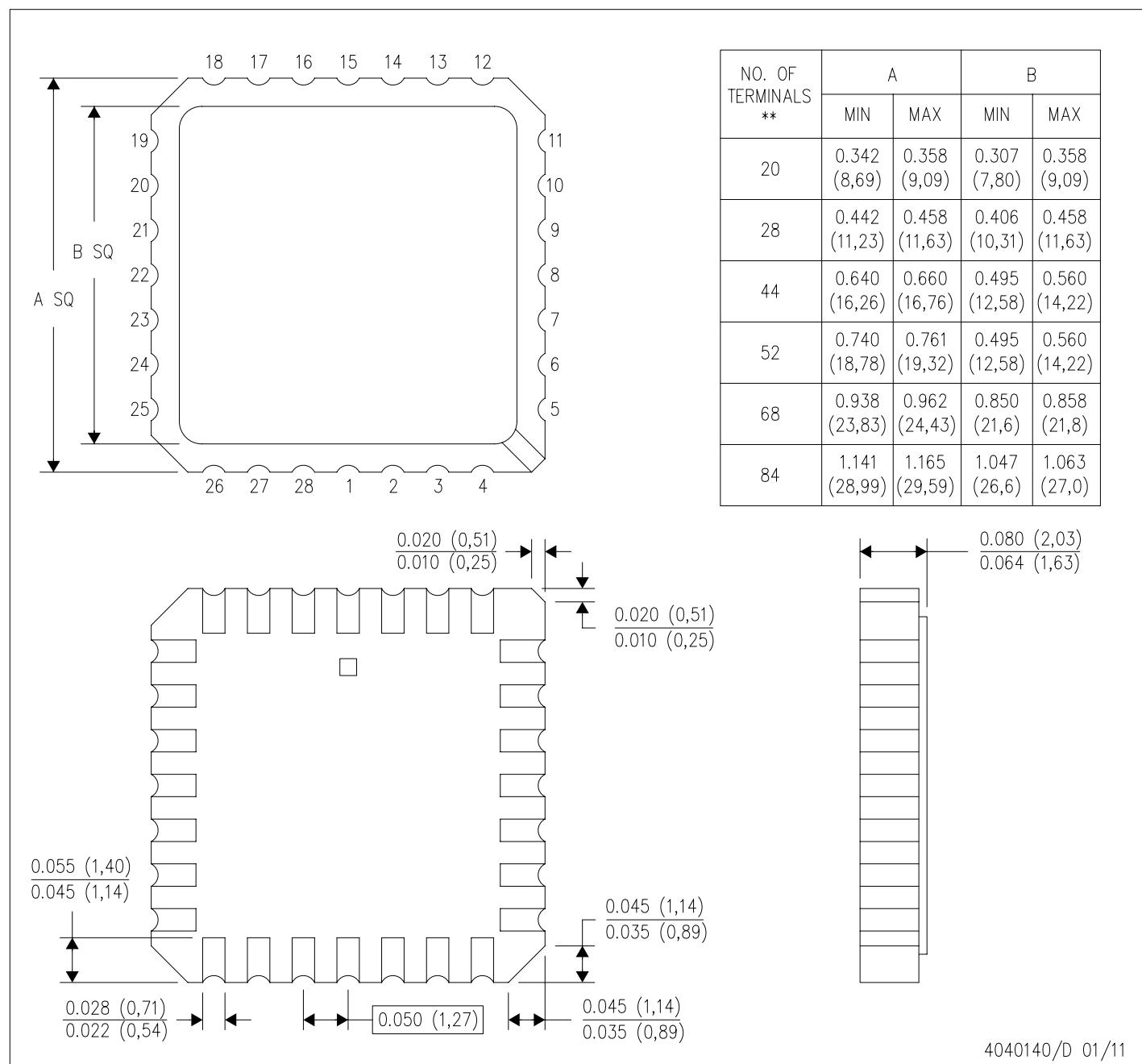


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL-STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER

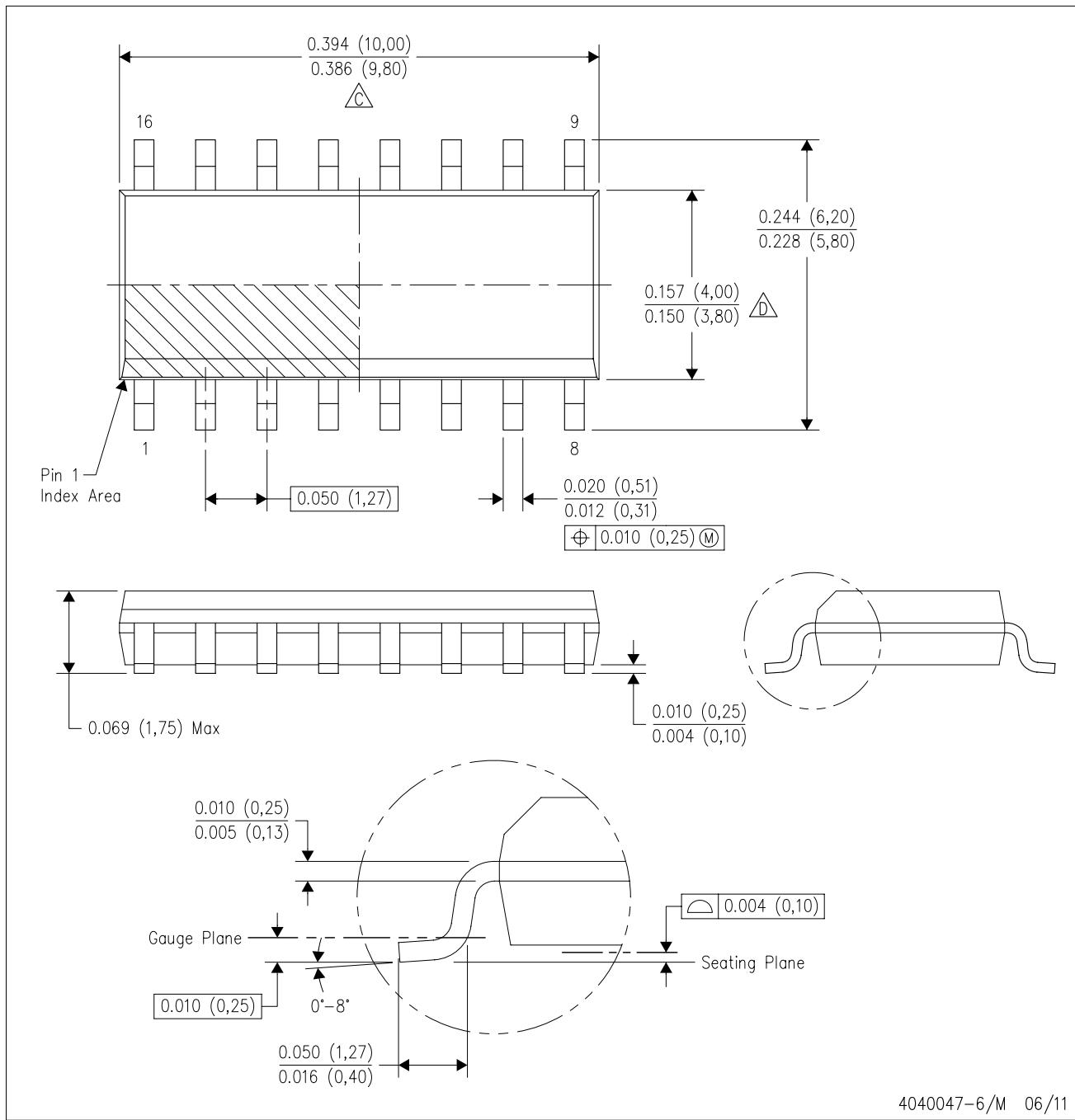


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. Falls within JEDEC MS-004

4040140/D 01/11

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

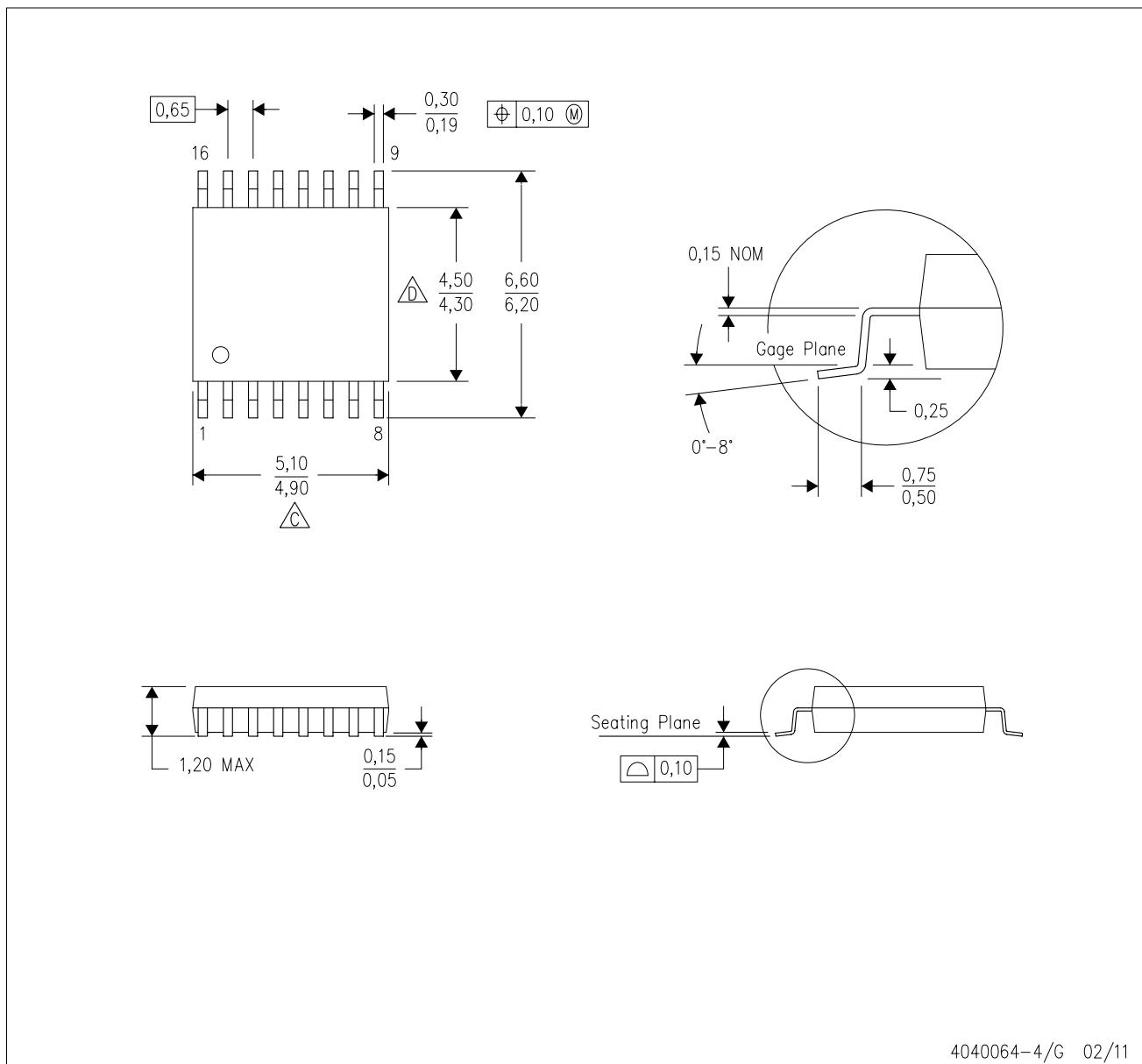
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

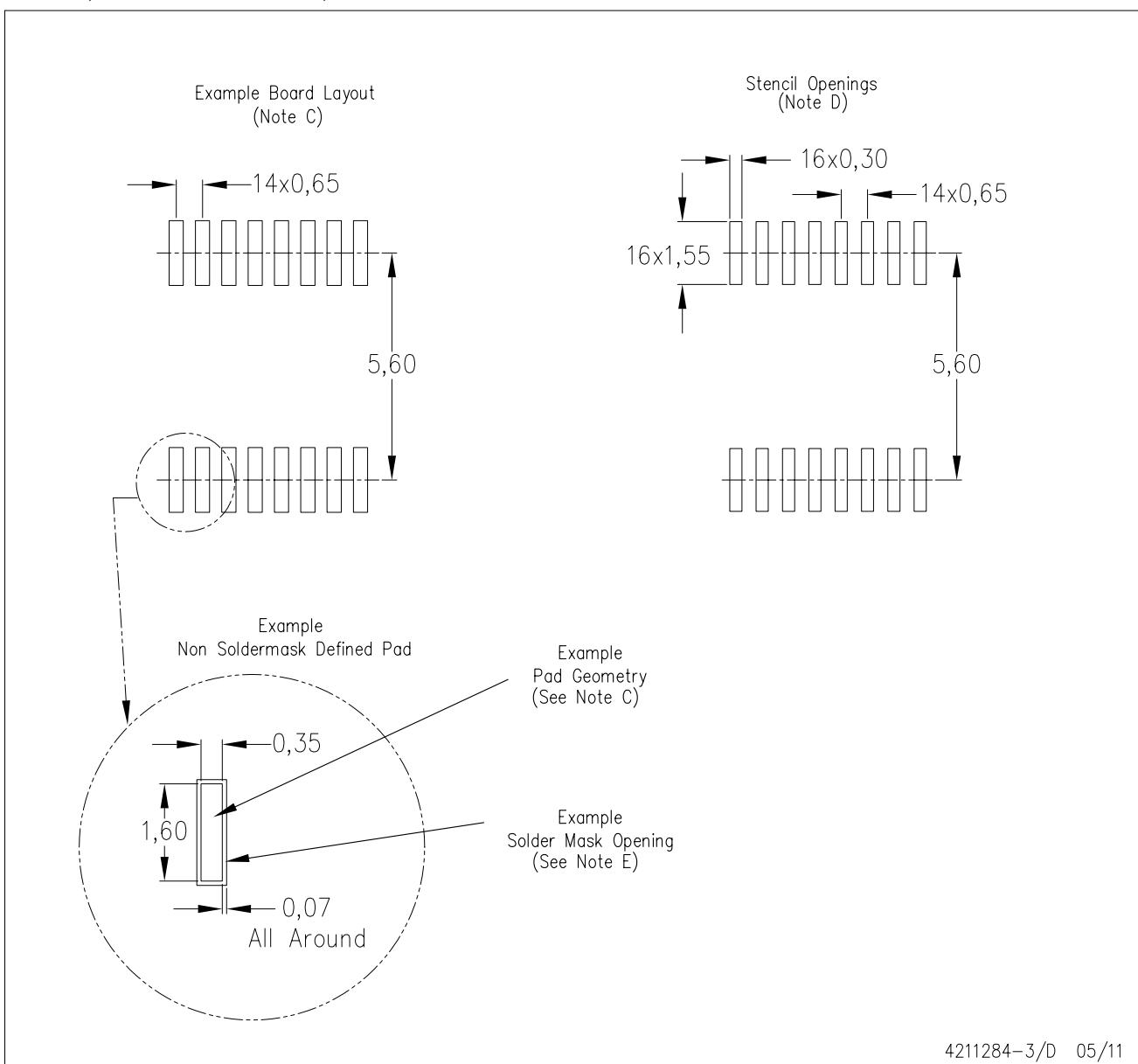
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



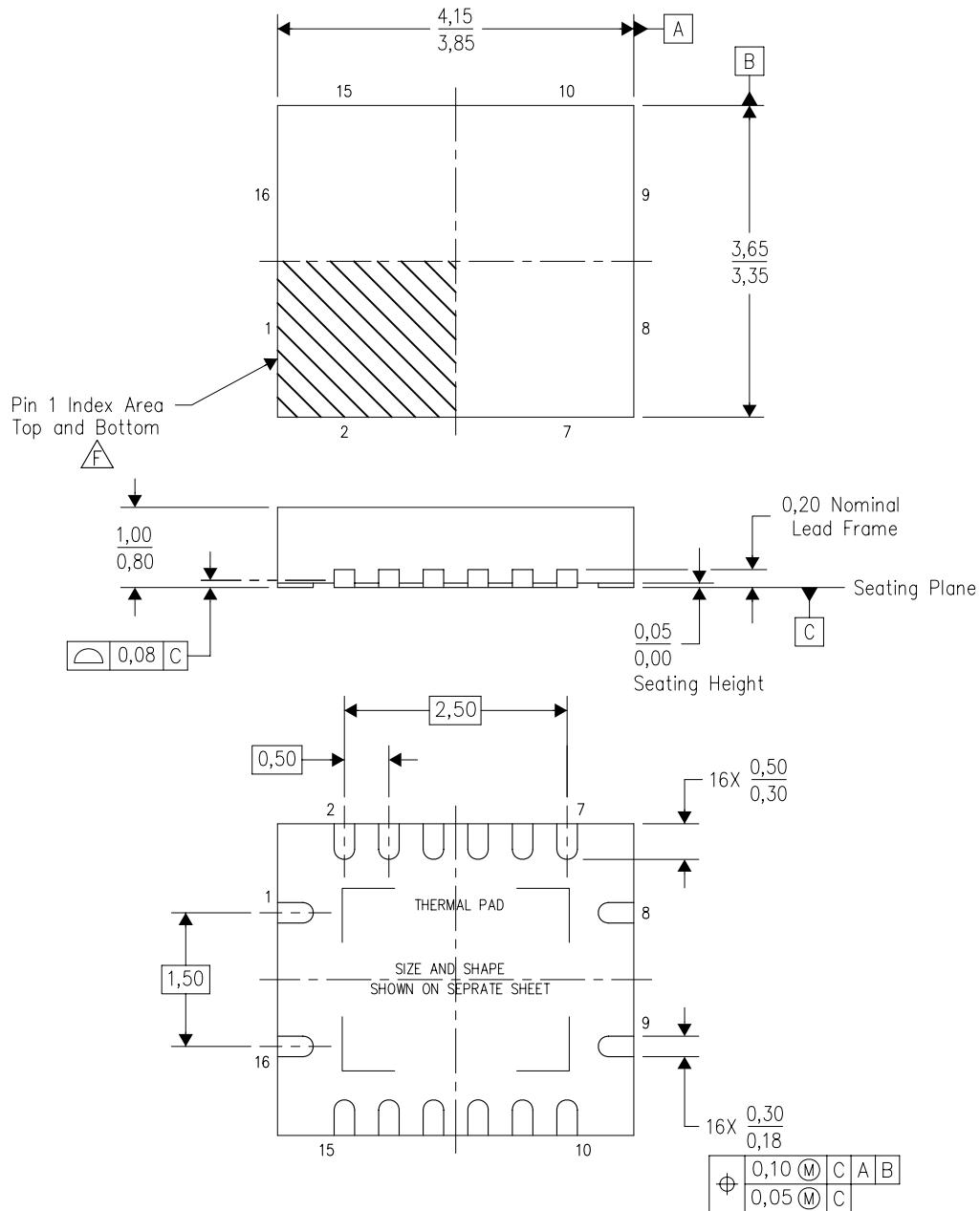
4211284-3/D 05/11

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



### Bottom View

4203539-3/l 06/2011

NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

 F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.  
The Pin 1 identifiers are either a molded, marked, or metal feature.

- G. Package complies to JEDEC MO-241 variation BA.

# THERMAL PAD MECHANICAL DATA

RGY (R-PVQFN-N16)

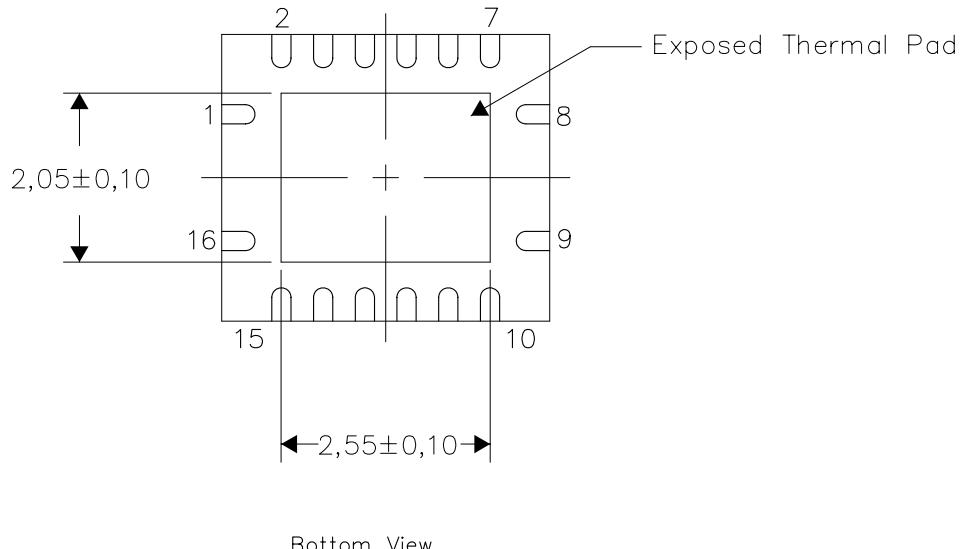
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

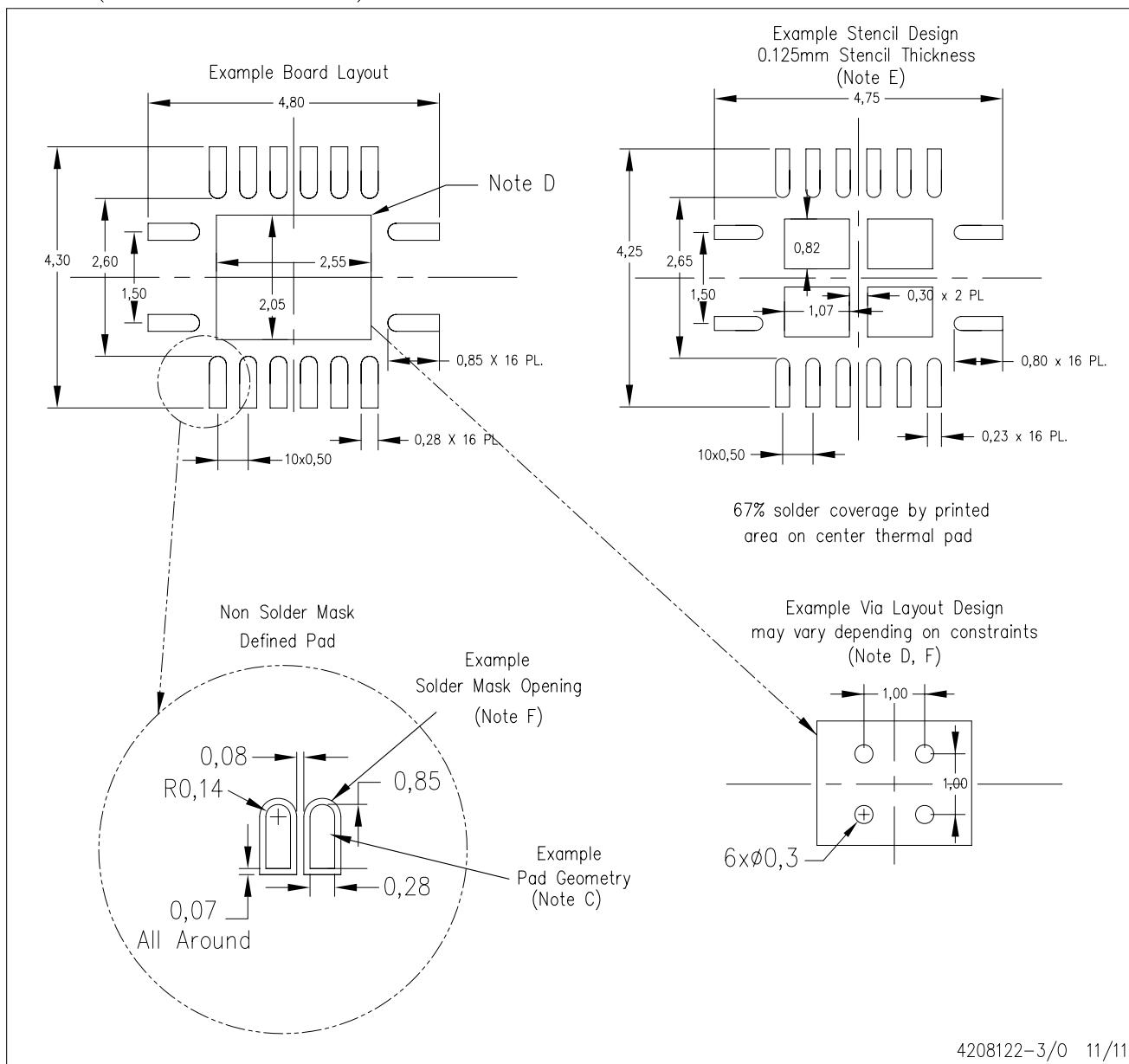
4206353-3/0 11/11

NOTE: All linear dimensions are in millimeters

## LAND PATTERN DATA

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



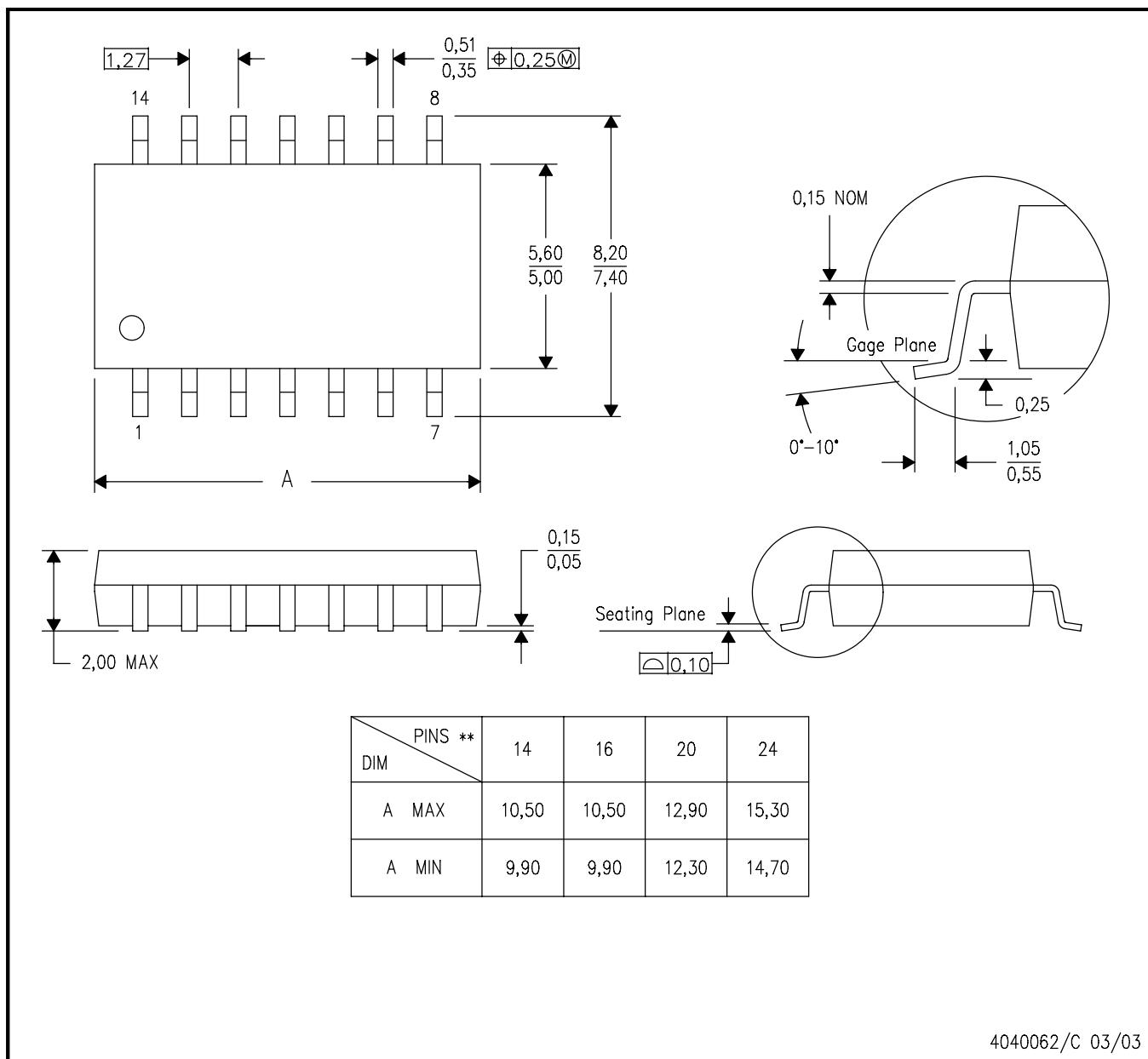
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



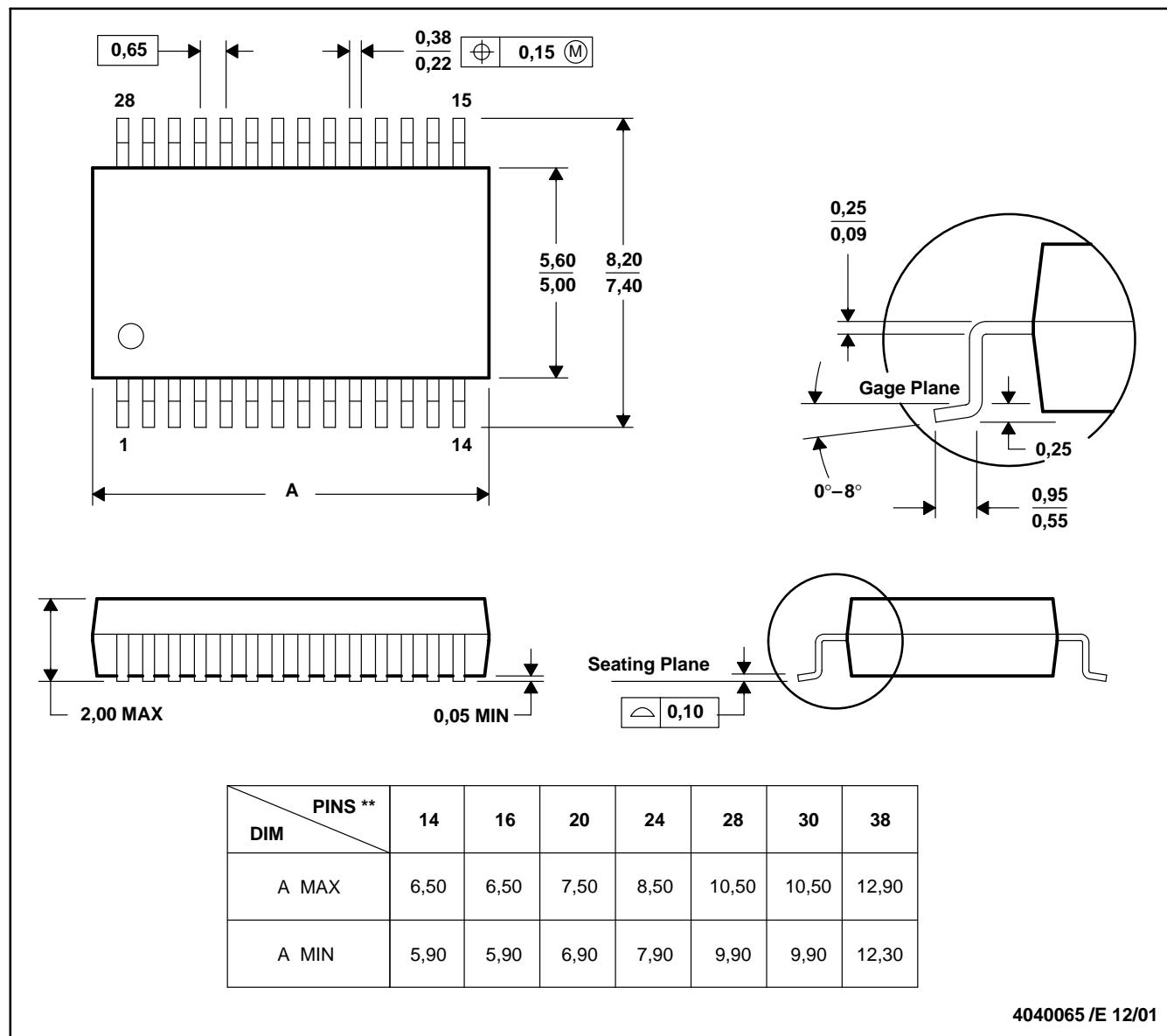
NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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