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Kind regards,

Team Nexperia

74LVC1G97

Low-power configurable multiple function gate

Rev. 5 — 12 December 2016

Product data sheet

1. General description

The 74LVC1G97 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions MUX, AND, OR, NAND, NOR, inverter and buffer; using the 3-bit input. All inputs can be connected to V_{CC} or GND.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8B/JESD36 (2.7 V to 3.6 V).
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C.



3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G97GW	−40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363
74LVC1G97GV	−40 °C to +125 °C	SC-74	plastic surface mounted package; 6 leads	SOT457
74LVC1G97GM	−40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G97GF	−40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm	SOT891
74LVC1G97GN	−40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74LVC1G97GS	−40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74LVC1G97GX	−40 °C to +125 °C	X2SON6	plastic thermal extremely thin small outline package; no leads; 6 terminals; body 1 × 0.8 × 0.35 mm	SOT1255

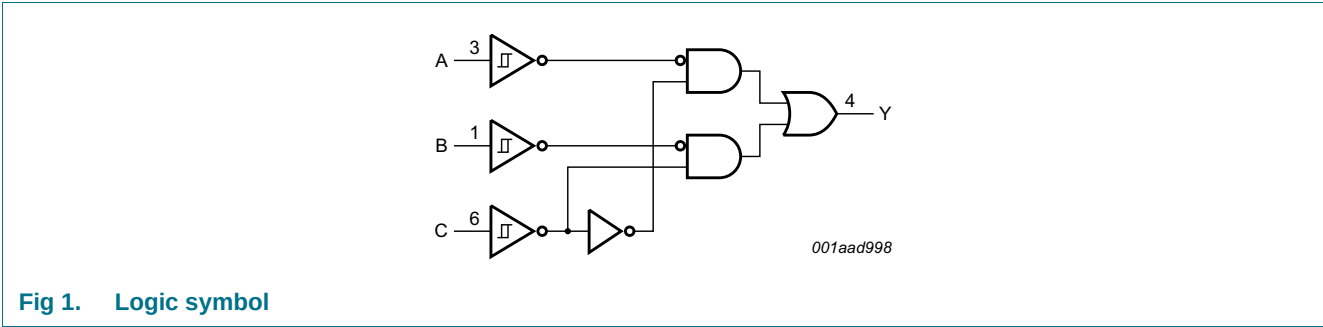
4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74LVC1G97GW	YV
74LVC1G97GV	Y97
74LVC1G97GM	YV
74LVC1G97GF	YV
74LVC1G97GN	YV
74LVC1G97GS	YV
74LVC1G97GX	YV

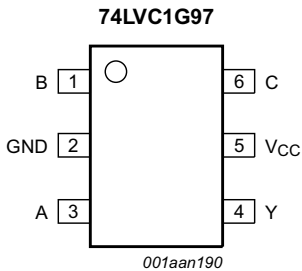
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



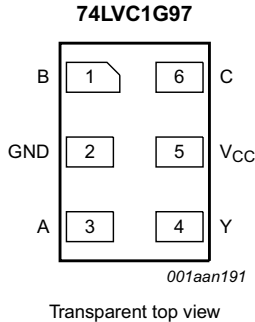
6. Pinning information

6.1 Pinning



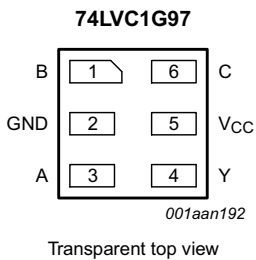
74LVC1G97

Pin configuration SOT363 and SOT457. The package is shown with pins 1 through 6. Pin 1 is labeled B, pin 2 is GND, pin 3 is A, pin 4 is Y, pin 5 is V_{CC}, and pin 6 is C. The diagram is labeled 001aan190.



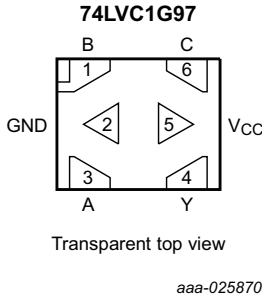
74LVC1G97

Pin configuration SOT886. The package is shown with pins 1 through 6. Pin 1 is labeled B, pin 2 is GND, pin 3 is A, pin 4 is Y, pin 5 is V_{CC}, and pin 6 is C. The diagram is labeled 001aan191 and Transparent top view.



74LVC1G97

Pin configuration SOT891, SOT1115 and SOT1202. The package is shown with pins 1 through 6. Pin 1 is labeled B, pin 2 is GND, pin 3 is A, pin 4 is Y, pin 5 is V_{CC}, and pin 6 is C. The diagram is labeled 001aan192 and Transparent top view.



74LVC1G97

Pin configuration SOT1255. The package is shown with pins 1 through 6. Pin 1 is labeled B, pin 2 is GND, pin 3 is A, pin 4 is Y, pin 5 is V_{CC}, and pin 6 is C. The diagram is labeled aaa-025870 and Transparent top view.

Fig 2. Pin configuration SOT363 and SOT457

Fig 3. Pin configuration SOT886

Fig 4. Pin configuration SOT891, SOT1115 and SOT1202

Fig 5. Pin configuration SOT1255

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
GND	2	ground (0 V)
A	3	data input
Y	4	data output
V _{CC}	5	supply voltage
C	6	data input

7. Functional description

Table 4. Function table^[1]

Input			Output
C	B	A	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

[1] H = HIGH voltage level; L = LOW voltage level.

7.1 Logic configurations

Table 5. Function selection table

Logic function	Figure
2-input MUX	see Figure 6
2-input AND	see Figure 7
2-input OR with one input inverted	see Figure 8
2-input NAND with one input inverted	see Figure 8
2-input AND with one input inverted	see Figure 9
2-input NOR with one input inverted	see Figure 9
2-input OR	see Figure 10
Inverter	see Figure 11
Buffer	see Figure 12

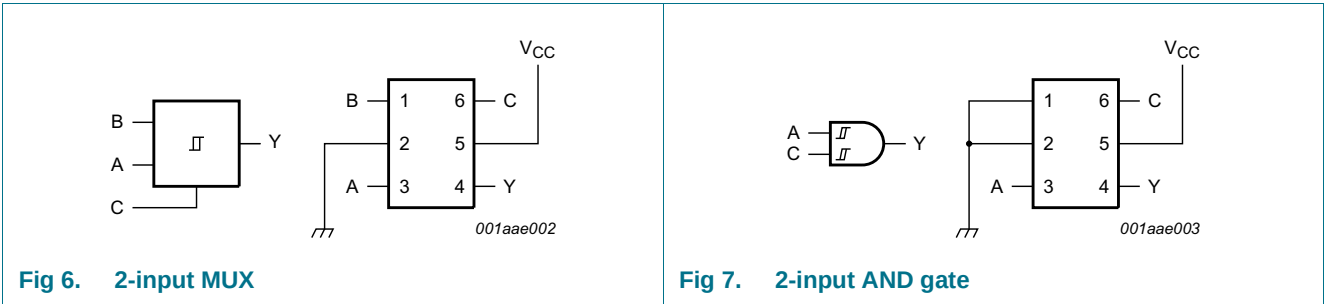


Fig 8. 2-input NAND gate with input A inverted or 2-input OR gate with input C inverted

Fig 9. 2-input NOR gate with input B inverted or 2-input AND gate with input C inverted

Fig 10. 2-input OR gate

Fig 11. Inverter

Fig 12. Buffer

8. Limiting values

Table 6. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		−0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	−50	-	mA
V _I	input voltage	[1]	−0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	Active mode [1][2]	−0.5	+6.5	V
		Power-down mode [1][2]	−0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	+100	mA

Table 6. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{\text{amb}} = -40\text{ °C to }+125\text{ °C}$ [3]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{\text{CC}} = 0\text{ V}$ (Power-down mode), the output voltage can be 5.5 V in normal operation.[3] For SC-88 and SC-74 packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.For XSON6 and X2SON6 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_{I}	input voltage		0	-	5.5	V
V_{O}	output voltage	Active mode	0	-	V_{CC}	V
		$V_{\text{CC}} = 0\text{ V}$; Power-down mode	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_{\text{I}} = V_{\text{CC}}$ or GND						
		$I_{\text{O}} = 100\text{ }\mu\text{A}$; $V_{\text{CC}} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.1	-	0.1	V
		$I_{\text{O}} = 4\text{ mA}$; $V_{\text{CC}} = 1.65\text{ V}$	-	-	0.45	-	0.7	V
		$I_{\text{O}} = 8\text{ mA}$; $V_{\text{CC}} = 2.3\text{ V}$	-	-	0.3	-	0.45	V
		$I_{\text{O}} = 12\text{ mA}$; $V_{\text{CC}} = 2.7\text{ V}$	-	-	0.4	-	0.6	V
		$I_{\text{O}} = 24\text{ mA}$; $V_{\text{CC}} = 3.0\text{ V}$	-	-	0.55	-	0.8	V
		$I_{\text{O}} = 32\text{ mA}$; $V_{\text{CC}} = 4.5\text{ V}$	-	-	0.55	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_{\text{I}} = V_{\text{CC}}$ or GND						
		$I_{\text{O}} = -100\text{ }\mu\text{A}$; $V_{\text{CC}} = 1.65\text{ V to }5.5\text{ V}$	$V_{\text{CC}} - 0.1$	-	-	$V_{\text{CC}} - 0.1$	-	V
		$I_{\text{O}} = -4\text{ mA}$; $V_{\text{CC}} = 1.65\text{ V}$	1.2	-	-	0.95	-	V
		$I_{\text{O}} = -8\text{ mA}$; $V_{\text{CC}} = 2.3\text{ V}$	1.9	-	-	1.7	-	V
		$I_{\text{O}} = -12\text{ mA}$; $V_{\text{CC}} = 2.7\text{ V}$	2.2	-	-	1.9	-	V
		$I_{\text{O}} = -24\text{ mA}$; $V_{\text{CC}} = 3.0\text{ V}$	2.3	-	-	2.0	-	V
		$I_{\text{O}} = -32\text{ mA}$; $V_{\text{CC}} = 4.5\text{ V}$	3.8	-	-	3.4	-	V
I_{I}	input leakage current	$V_{\text{I}} = 5.5\text{ V}$ or GND; $V_{\text{CC}} = 0\text{ V to }5.5\text{ V}$	-	± 0.1	± 1	-	± 1	μA

Table 8. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	±0.1	±2	-	±2	μA
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	0.1	4	-	4	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} – 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	-	5	500	-	500	μA
C _I	input capacitance		-	2.5	-	-	-	pF

[1] Typical values are measured at maximum V_{CC} and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 9. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 14](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	A, B, C to Y; see Figure 13 ^[2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	6.0	14.4	1.0	18.0	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	3.5	8.3	0.5	10.4	ns
		V _{CC} = 2.7 V	0.5	4.2	8.5	0.5	10.6	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	3.8	6.3	0.5	7.9	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	3.0	5.1	0.5	6.4	ns
C _{PD}	power dissipation capacitance	V _{CC} = 3.3 V; V _I = GND to V _{CC} ^[3]	-	22	-	-	-	pF

[1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.[2] t_{pd} is the same as t_{PLH} and t_{PHL}.[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$
f_i = input frequency in MHz;f_o = output frequency in MHz;C_L = output load capacitance in pF;V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of outputs.

12. Waveforms

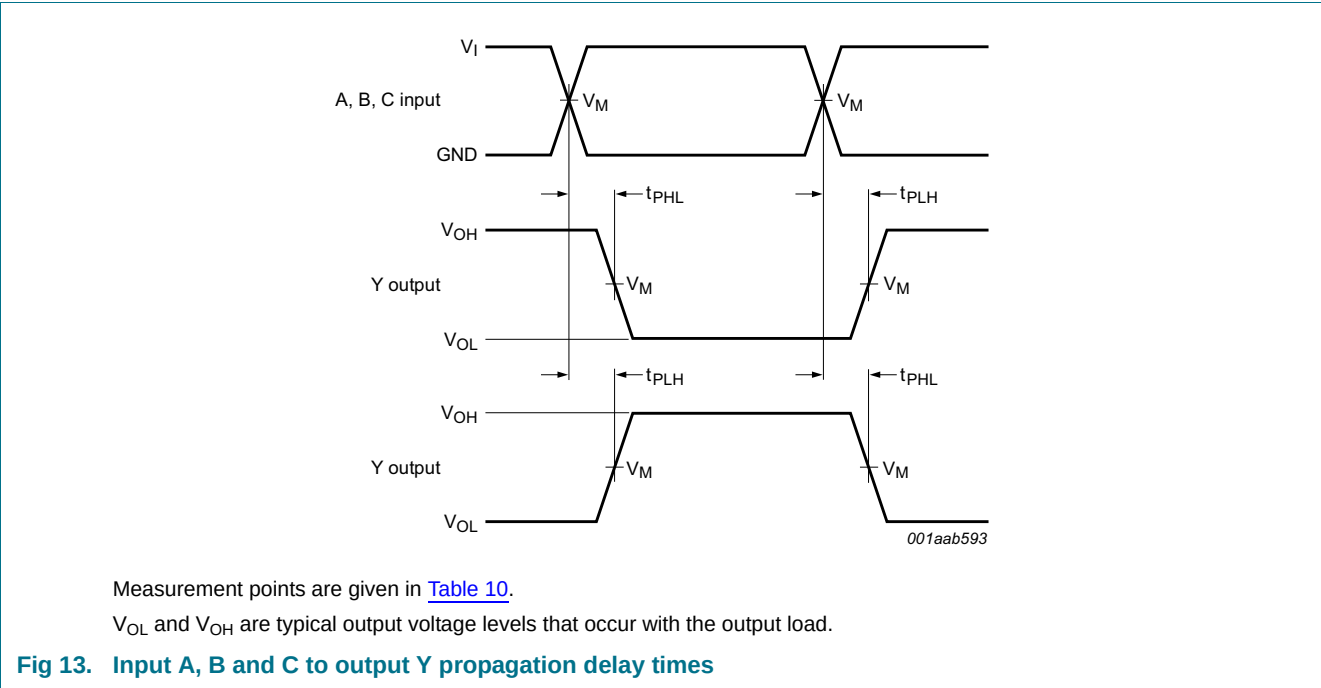


Table 10. Measurement points

Supply voltage	Input		Output
V_{CC}	V_M	V_I	V_M
1.65 V to 1.95 V	$0.5V_{CC}$	V_{CC}	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	V_{CC}	$0.5V_{CC}$
2.7 V	1.5 V	2.7 V	1.5 V
3.0 V to 3.6 V	1.5 V	2.7 V	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	V_{CC}	$0.5V_{CC}$

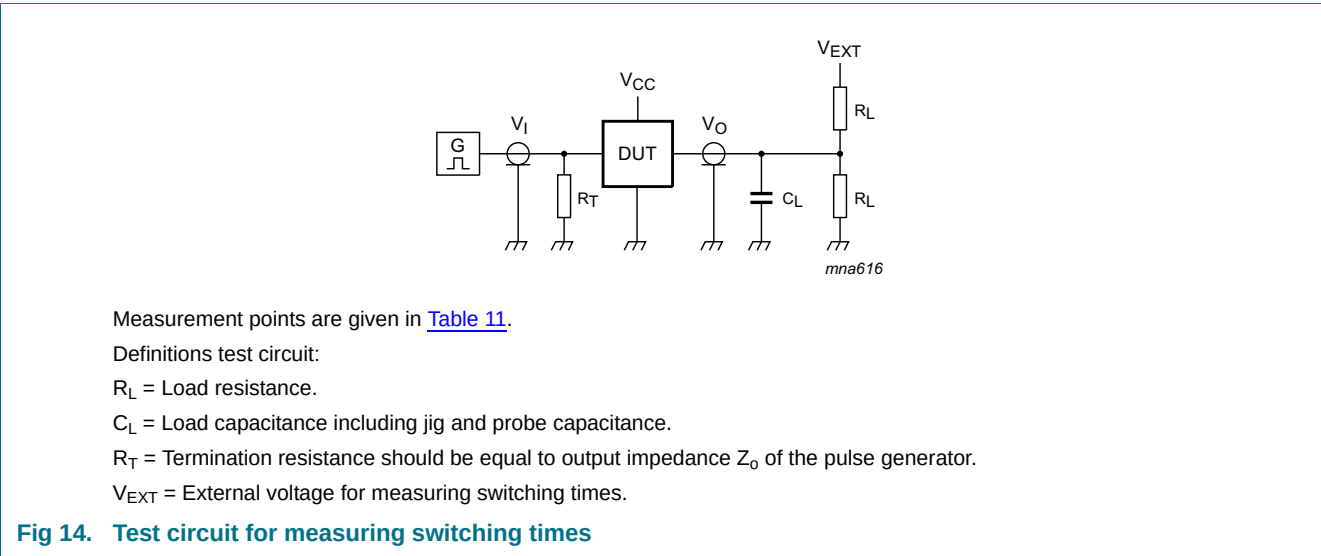


Table 11. Measurement points

Supply voltage	Input		Load		V _{EXT}
V _{CC}	V _I	t _r = t _f	C _L	R _L	t _{PLH} , t _{PHL}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open

13. Transfer characteristics

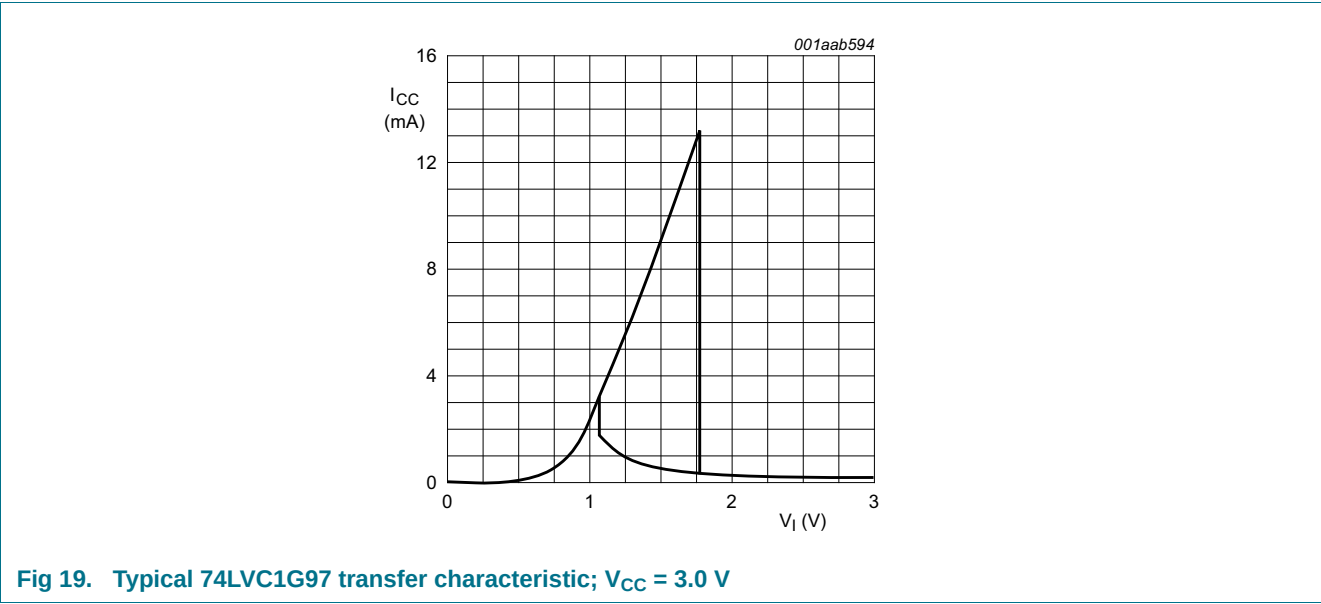
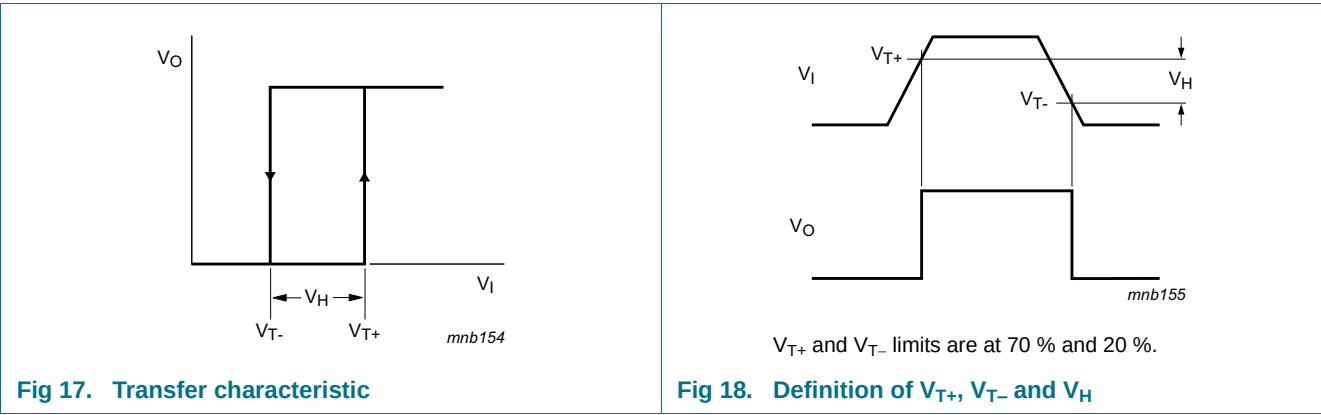
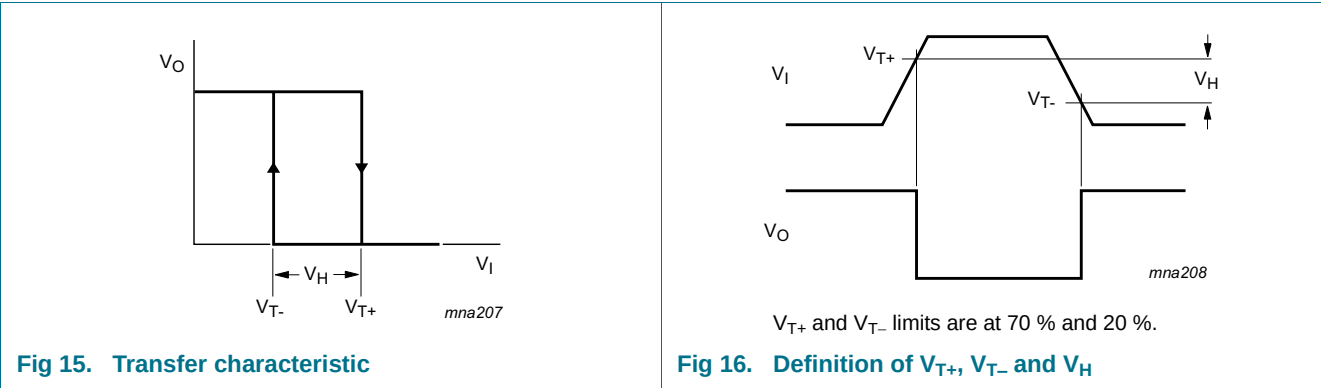
Table 12. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{T+}	positive-going threshold voltage	see Figure 15 , Figure 16 , Figure 17 and Figure 18						
		V _{CC} = 1.8 V	0.70	1.02	1.20	0.67	1.20	V
		V _{CC} = 2.3 V	1.11	1.42	1.60	1.08	1.60	V
		V _{CC} = 3.0 V	1.50	1.79	2.00	1.47	2.00	V
		V _{CC} = 4.5 V	2.16	2.52	2.74	2.13	2.74	V
		V _{CC} = 5.5 V	2.61	2.99	3.33	2.58	3.33	V
V _{T–}	negative-going threshold voltage	see Figure 15 , Figure 16 , Figure 17 and Figure 18						
		V _{CC} = 1.8 V	0.30	0.53	0.72	0.30	0.75	V
		V _{CC} = 2.3 V	0.58	0.77	1.00	0.58	1.03	V
		V _{CC} = 3.0 V	0.80	1.04	1.30	0.80	1.33	V
		V _{CC} = 4.5 V	1.21	1.55	1.90	1.21	1.93	V
		V _{CC} = 5.5 V	1.45	1.86	2.29	1.45	2.32	V
V _H	hysteresis voltage	(V _{T+} – V _{T–}). See Figure 15 , Figure 16 , Figure 17 and Figure 18						
		V _{CC} = 1.8 V	0.30	0.48	0.62	0.23	0.62	V
		V _{CC} = 2.3 V	0.40	0.64	0.80	0.34	0.80	V
		V _{CC} = 3.0 V	0.50	0.75	1.00	0.44	1.00	V
		V _{CC} = 4.5 V	0.71	0.97	1.20	0.65	1.20	V
		V _{CC} = 5.5 V	0.71	1.13	1.40	0.65	1.40	V

[1] Typical values are measured at T_{amb} = 25 °C.

14. Waveforms transfer characteristics



15. Package outline

Plastic surface-mounted package; 6 leads

SOT363

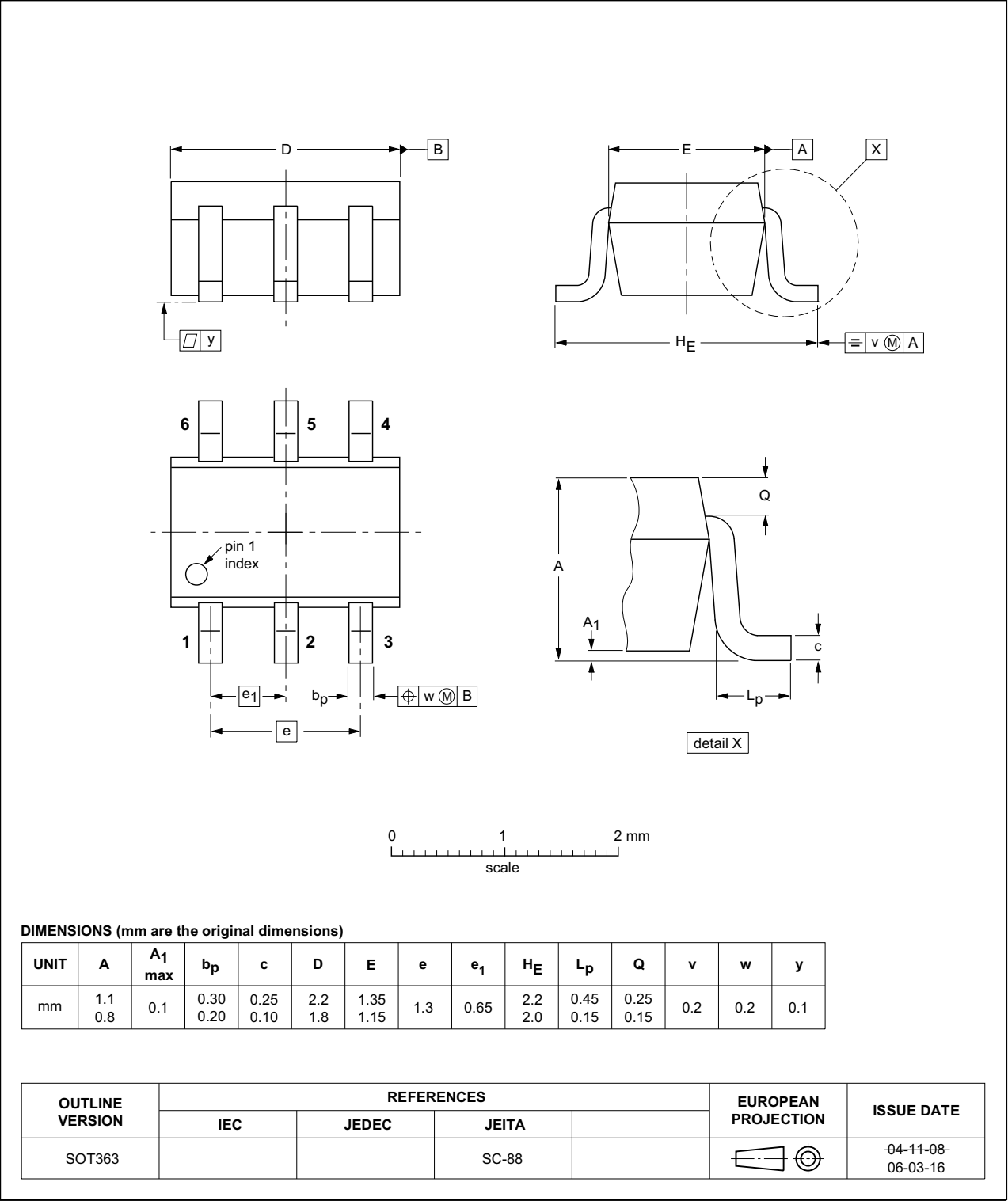


Fig 20. Package outline SOT363 (SC-88)

Plastic surface-mounted package (TSOP6); 6 leads

SOT457

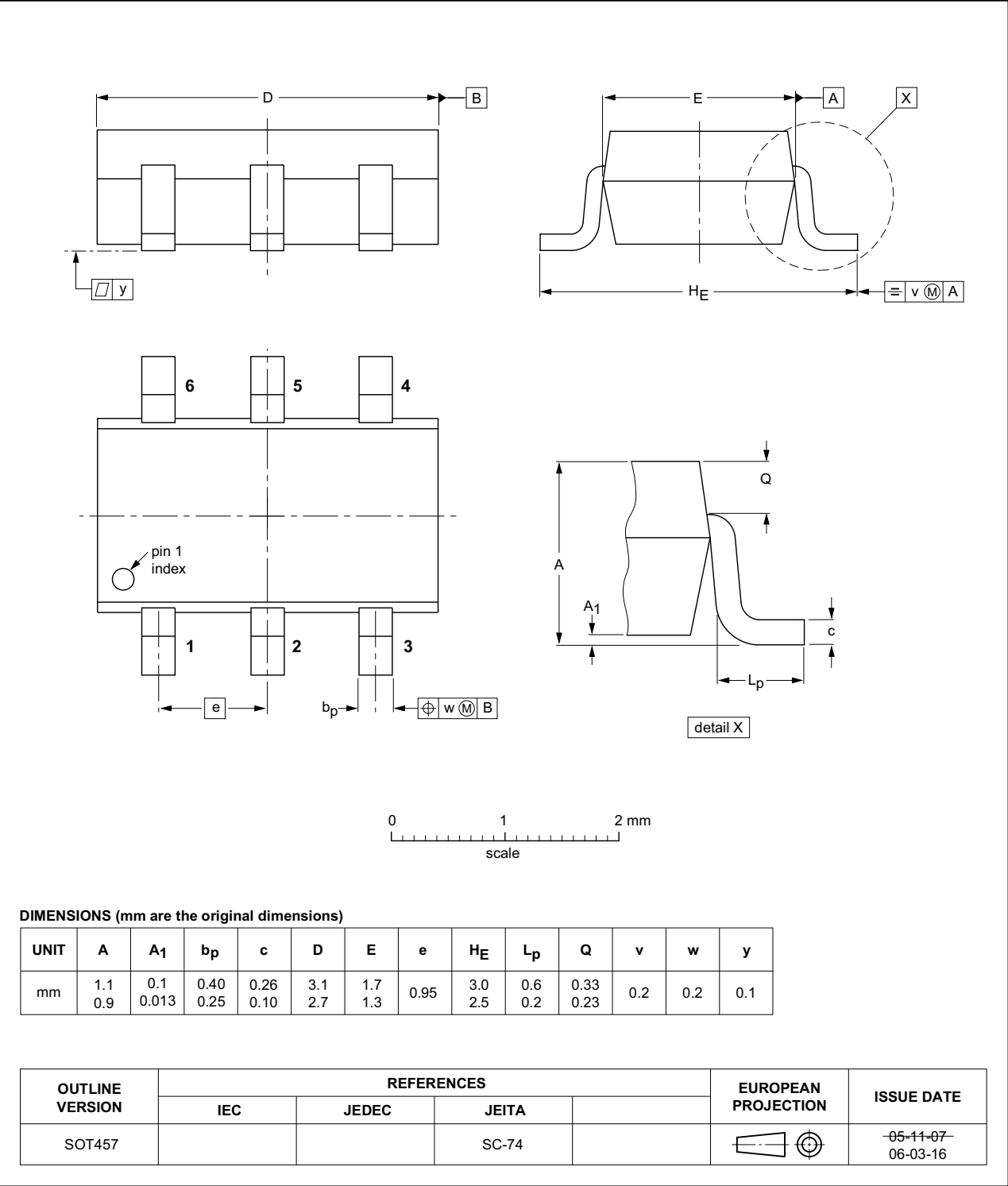


Fig 21. Package outline SOT457 (SC-74)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

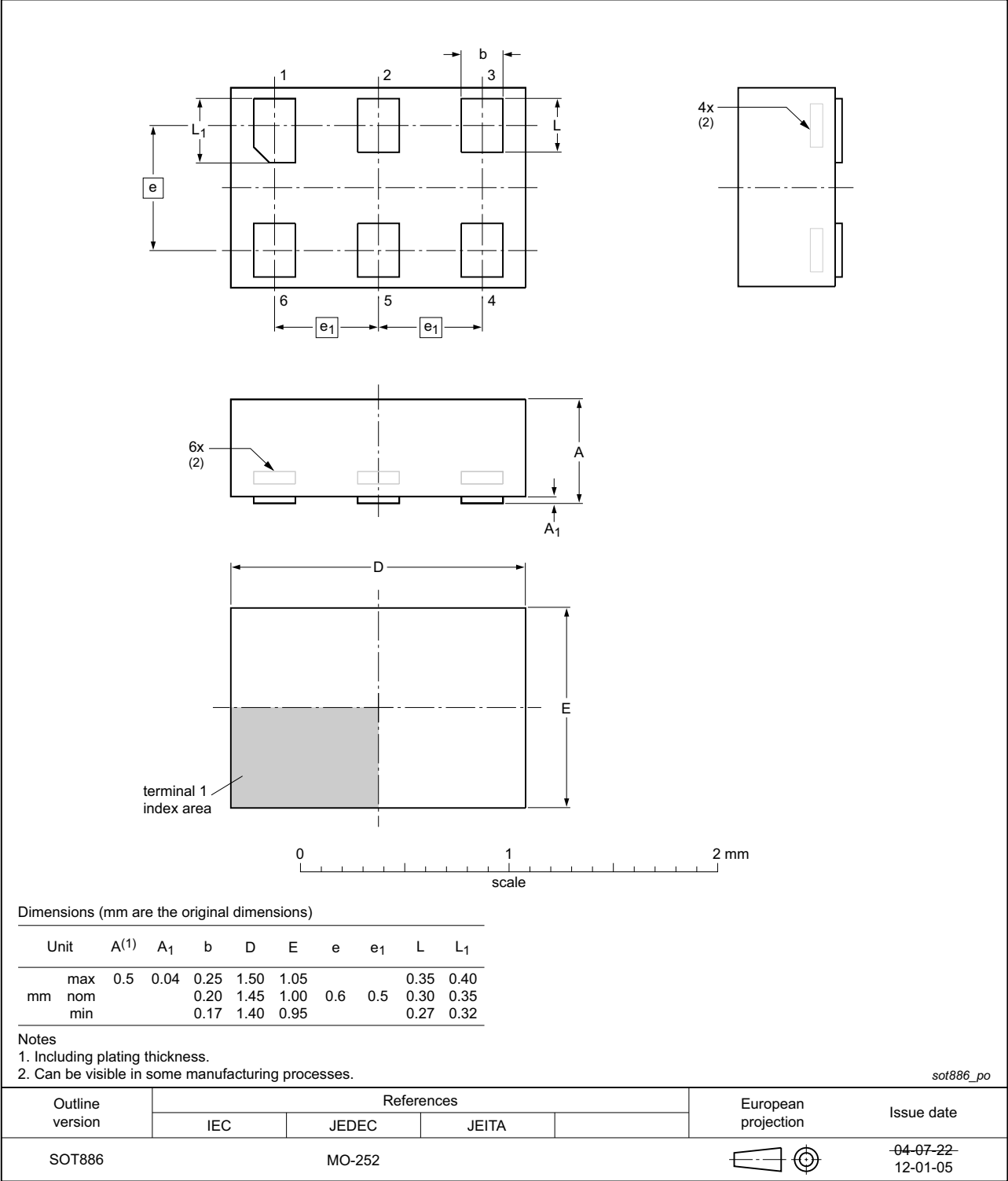


Fig 22. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm

SOT891

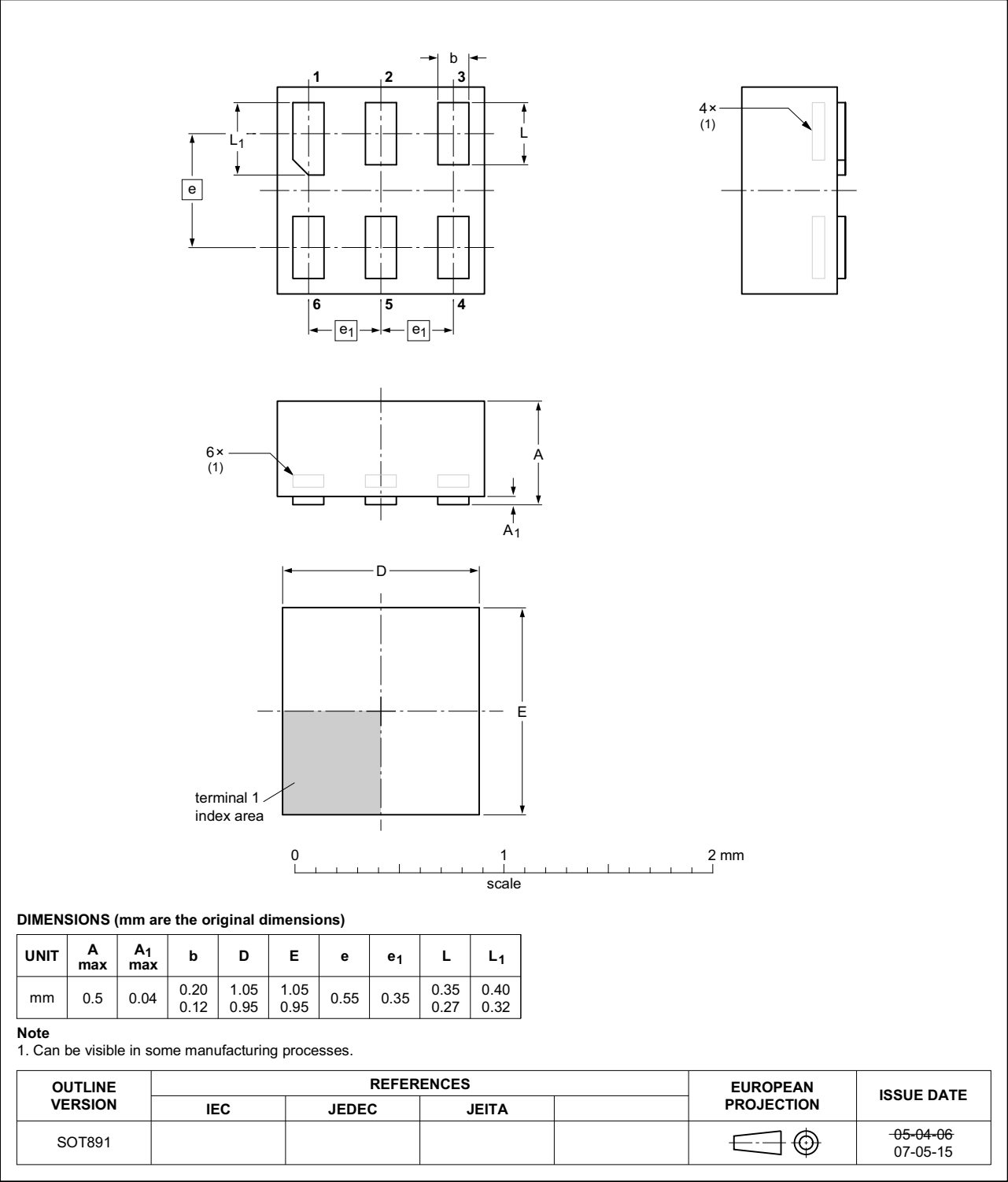


Fig 23. Package outline SOT891 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm

SOT1115

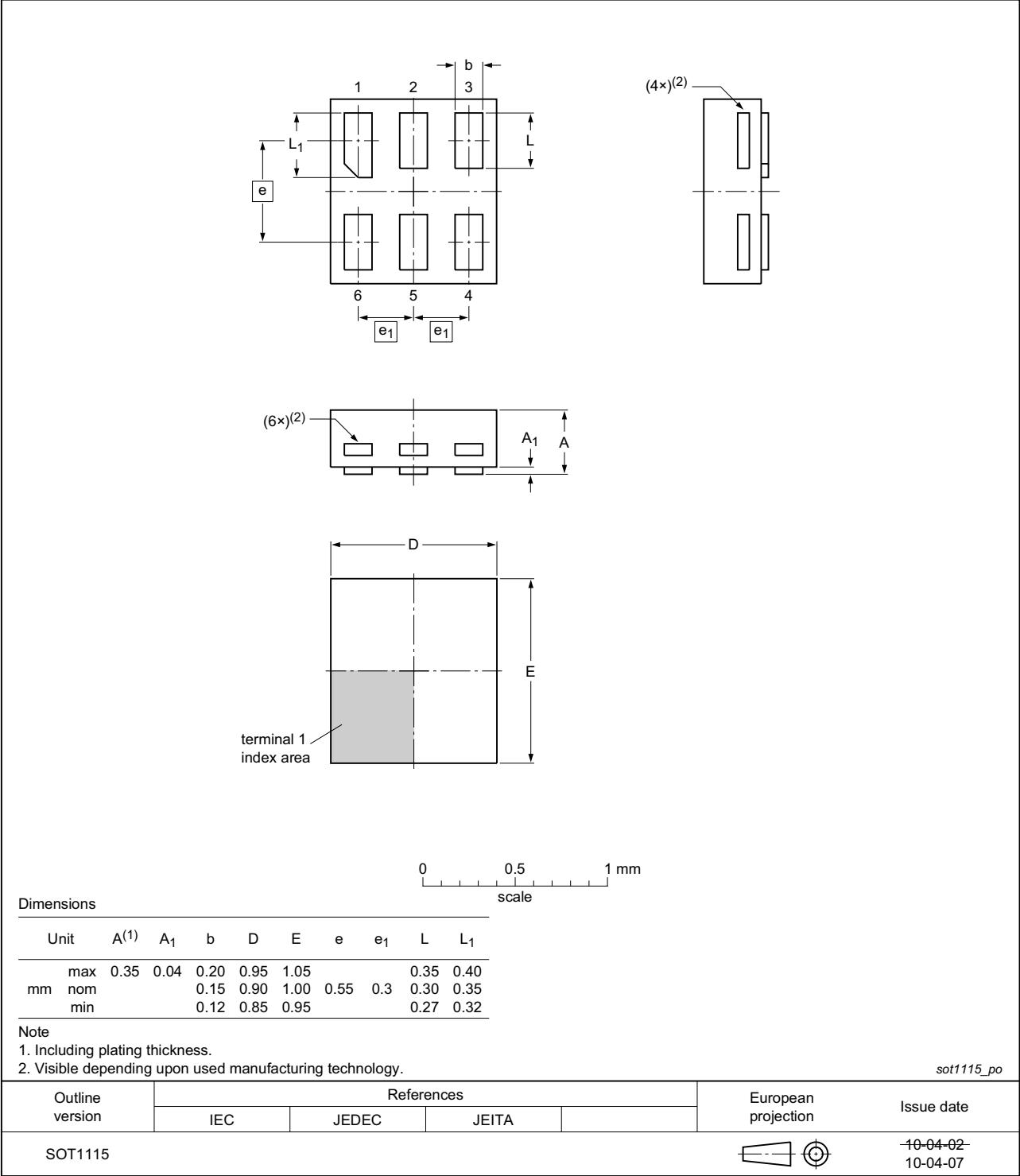
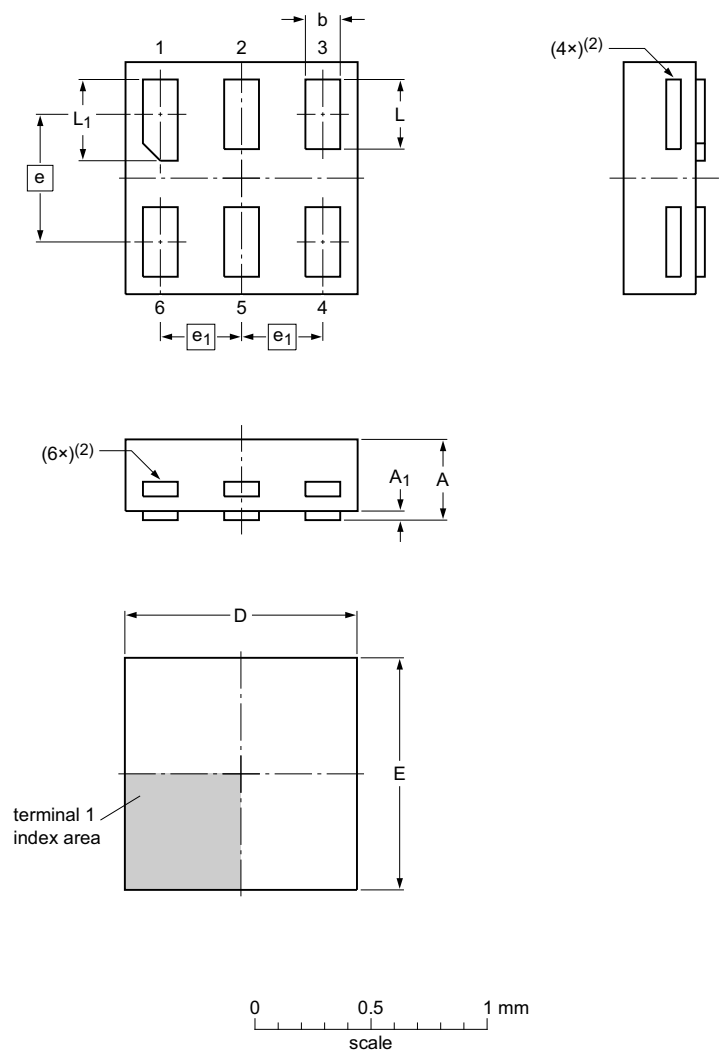


Fig 24. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm

SOT1202



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max	0.35	0.04	0.20	1.05	1.05		0.35	0.40
	nom			0.15	1.00	1.00	0.55	0.30	0.35
	min			0.12	0.95	0.95		0.27	0.32

Note

- 1. Including plating thickness.
- 2. Visible depending upon used manufacturing technology.

sot1202_po

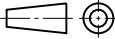
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						10-04-02 10-04-06

Fig 25. Package outline SOT1202 (XSON6)

X2SON6: plastic thermal enhanced extremely thin small outline package; no leads;
6 terminals; body 1.0 x 0.8 x 0.35 mm

SOT1255

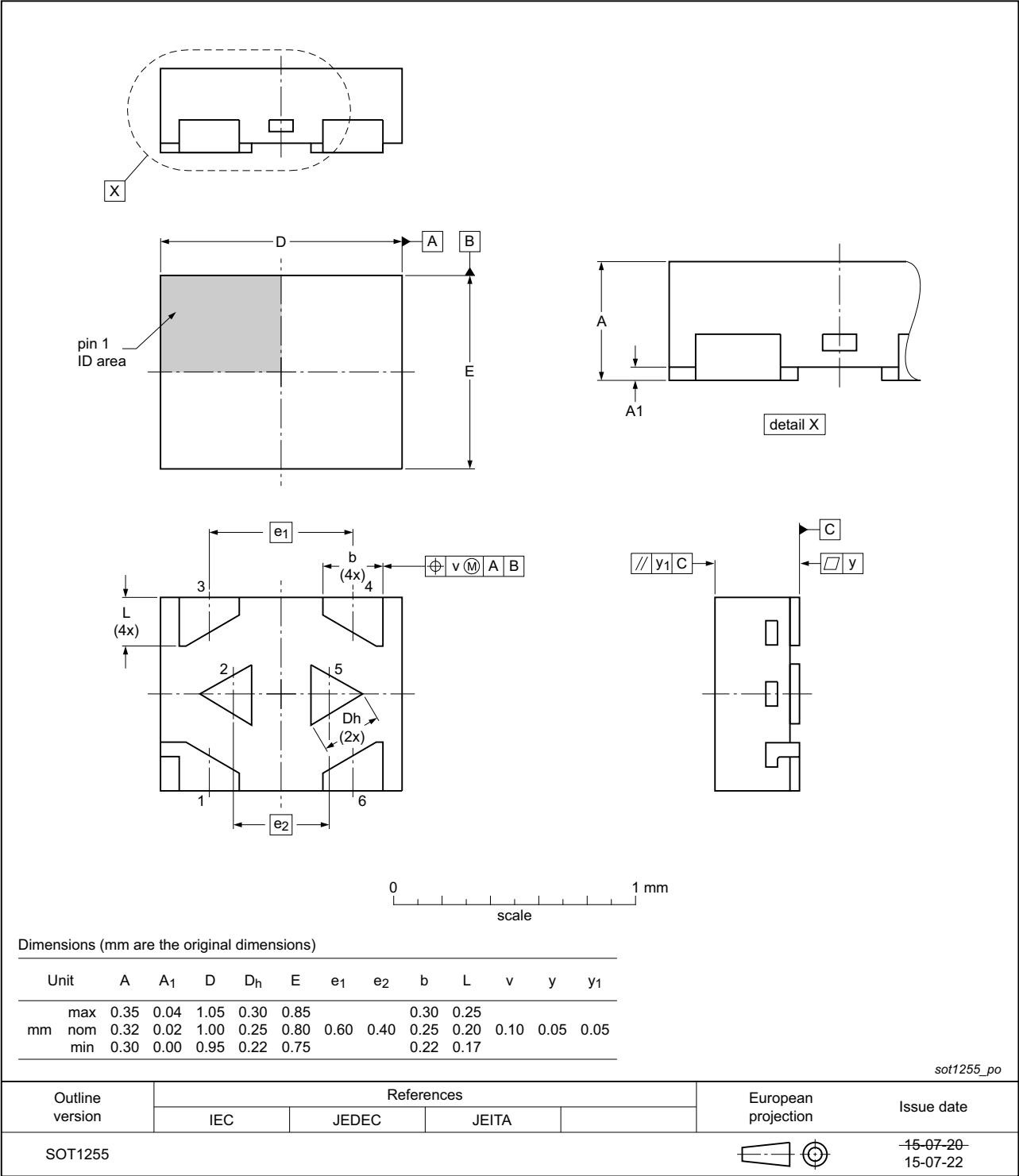


Fig 26. Package outline SOT1255 (X2SON6)

16. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
TTL	Transistor-Transistor Logic
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
DUT	Device Under Test

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G97 v.5	20161212	Product data sheet	-	74LVC1G97 v.4
Modifications:	Table 8: The maximum limits for leakage current and supply current have changed. - Type number 74LVC1G97GX (X2SON6/SOT1255) added.			
74LVC1G97 v.4	20140910	Product data sheet	-	74LVC1G97 v.3
Modifications:	Package outline drawing of SOT886 (Figure 22) modified.			
74LVC1G97 v.3	20111207	Product data sheet	-	74LVC1G97 v.2
74LVC1G97 v.2	20110309	Product data sheet	-	74LVC1G97 v.1
74LVC1G97 v.1	20101221	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 12 December 2016

Document identifier: 74LVC1G97