

DATA SHEET

74LVT32374

**3.3 V 32-bit edge-triggered D-type
flip-flop; 3-state**

Product specification
Supersedes data of 2002 Mar 20

2004 Oct 15

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FEATURES

- 32-bit edge-triggered flip-flop
- 3-state buffers
- Output capability: +64 mA/-32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection exceeds 500 mA in accordance with JEDEC std 17
- ESD protection exceeds 2000 V in accordance with MIL STD 883 method 3015 and 200 V in accordance with machine model.

DESCRIPTION

The 74LVT32374 is a high-performance BICMOS product designed for V_{CC} operation at 3.3 V.

The 74LVT32374 is a 32-bit edge-triggered D-type flip-flop featuring non-inverting 3-state outputs. The device can be used as four 8-bit flip-flops, or two 16-bit flip-flops or one 32-bit flip-flop. On the positive transition of the clock (CP), the Q outputs of the flip-flop take on the logic levels set-up at the D inputs.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f \leq 2.5\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nCP to nQ _n	$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	2.9	ns
C_I	input capacitance	$V_I = 0\text{ V}$ or 3.0 V	3	pF
C_O	output capacitance	outputs disabled; $V_O = 0\text{ V}$ or 3.0 V	9	pF
I_{CCZ}	total supply current	output disabled; $V_{CC} = 3.6\text{ V}$	140	μA

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FUNCTION TABLE

See note 1.

OPERATING MODE	INPUT			INTERNAL REGISTER	OUTPUT
	nOE	nCP	nD _n		nQ _n
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Hold	L	↑ +	X	NC	NC
Disable outputs	H	↑ +	X	NC	Z
	H	↑	nD _n	nD _n	Z

Note

1. H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW OE transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW OE transition;
NC = not connected;
X = don't care;
Z = high-impedance OFF-state;
↑ = LOW-to-HIGH CP transition;
↑
+ = not a LOW-to-HIGH CP transition.

ORDERING INFORMATION

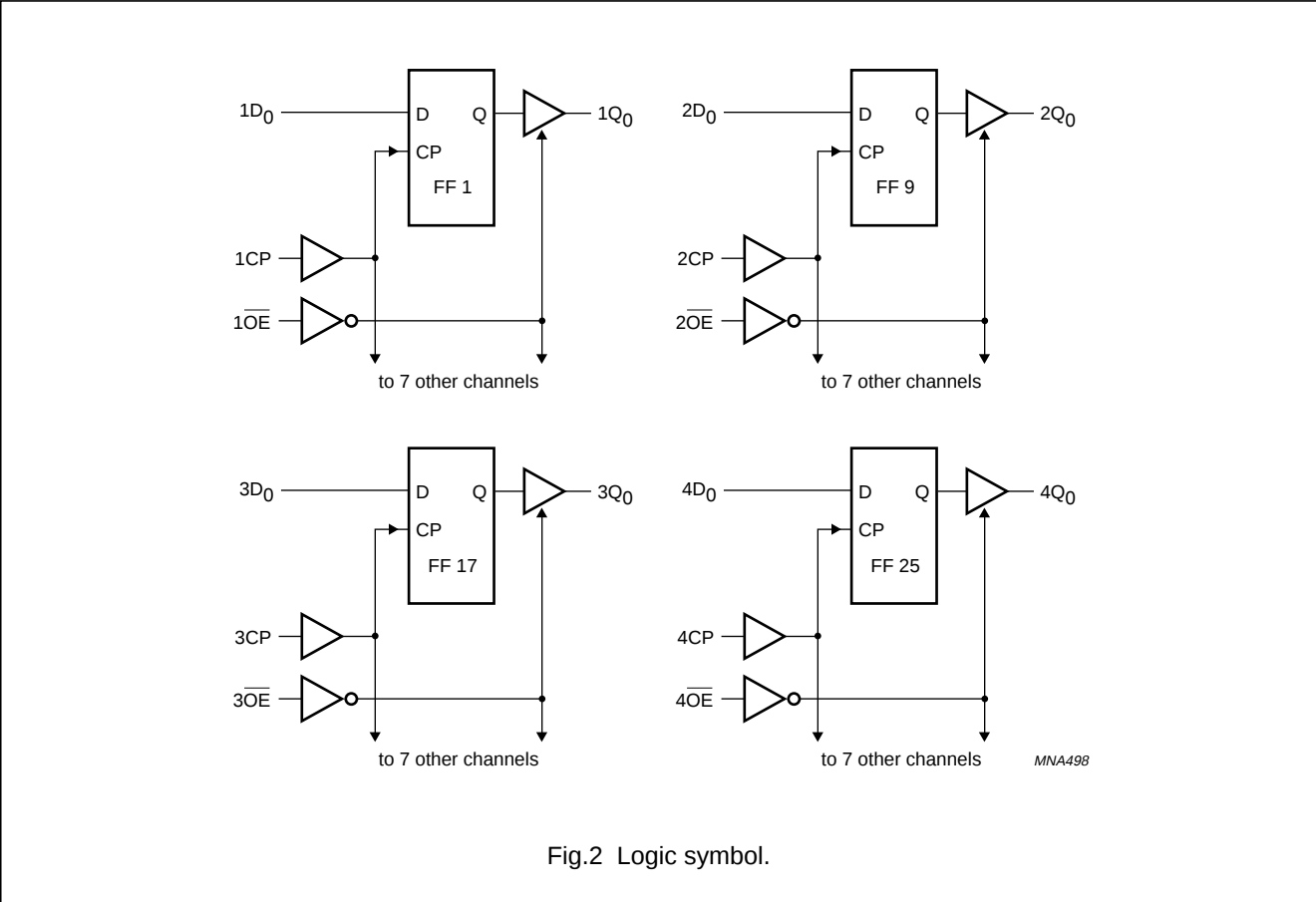
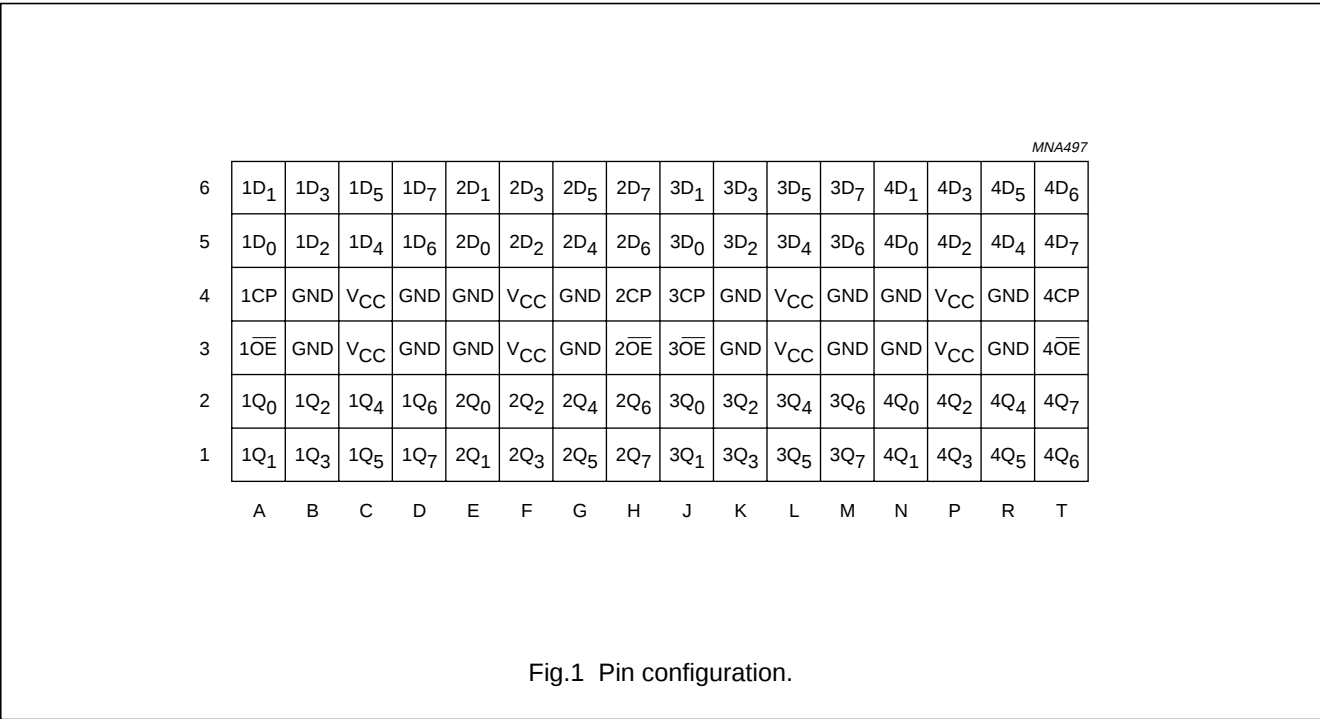
TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVT32374EC	−40 °C to +85 °C	96	LFBGA96	plastic	SOT536-1

PINNING

SYMBOL	DESCRIPTION
nD _n	data input
nCP	clock input
nQ _n	flip-flop output
GND	ground (0 V)
nOE	output enable input (active LOW)
V _{CC}	supply voltage

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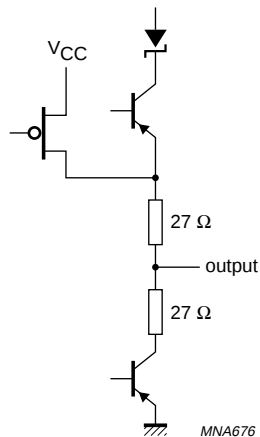


Fig.3 Schematic of each output.

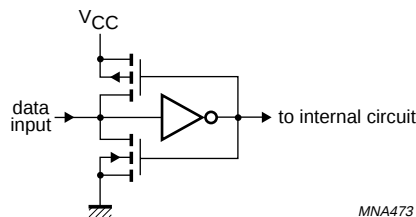


Fig.4 Bus hold circuit.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage		2.7	+3.6	V
V _I	input voltage	note 1	0	5.5	V
V _{IH}	HIGH-level input voltage		2.0	–	V
V _{IL}	LOW-level input voltage		–	0.8	V
I _{OH}	HIGH-level output current		–	–32	mA
I _{OL}	LOW-level output current		–	32	mA
		current duty cycle ≤ 50 %; f ≥ 1 kHz	–	64	mA
Δt/ΔV	input transition rise or fall times	outputs enabled	–	10	ns/V
T _{amb}	ambient temperature		–40	+85	°C
P _{tot}	power dissipation per package	note 2	–	1000	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		-0.5	–	+4.6	V
I_{IK}	input diode current	$V_I < 0$ V	–	-50	–	mA
V_I	input voltage	note 2	-0.5	–	+7.0	V
I_{OK}	output diode current		–	-50	–	mA
V_O	output voltage	output in OFF or HIGH state; note 2	-0.5	–	+7.0	V
I_O	output current	output in LOW state	–	128	–	mA
		output in HIGH state	–	-64	–	mA
T_{stg}	storage temperature		-65	–	+150	°C

Notes

1. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 °C to +85 °C							
V _{IK}	input clamp voltage	I _{IK} = −18 mA	2.7	−	−0.85	−1.2	V
V _{OH}	HIGH-level output voltage	I _{OH} = −32 mA	3.0	2.0	2.3	−	V
V _{OL}	LOW-level output voltage	I _{OL} = 64 mA	3.0	−	0.4	0.55	V
V _{RST}	power-up output LOW voltage	I _O = −1 mA; V _I = GND or V _{CC} ; note 2	3.6	−	0.1	0.55	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; control pins	3.6	−	0.1	±1	μA
		V _I = 5.5 V	0 or 3.6	−	0.4	10	μA
		V _I = V _{CC} ; data pins; note 3	3.6	−	0.1	1	μA
		V _I = 0 V; data pins; note 3	3.6	−	−0.4	−5	μA
I _{off}	output OFF current	V _I or V _O = 0 V to 4.5 V	0	−	0.1	±100	μA
I _{hold}	bus hold current D inputs	V _I = 0.8 V; note 4	3.0	75	135	−	μA
		V _I = 2.0 V; note 4	3.0	−75	−135	−	μA
		V _{CC} = 3.6 V; note 4	0 to 3.6	±500	−	−	μA
I _{EX}	current into an output in the HIGH state when V _O > V _{CC}	V _O = 5.5 V	3.0	−	50	125	μA
I _{pu/pd}	power-up/down 3-state output current	V _O = 5.5 V to V _{CC} ; V _I = GND or V _{CC} ; V _{OE} = don't care; note 5	≤ 1.2 V	−	1	±100	μA
I _{OZH}	3-state output HIGH current	V _O = 3.0 V; V _I = V _{IH} or V _{IL}	3.6	−	0.5	5	μA
I _{OZL}	3-state output LOW current	V _O = 0.5 V; V _I = V _{IH} or V _{IL}	3.6	−	+0.5	−5	μA
I _{CCH}	quiescent supply current	outputs HIGH; I _O = 0 A; V _I = GND or V _{CC}	3.6	−	0.14	0.24	mA
I _{CCL}	quiescent supply current	outputs LOW; I _O = 0 A; V _I = GND or V _{CC}	3.6	−	8	12	mA
I _{CCZ}	quiescent supply current	outputs disabled; I _O = 0 A; V _I = GND or V _{CC} ; note 6	3.6	−	0.14	0.24	mA
ΔI _{CC}	additional supply current per input pin	one input at V _{CC} − 0.6 V; other inputs at GND or V _{CC} ; note 7	3.0 to 3.6	−	0.1	0.2	μA

Notes

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
3. Unused pins at V_{CC} or GND.
4. This is the bus hold overdrive current required to force the input to the opposite logic state.
5. This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
7. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

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AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500 \Omega$.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T _{amb} = −40 °C to +85 °C							
t _{PLH}	propagation delay nCP to nQ _n	see Fig.5	2.7	–	–	6.2	ns
			3.0 to 3.6	1.5	3.0	5.3	ns
t _{PHL}	propagation delay nCP to nQ _n	see Fig.5	2.7	–	–	5.1	ns
			3.0 to 3.6	1.5	3.0	4.9	ns
t _{PZH}	output enable time to HIGH level	see Figs 7 and 8	2.7	–	–	6.9	ns
			3.0 to 3.6	1.5	3.5	5.6	ns
t _{PZL}	output enable time to LOW level	see Figs 7 and 8	2.7	–	–	6.0	ns
			3.0 to 3.6	1.5	3.2	4.9	ns
t _{PHZ}	output disable time from HIGH level	see Figs 7 and 8	2.7	–	–	5.7	ns
			3.0 to 3.6	1.5	3.5	5.4	ns
t _{PLZ}	output disable time from LOW level	see Figs 7 and 8	2.7	1.5	3.2	5.1	ns
			3.0 to 3.6	1.5	3.2	5.0	ns
t _{suH}	set-up time nD _n HIGH to nCP	see Fig.6	2.7	2.0	–	–	ns
			3.0 to 3.6	2.0	0.7	–	ns
t _{suL}	set-up time nD _n LOW to nCP	see Fig.6	2.7	2.0	–	–	ns
			3.0 to 3.6	2.0	0.7	–	ns
t _{hH}	hold time nD _n HIGH to nCP	see Fig.6	2.7	0.1	–	–	ns
			3.0 to 3.6	0.8	0	–	ns
t _{hL}	hold time nD _n LOW to nCP	see Fig.6	2.7	0.1	–	–	ns
			3.0 to 3.6	0.8	0	–	ns
t _{WH}	nCP HIGH pulse width	see Fig.6	2.7	1.5	–	–	ns
			3.0 to 3.6	1.5	0.6	–	ns
t _{WL}	nCP LOW pulse width	see Fig.6	2.7	3.0	–	–	ns
			3.0 to 3.6	3.0	1.6	–	ns
f _{max}	maximum clock pulse frequency	see Fig.5	3.0 to 3.6	150	–	–	MHz

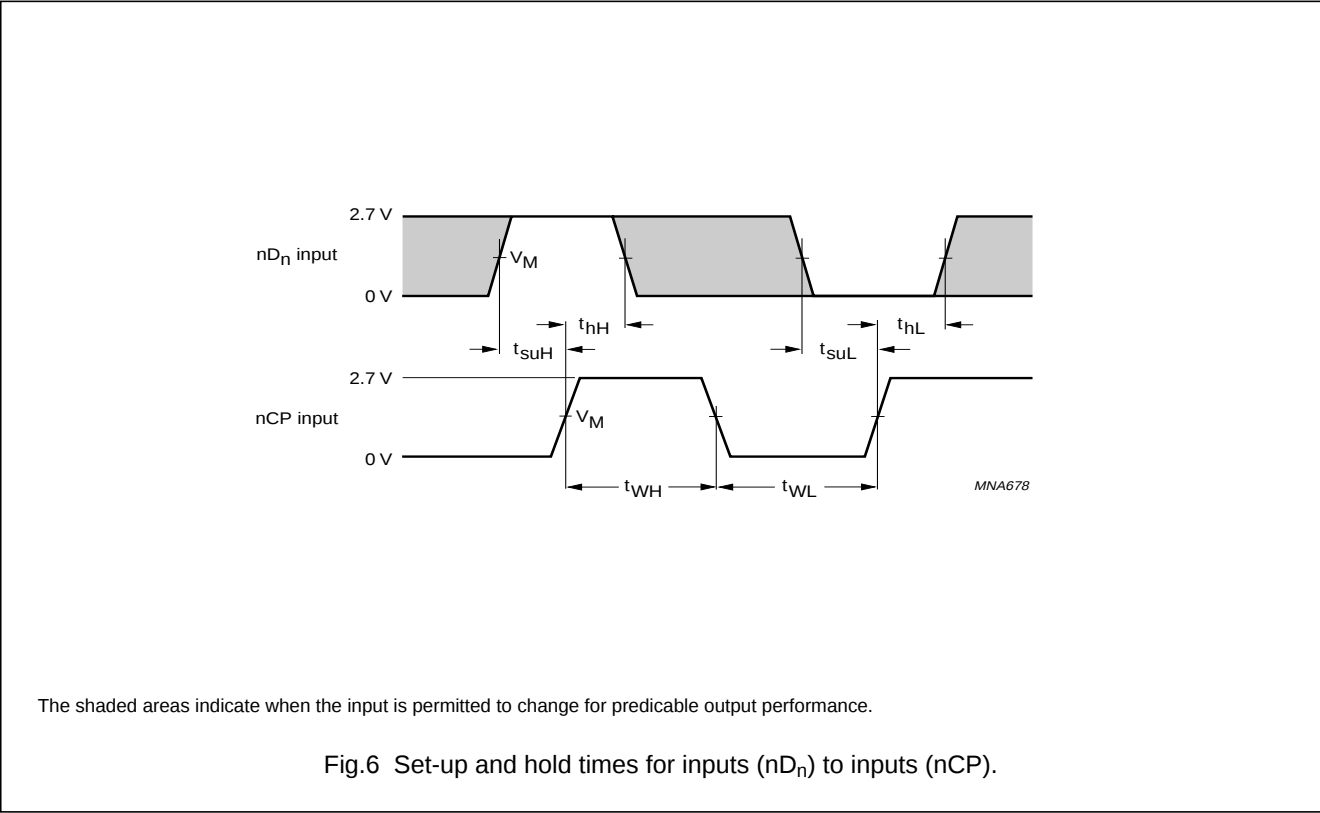
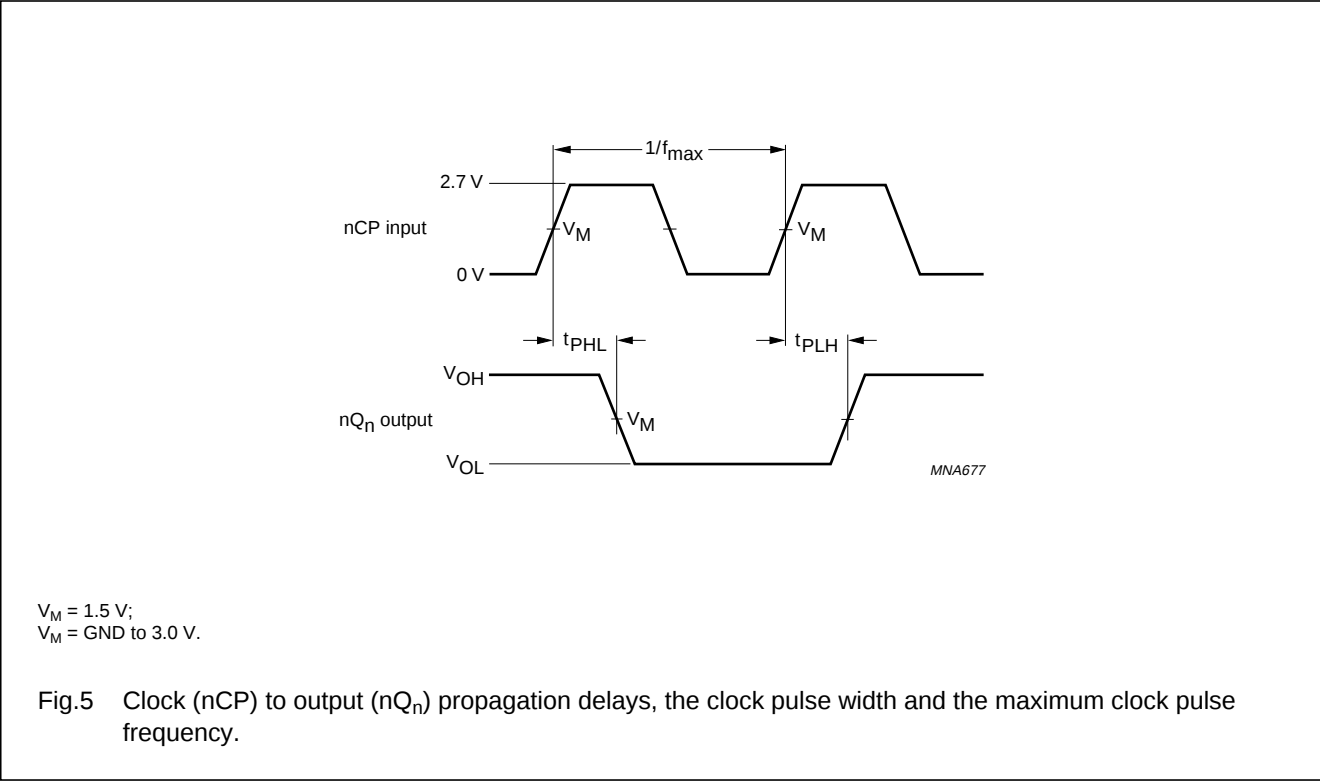
Note

1. All typical values are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.

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AC WAVEFORMS



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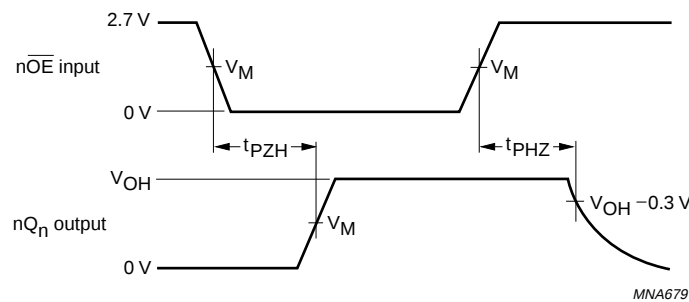


Fig.7 3-state output enable time to HIGH level and output disable time from HIGH level.

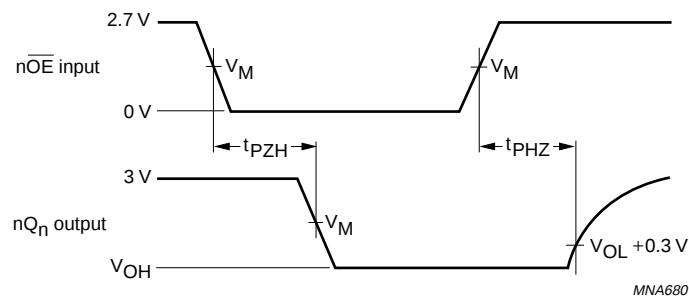
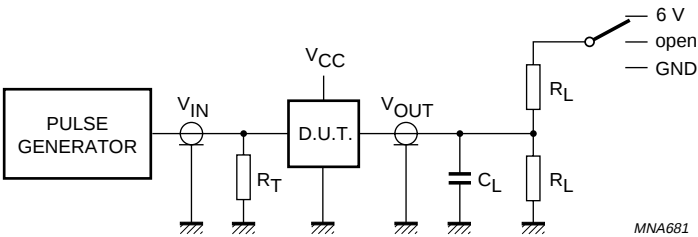


Fig.8 3-state output enable time to LOW level and output disable time from LOW level.

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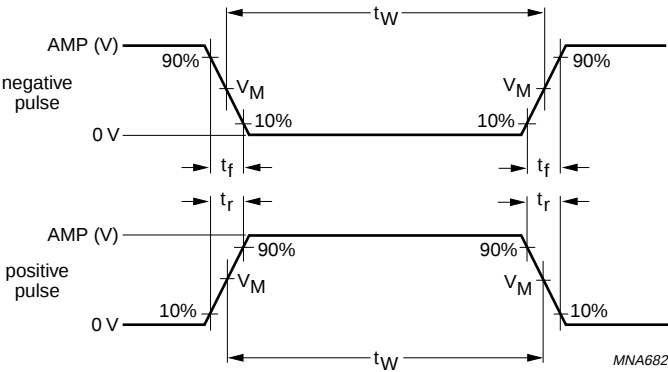
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TEST	SWITCH
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
 R_L = Load resistor.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.9 Load circuitry for switching times.



INPUT PULSE REQUIREMENTS				
AMPLITUDE	PULSE RATE	t_w	t_r	t_f
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	≤ 2.5 ns

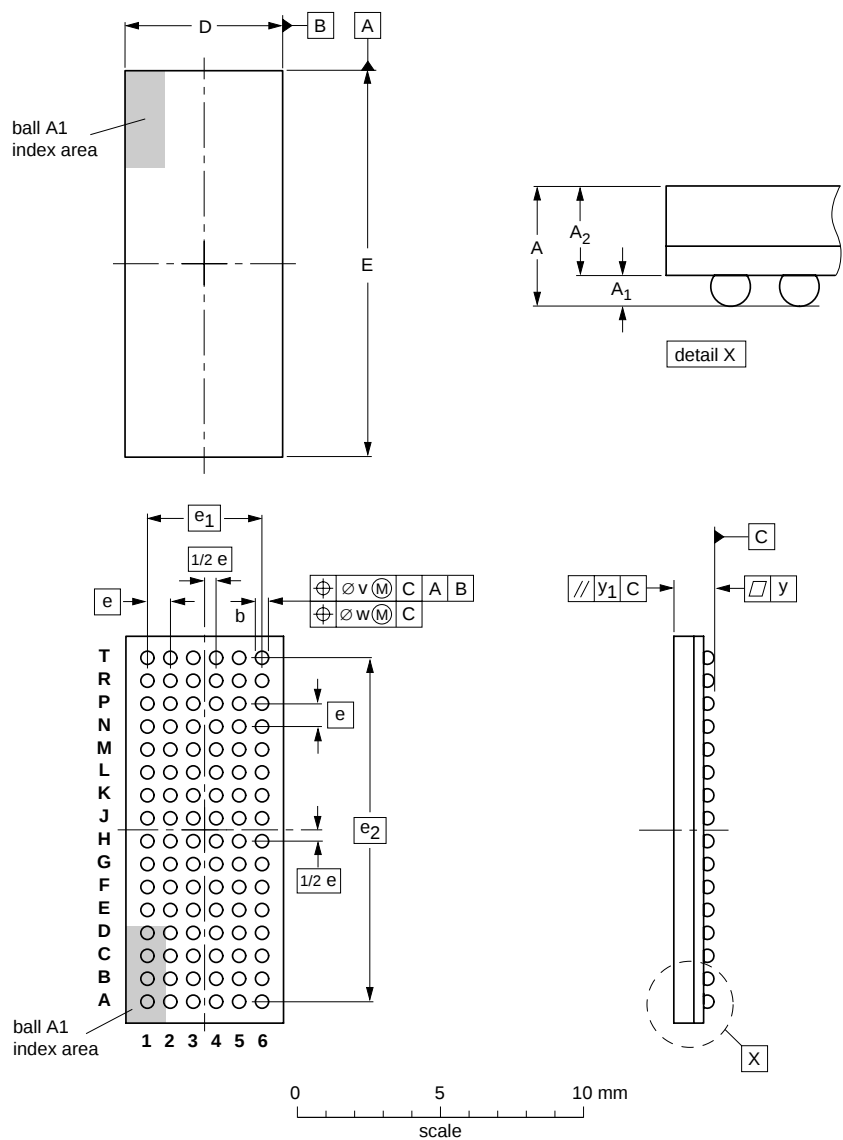
Fig.10 Input pulse definition.

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PACKAGE OUTLINE

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	b	D	E	e	e ₁	e ₂	v	w	y	y ₁
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	4	12	0.15	0.1	0.1	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT536-1						00-03-04 03-02-05

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