

74LVT374

3.3 V octal D-type flip-flop; 3-state

Rev. 3 — 14 September 2011

Product data sheet

1. General description

The 74LVT374 is a high-performance product designed for V_{CC} operation at 3.3 V.

This device is an 8-bit, edge triggered register coupled to eight 3-state output buffers. The two sections of the device are controlled independently by the clock (pin CP) and output enable (pin $\overline{OE}$) control gates. The state of each Dn input (one setup time before the LOW-to-HIGH clock transition) is transferred to the corresponding flip-flops Qn output.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors.

The active LOW output enable (pin $\overline{OE}$) controls all eight 3-state buffers independent of the clock operation.

When pin $\overline{OE}$ is LOW, the stored data appears at the outputs. When pin $\overline{OE}$ is HIGH, the outputs are in the high-impedance OFF-state, which means they will neither drive nor load the bus.

2. Features and benefits

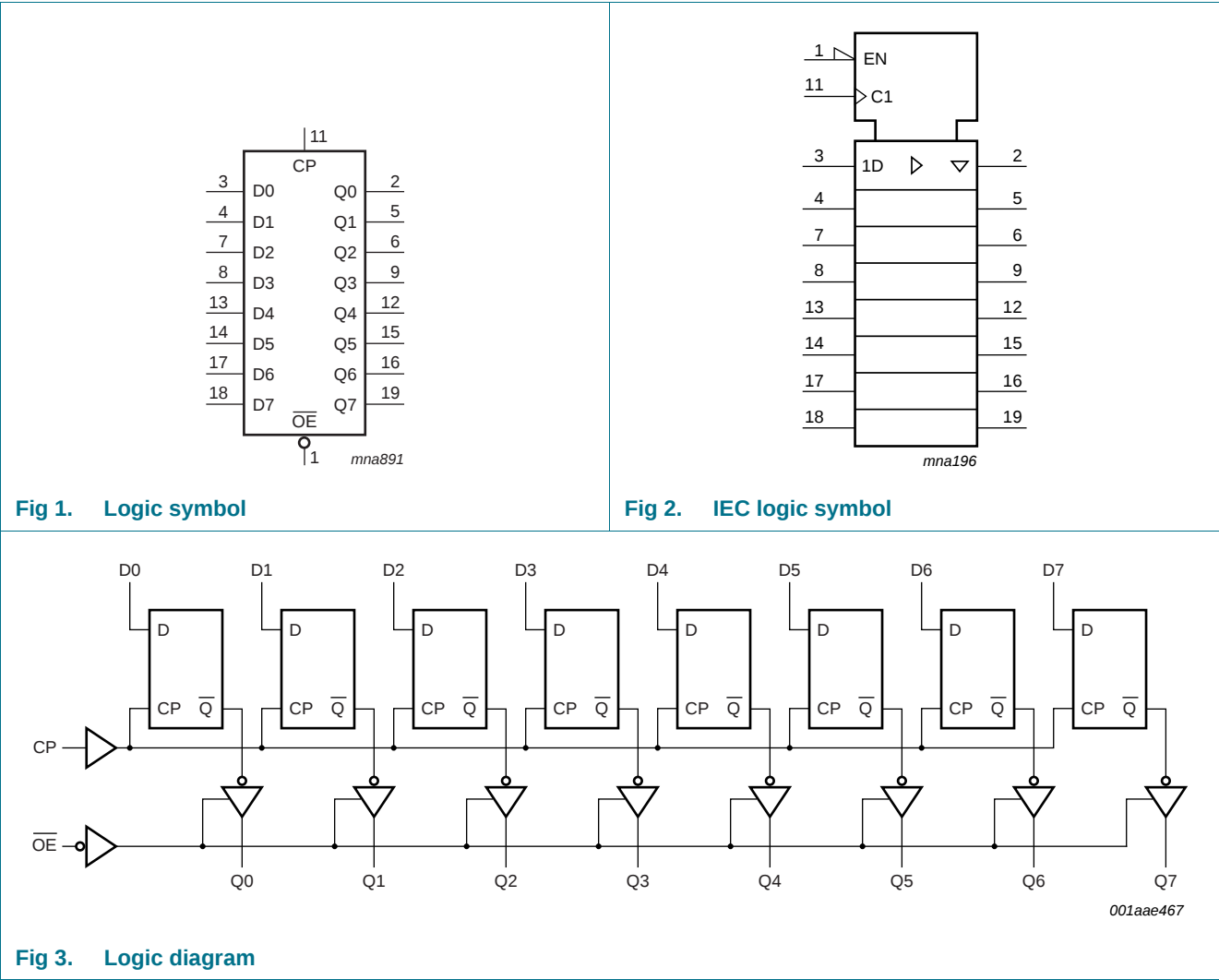
- Inputs and outputs arranged for easy interfacing to microprocessors
- 3-state outputs for bus interfacing
- Common output enable control
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up reset
- Power-up 3-state
- Latch-up protection
 - ◆ JESD78 class II exceeds 500 mA
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$



3. Ordering information

Table 1. Ordering information				
Type number	Package			
	Temperature range	Name	Description	Version
74LVT374D	−40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT374DB	−40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVT374PW	−40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram



5. Pinning information

5.1 Pinning

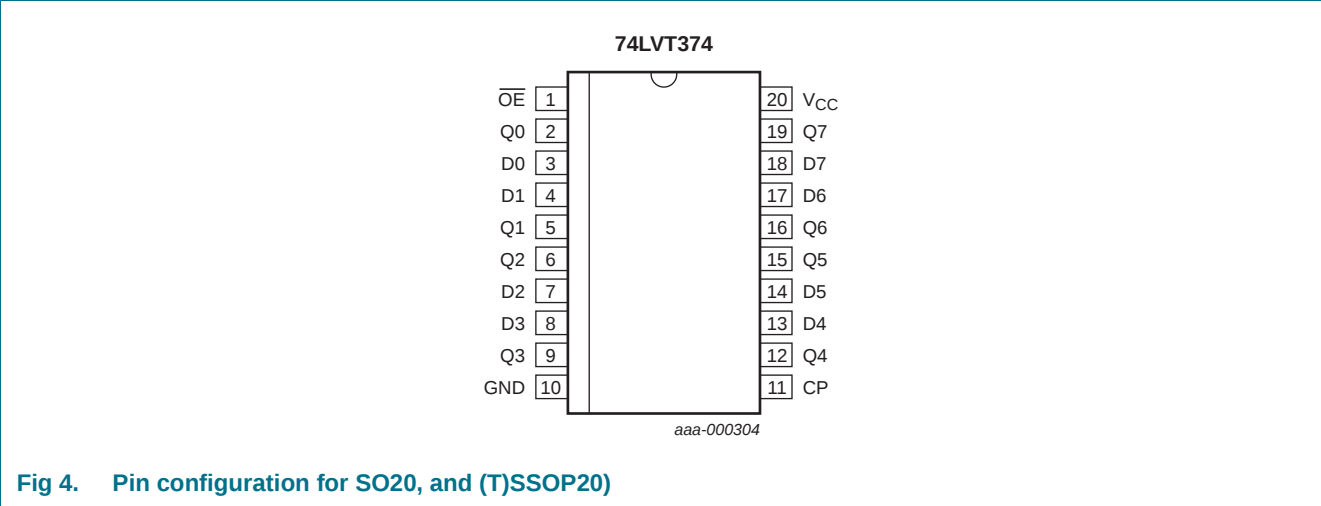


Fig 4. Pin configuration for SO20, and (T)SSOP20)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	output enable input (active LOW)
D0 to D7	3, 4, 7, 8, 13, 14, 17, 18	data input
GND	10	ground (0 V)
CP	11	clock pulse input (active rising edge)
Q0 to Q7	2, 5, 6, 9, 12, 15, 16, 19	data output
V_{CC}	20	supply voltage

6. Functional description

6.1 Function table

Table 3. Function table [1]

Operating mode	Control		Input	Internal register	Output
	OE	CP	Dn		Qn
Load and read register	L	$\uparrow$	L	L	L
			h	H	H
Hold	L	NC	X	NC	NC
Disable outputs	H	L or H	X	NC	Z
		$\uparrow$	Dn	Dn	Z

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 $\uparrow$ = LOW-to-HIGH clock transition;
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition;
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition;
 Z = high-impedance OFF-state;
 NC = no change;
 X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage		[1] -0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-	-50	mA
I_{OK}	output clamping current	$V_O < 0$ V	-	-50	mA
I_O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		[2] -	150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C	[3] -	500	mW

- [1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
 [3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.
 For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.
 For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		2.7	3.6	V
V _I	input voltage		0	5.5	V
V _{IH}	HIGH-level input voltage		2.0	-	V
V _{IL}	LOW-level input voltage		-	0.8	V
I _{OH}	HIGH-level output current		-	-32	mA
I _{OL}	LOW-level output current		-	32	mA
		current duty cycle ≤ 50 %; f _i ≥ 1 kHz	-	64	mA
T _{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
V _{IK}	input clamping voltage	V _{CC} = 2.7 V; I _{IK} = -18 mA	-1.2	-0.9	-	V
V _{OH}	HIGH-level output voltage	V _{CC} = 2.7 V to 3.6 V; I _{OH} = -100 μA	V _{CC} - 0.2	V _{CC} - 0.1	-	V
		V _{CC} = 2.7 V; I _{OH} = -8 mA	2.4	2.5	-	V
		V _{CC} = 3.0 V; I _{OH} = -32 mA	2.0	2.2	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 2.7 V				
		I _{OL} = 100 μA	-	0.1	0.2	V
		I _{OL} = 24 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V				
		I _{OL} = 16 mA	-	0.25	0.4	V
		I _{OL} = 32 mA	-	0.3	0.5	V
V _{OL(pu)}	power-up LOW-level output voltage	I _{OL} = 64 mA	-	0.4	0.55	V
		V _{CC} = 3.6 V; I _O = 1 mA; V _I = GND or V _{CC} ^[2]	-	0.13	0.55	V
I _I	input leakage current	all input pins; V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	1	10	μA
		control pins; V _{CC} = 3.6 V; V _I = V _{CC} or GND	-	±0.1	±1	μA
		data pins; V _{CC} = 3.6 V ^[3]				
		V _I = V _{CC}	-	0.1	1	μA
		V _I = 0 V	-5	-1	-	μA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	1	±100	μA
I _{LO}	output leakage current	V _O = 5.5 V and V _{CC} = 3.0 V; output HIGH ^[4]	-	60	125	μA
I _{BHL}	bus hold LOW current	V _{CC} = 3.0 V; V _I = 0.8 V	75	150	-	μA
I _{BHH}	bus hold HIGH current	V _{CC} = 3.0 V; V _I = 2.0 V ^[4]	-	-150	-75	μA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 3.6; V _I = 0 V to 3.6 V ^[4]	-	-	500	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 3.6; V _I = 0 V to 3.6 V	-500	-	-	μA
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; OE = don't care ^[5]	-	1	±100	μA
I _{OZ}	OFF-state output current	V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL}				
		output HIGH: V _O = 3.0 V	-	1	5	μA
		output LOW: V _O = 0.5 V	-5	1	-	μA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A				
		outputs HIGH	-	0.13	0.19	mA
		outputs LOW	-	3	12	mA
		outputs disabled ^[6]	-	0.13	0.19	mA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 3 V to 3.6 V; one input at V _{CC} - 0.6 V and other inputs at V _{CC} or GND ^[7]	-	0.1	0.2	mA
C _I	input capacitance	V _I = 0 V or 3.0 V	-	4	-	pF
C _O	output capacitance	outputs disabled; V _O = 0 V or 3.0 V	-	7	-	pF

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

[3] Unused pins at V_{CC} or GND.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.[6] I_{CC} is measured with outputs pulled to V_{CC} or GND.[7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristicsVoltages are referenced to ground (GND = 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
t _{PLH}	LOW to HIGH propagation delay	CP to Qn; see Table 6				
		V _{CC} = 3.0 V to 3.6 V	1.7	3.2	5.1	ns
		V _{CC} = 2.7 V	-	-	5.8	ns
t _{PHL}	HIGH to LOW propagation delay	CP to Qn; see Table 6				
		V _{CC} = 3.0 V to 3.6 V	2.2	3.5	5.2	ns
		V _{CC} = 2.7 V	-	-	5.5	ns
t _{PZH}	OFF-state to HIGH propagation delay	$\overline{\text{OE}}$ to Qn; see Figure 6				
		V _{CC} = 3.0 V to 3.6 V	1.5	3.2	5.3	ns
		V _{CC} = 2.7 V	-	-	7.3	ns

Table 7. Dynamic characteristics ...continued

Voltages are referenced to ground (GND = 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	T _{amb} = –40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
t _{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to Qn; see Figure 7				
		V _{CC} = 3.0 V to 3.6 V	2.0	3.4	5.2	ns
		V _{CC} = 2.7 V	-	-	6.1	ns
t _{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to Qn; see Figure 6				
		V _{CC} = 3.0 V to 3.6 V	1.9	4.3	6.7	ns
		V _{CC} = 2.7 V	-	-	7.1	ns
t _{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to Qn; see Figure 7				
		V _{CC} = 3.0 V to 3.6 V	2.0	3.4	5.1	ns
		V _{CC} = 2.7 V	-	-	5.1	ns
t _{su}	set-up time	Dn to CP; see Figure 8 ^[2]				
		V _{CC} = 3.0 V to 3.6 V	2.0	0.7	-	ns
		V _{CC} = 2.7 V	2.0	-	-	ns
t _h	hold time	Dn to CP; see Figure 8 ^[3]				
		V _{CC} = 3.0 V to 3.6 V	0.3	-0.5	-	ns
		V _{CC} = 2.7 V	0	-	-	ns
t _w	pulse width	CP input HIGH; see Figure 5 ^[4]				
		V _{CC} = 3.0 V to 3.6 V	1.5	0.8	-	ns
		V _{CC} = 2.7 V	1.5	-	-	ns
		CP input LOW; see Figure 5 ^[4]				
		V _{CC} = 3.0 V to 3.6 V	2.5	1.7	-	ns
		V _{CC} = 2.7 V	3.0	-	-	ns
f _{max}	maximum frequency	CP input; see Figure 5				
		V _{CC} = 3.0 V to 3.6 V	125	200	-	MHz
		V _{CC} = 2.7 V	125	-	-	MHz

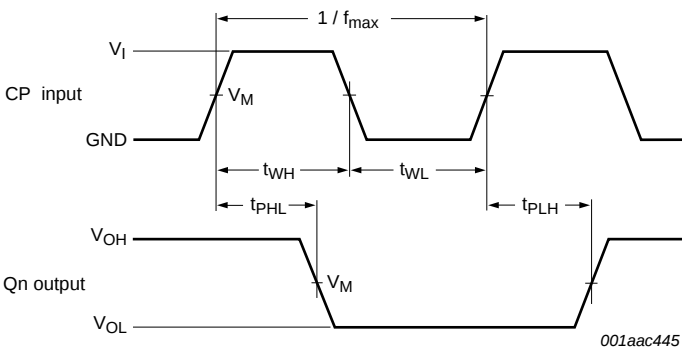
[1] Typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] t_{su} is the same as t_{su(H)} and t_{su(L)}

[3] t_h is the same as t_{h(H)} and t_{h(L)}

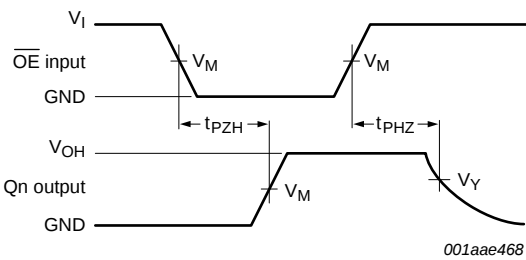
[4] t_w is the same as t_{WH} and t_{WL}

11. Waveforms



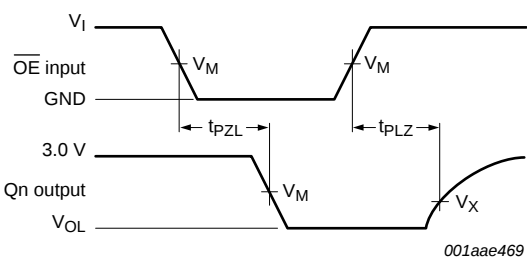
Measurement points are given in [Table 8](#)
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Propagation delay clock input (CP) to output (Qn), pulse width clock (CP) and maximum clock frequency



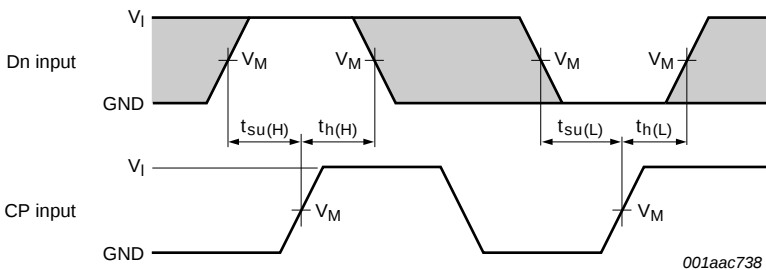
Measurement points are given in [Table 8](#)
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Output enable time to HIGH-state and output disable time from HIGH-state



Measurement points are given in [Table 8](#)
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Output enable time to LOW-state and output disable time from LOW-state

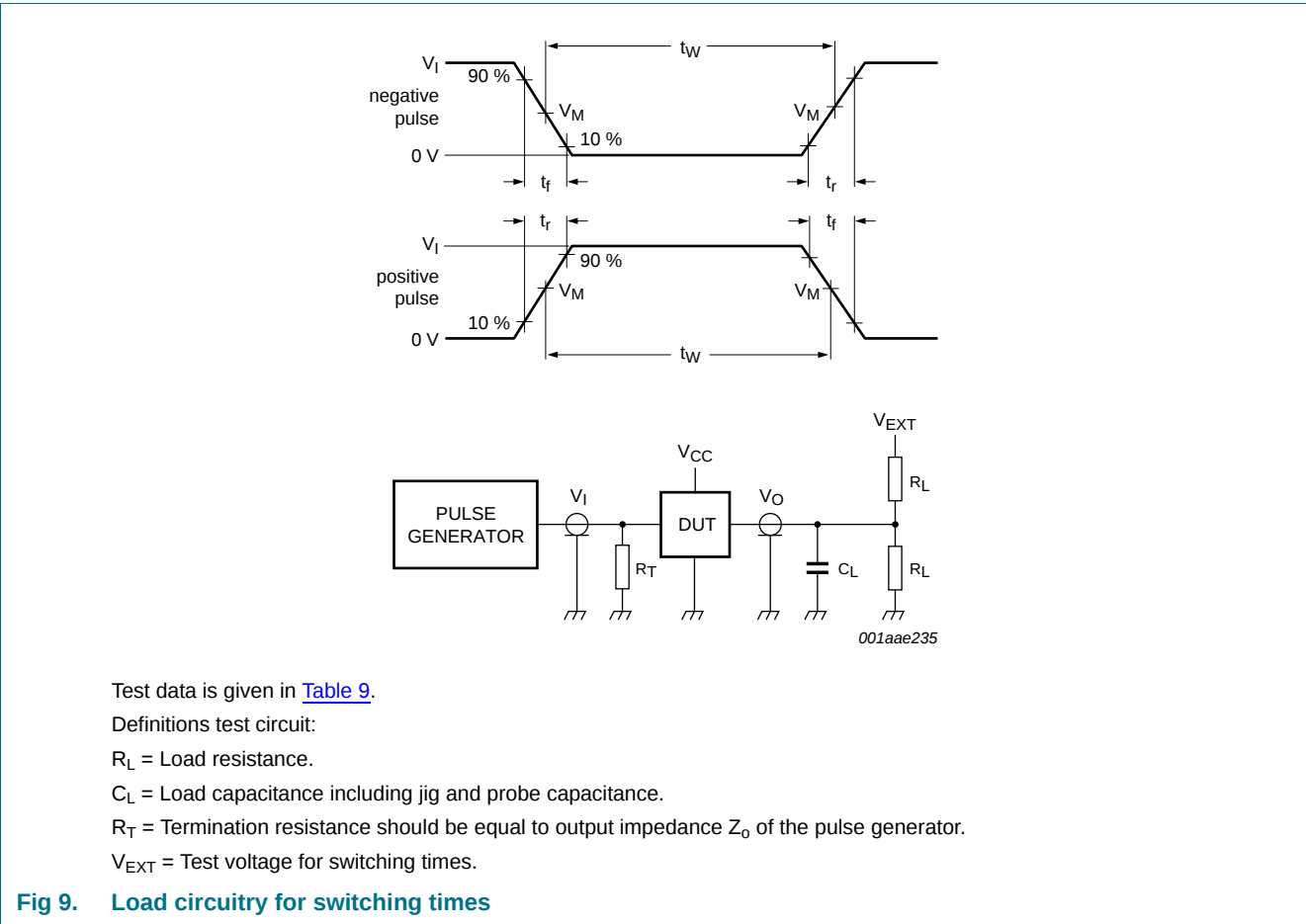


Measurement points are given in [Table 8](#)
Remark: The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 8. Data setup and hold times

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$



Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig 9. Load circuitry for switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	$\leq 10\text{ MHz}$	500 ns	$\leq 2.5\text{ ns}$	50 pF	500 Ω	GND	6 V	open

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

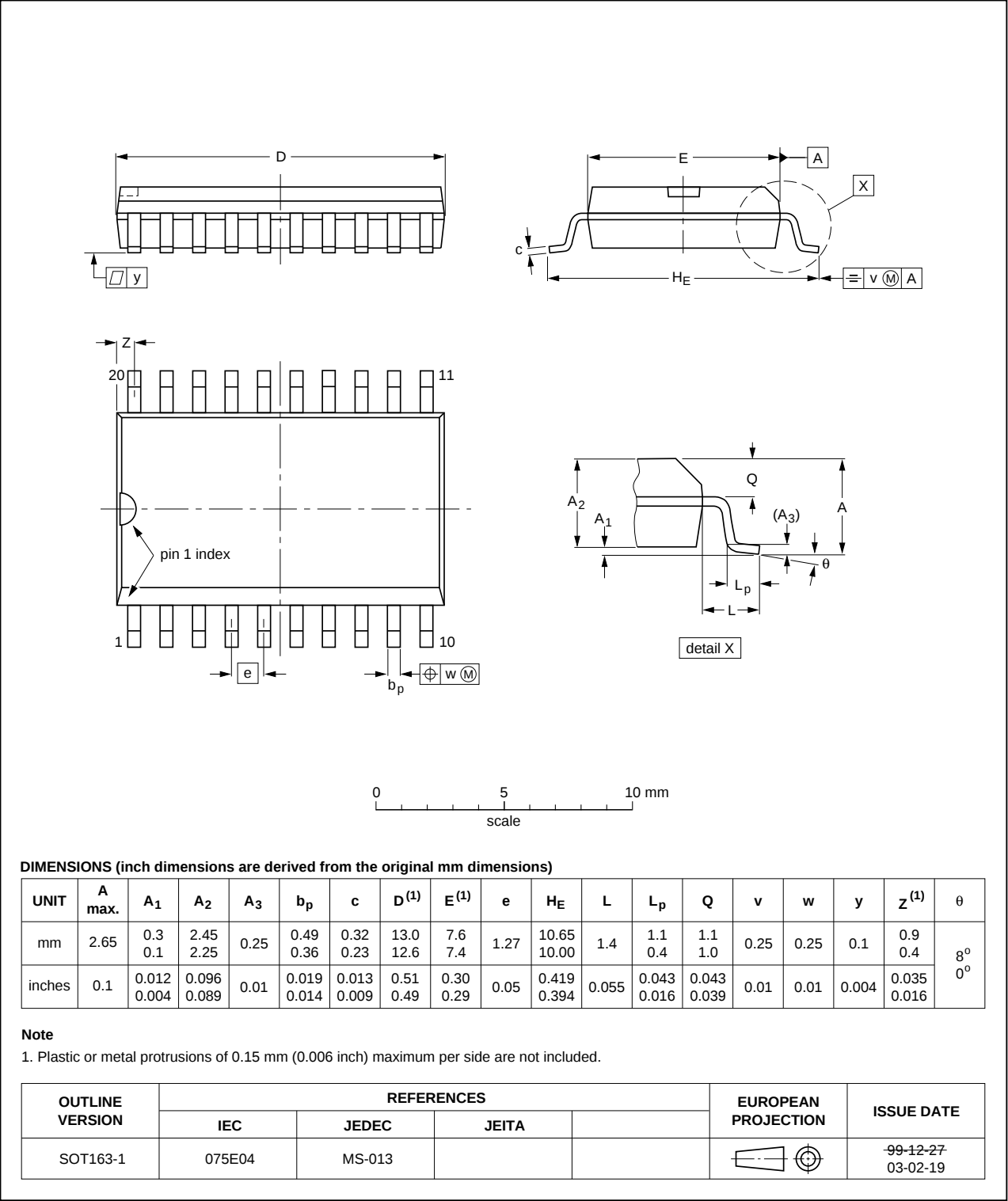


Fig 10. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

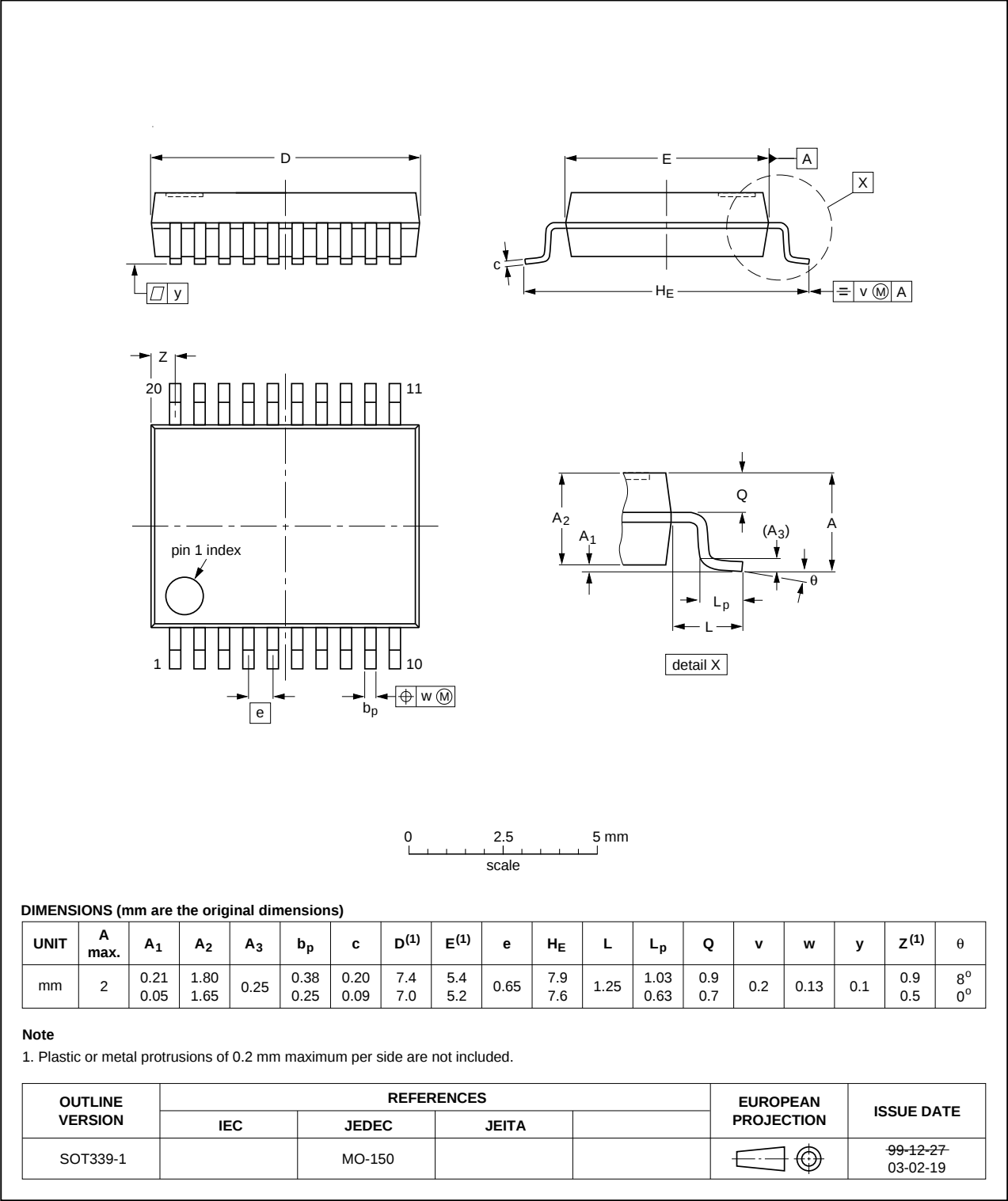


Fig 11. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

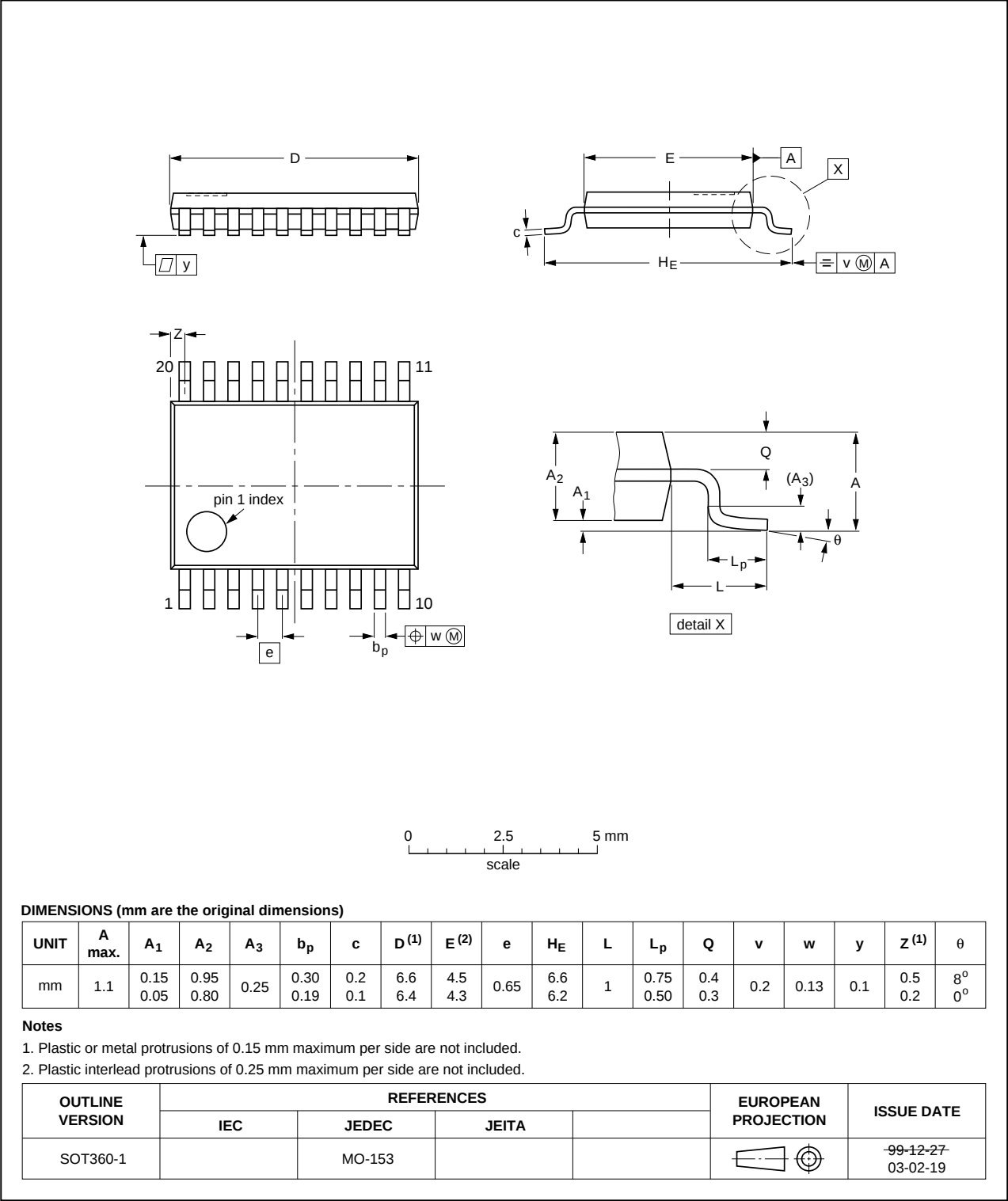


Fig 12. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MOS	Metal Oxide Semiconductor
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT374 v.3	20110914	Product data sheet	-	74LVT374 v.2
Modifications:	- Table 3 has been corrected for the disabled outputs mode (errata). - The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate.			
74LVT374 v.2	19980219	product specification	-	74LVT374 v.1
74LVT374 v.1	19960208	product specification	-	-

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15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	4
6.1	Function table	4
7	Limiting values	4
8	Recommended operating conditions	5
9	Static characteristics	5
10	Dynamic characteristics	6
11	Waveforms	8
12	Package outline	10
13	Abbreviations	13
14	Revision history	13
15	Legal information	14
15.1	Data sheet status	14
15.2	Definitions	14
15.3	Disclaimers	14
15.4	Trademarks	15
16	Contact information	15
17	Contents	16

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